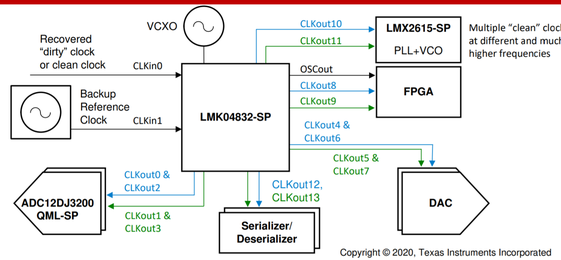
***Abstract*—The LMK04832-SP is a JESD204B compliant clock conditioner with integrated VCOs that can provide clock signals up to 3.2 GHz on up to 14 outputs. The device was tested for ELDRS and SEE and shown to be ELDRS-free, rated to 100 krad(Si) for low dose rate environments and SEL and SEFI immune. SEU characterization and RLAT data are also presented.**

Total Ionizing Dose and Single Event Effects Test Results of Texas Instruments LMK04832-SP (5962R1722701VXC) 3.2 GHz JESD204B Clock Jitter Cleaner with 14 Outputs

Kirby Kruckmeyer, Thang Trinh, Heriberto Castro, Aaron Black, Vibhu Vanjari, Ram Gooty, Samantha Williams and Derek Payne



LMK04832-SP 3.2 GHz JITTER CLEANER/CLOCK SYNTHESIZER

- Two PLLs and internal VCOs
- 3 configurable inputs
- 14 outputs

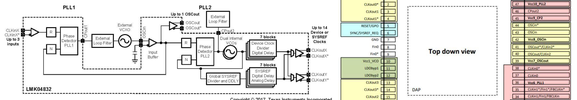
Supply: 3.15-3.45 V

Process: BiCMOS8B+
- BICMOS process with SiGe bipolar transistors

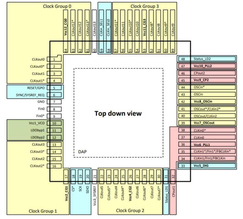
Different operating modes
- **Jitter cleaner:** dual loop mode; both PLLs enabled; external VXCO
- **Clock synthesizer:** single loop mode; PLL2
- **Clock distributor:** both PLLs disabled; up to 6.4 GHz input
- PLL2 can operate with internal or external VCOs

Outputs
- Configurable as 14 standard outputs or 7 JESD204B compliant outputs
- Output frequency and delay individually configurable
- Output format options: CML, LVPECL, LCPECL, HSDS, LVDS, or 2xLVCMOS

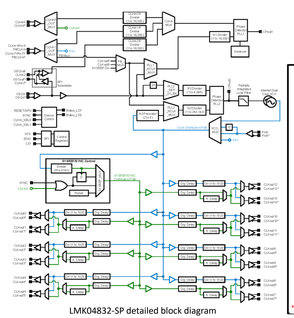
Configured by SPI
- Configuration held in registers
- Register settings can be read back



Block diagram as jitter cleaner (dual loop mode)



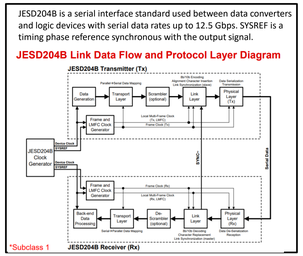
LMK04832-SP pinout



LMK04832-SP detailed block diagram

JESD204B is a serial interface standard used between data converters and logic devices with serial data rates up to 12.5 Gbps. SYSREF is a timing phase reference synchronous with the output signal.

JESD204B Link Data Flow and Protocol Layer Diagram



*Subclass 1

ELDRS Characterization

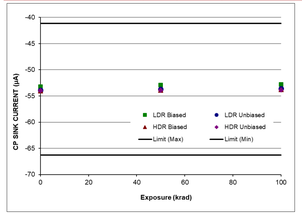
Enhanced Low Dose Rate Sensitivity (ELDRS) characterization per MIL-STD-883 Method 1019
- Devices under tests (DUT) received burn-in at 125°C for 240 hours prior to testing
- Different splits of DUTs were irradiated biased and unbiased at low dose rate (LDR) and high dose rate (HDR)
- Unbiased units have leads connected together during irradiation
- Biased units fully operational during irradiation; configured so that at all of the output configurations options (CML, LVPECL, LCPECL, HSDS, LVDS, and 2xLVCMOS) were exercised on at least one output each
- DUTs fully electrically tested to the product datasheet before irradiation and at each test point. Over 7000 parameters tested on each DUT
- Median parametric drift through 100 krad compared between LDR and HDR DUTs
- Test vehicle: early version of LMK04832

Condition	Dose Rate	DUT serial numbers	Test Points
LDR Biased	0.01 rad(Si)/s	33, 39, 41, 52, 53	0, 50, 100 krad(Si)
LDR Unbiased	0.01 rad(Si)/s	57, 58, 59, 61, 64	0, 50, 100 krad(Si)
HDR Biased	67.8 rad(Si)/s	5, 15, 19, 20, 24	0, 30, 50, 100 krad(Si)
HDR Unbiased	67.8 rad(Si)/s	25, 26, 28, 29, 32	0, 30, 50, 100 krad(Si)

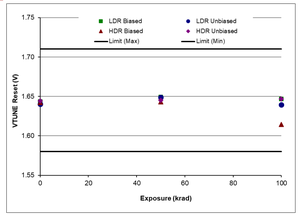
ELDRS Characterization Test Conditions	
Supply voltage	3.4 V
Supply current	570 mA
VCO and PLL frequency	3.2 GHz
LDR location	Cobham Rad, Colorado Springs, CO
HDR location	Texas Instruments, Santa Clara, CA
Electrical test locations	Texas Instruments, Santa Clara, CA
Electrical test supply voltage	3.135V, 3.3V, 3.465V
Parameters tested	7000+
Lot name	L01200248
Test dates	January 28 to July 1, 2020

Results

No parameters showed significant drift at LDR or significantly more drift at LDR when compared to HDR.
One parameter showed significant parametric at HDR with the units biased during irradiation.



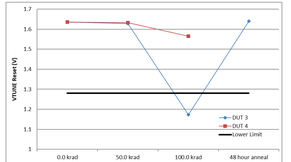
Typical plot of parametric readiings vs. radiation level. No significant parametric drift was seen through 100 krad on any parameters except VTUNE Reset Voltage.



VTUNE Reset Voltage was the only parameter to show significant parametric drift and only at high dose rate. No parameters showed significant drift at low dose rate.

Radiation Lot Acceptance Testing (RLAT)

- Since process was shown to be ELDRS-free, RLAT is done at HDR on a wafer level basis
- Per MIL-PRF-38535, RLAT sample size is 2 units for products with more than 4000 transistors
- One parameter drifted outside the test limit at 100 krad but recovered after a 48 hour room temperature anneal
- This qualifies wafer for 100 krad for dose rates lower than 0.58 rad/s
- Wafer is not qualified for high dose rates

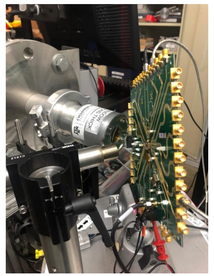


VTUNE Reset Voltage drifted out of spec on DUT 3 but recovered after 48 hour anneal. All other parameters remained within the test limits.

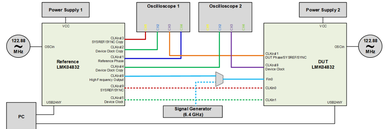
Single-Event Effects

DUT tested under 5 different operating conditions
-To ensure that all inputs, outputs, PLLs, VCOs and signal paths got tested

Functional Mode	Dual Loop	Dual Loop Nested 0-Delay	Single Loop 0-Delay	Distribution	Dual Loop, Holdover
SYSREF Enabled	No	Yes	Yes	Yes	Yes
Feedback MUX	No	SYSREF -> PLL1 N Divider	CLKout8 -> PLL2 N Divider	No	No
Holdover	No	No	No	No	Yes
Input	CLKin1	CLKin0	CLKin1	Fin0	CLKin1
Input Freq (MHz)	122.88	1.02	122.88	3200.00	122.88
PLL1 Enabled	Yes	Yes	No	No	Yes
PLL1 R and N Divider	120	1.00	N/A	N/A	120
External VCXO Freq (MHz)	122.88	122.88	N/A	N/A	122.88
PLL2 Enabled	Yes	Yes	Yes	No	Yes
PLL2 R Divider	1	1.00	4	N/A	1
PLL2 N Divider	13	12.00	4	N/A	10
PLL2 N Cal Divider	N/A	12.00	48	N/A	N/A
PLL2 N Prescaler	2	2.00	2	N/A	2
VCO Freq (MHz)	3194.88	2949.12	2949.12	N/A	2457.60
Output CLK Divider	24	24	24	24	20
Output Freq (MHz)	133.12	122.88	122.88	66.66	122.88
Test	SEL, SEU	SEFI, SEU	SEL, SEFI, SEU	SEL, SEFI, SEU	SEL, SEFI



DUT board at the beam. On the left is the hot air gun used to heat the DUT for SEL testing.



Block diagram of test setup. The reference frequency to the DUT was provided by a second LMK04832-SP.

Ion	LET (MeV-cm²/mg)	Incident Angle (Degree)	LETeff (MeV-cm²/mg)
Ne	2.8		
Ar	8.7		
Cu	29.5		
Ag	48	45	70
Au	88	40	121

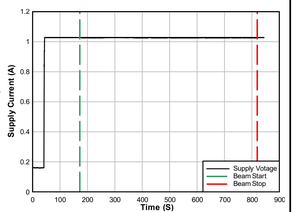
Heavy ion irradiation was done using the 15-A MeV cocktail and K500 beam line at the Texas A&M University Cyclotron Institute Radiation Effects Facility (TAMU).

Single-Event Latchup (SEL)

DUT tested under 4 modes as shown in top table
- Each mode tested at 121 MeV-cm²/mg to 1 x 10⁷ ions/cm²
- DUT case temperature monitored with thermistor
- DUT heated with hot air gun to case temperature of 125°C
  Junction temperature approximately 145°C
- Supply voltage at 3.45V as measured at DUT board

Results

No incidences of SEL detected during any ion runs. Supply current did monetarily drop by 4 mA or increase by 1 mA from ion strikes but always returned to nominal value.



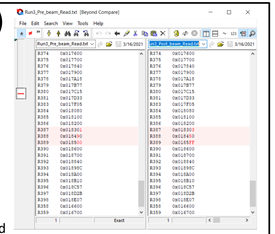
Supply current during one of the 4 SEL ion runs with the DUT case temperature at 125°C and junction temperature at 145°C. LETeff = 121 MeV-cm²/mg. Fluence = 1 x 10⁷ ions/cm².

Single-Event Functional Interrupt (SEFI)

SEFI monitored in two ways:
Register readings were read before and after ion runs and compared
Output was monitored during ion runs

Results

No incidences of SEFI detected during any ion runs
No resetting of the part or rewriting/scrubbing of registers required
During ion runs, output could be momentarily upset but always returned to programmed status at the end of the ion run
No programmable registers changed state through an ion run
Three status registers did change; one indicated the DUT lost lock and then relocked; the other two indicated that the DUT recalibrated itself



Comparing register readings before (left) and after (right) ion run. No programmable registers changed. Three status registers changed indicating self correction to SEUs.

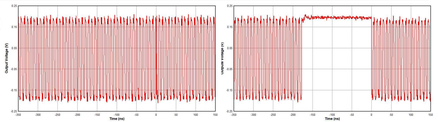
Single-Event Upset (SEU)

CLKout8 in LVDS mode
CLKout8* pin monitored with oscilloscope
Trigger set to "width" mode on falling edge

Results

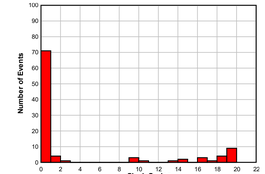
Two signatures seen:
- 67% SEUs one clock cycle or less
- 33% SEUs lasted more than one clock

Longest event lasted 22 clock cycles



67% of events recovered in one clock cycle or less — 33% of events lasted more than one clock cycle

SEU cross sections were calculated by dividing the number of event by the fluence at each LETeff.
Weibull plots was fitted to the data.
Event rates were calculated for LEO(ISS) and GEO environments by integrating the cross sections determined by the Weibull fits with the CREME96 orbital integral flux estimations assuming a minimum shielding configuration of 100 mils (2.54 mm) of aluminum, and "worst-week" solar activity (similar to a 99% upper bound for the environment). Also included is a Petersen Figure of Merit (FOM) calculation for each of the four operating modes tested.



Histogram of event length for one ion run. There were 100 events recorded during this ion run.

Weibull fit equation. Cross sections at highest LETeff tested (70 MeV-cm²/mg) were used for limiting cross sections.

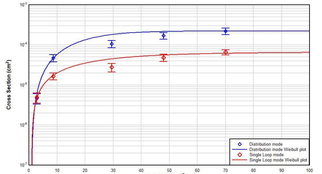
$$F(L) = A\left(1 - exp\left\{-\left[\frac{L - L_0}{W}\right]^s\right\}\right); L > L_0$$

where, $F(L)$ is the event cross-section for a particular LET
A is the limiting cross-section
W is the width of the distribution
L_0 is the threshold LET
s is the shape parameter

FOM equation. $L_{0.25}$ was determined from Weibull curve.

$$FOM = 200 \times \frac{A}{L_{0.25}}$$

where, A is the limiting cross-section
$L_{0.25}$ is the LET at 25% of the limiting cross-section



SEU cross section vs. LETeff for two of the modes tested

Mode	Weibull Fit Parameters A	Lo	W	s	Event Rate (Event/Day) LEO (ISS)	GEO	FOM
Dual Loop	8.54×10^{-5}	1	25	1.1	5.89×10^{-3}	5.85×10^{-2}	2.08×10^{-4}
Dual Loop Nested 0-Delay	7.41×10^{-5}	1	27	1.0	5.89×10^{-3}	5.95×10^{-2}	1.92×10^{-4}
Single Loop 0- Delay	6.60×10^{-5}	1	25	1.0	5.62×10^{-3}	5.69×10^{-2}	1.96×10^{-4}
Distribution	2.22×10^{-4}	1	20	1.5	1.00×10^{-2}	9.50×10^{-2}	4.70×10^{-4}

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