Application Report
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Glitch Free Power Sequencing With AXC Level Translators

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ABSTRACT

Today's complex systems have devices operating at multiple voltage nodes that require power sequencing. TI's latest AXC family from the general purpose direction-controlled translation portfolio has the flexibility to be powered up or down in any sequence while avoiding the false power on and power off glitches. This application note focuses on measuring the power sequencing performance of the SN74AXC1T45 under different conditions through thorough lab testing.

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1 Introduction

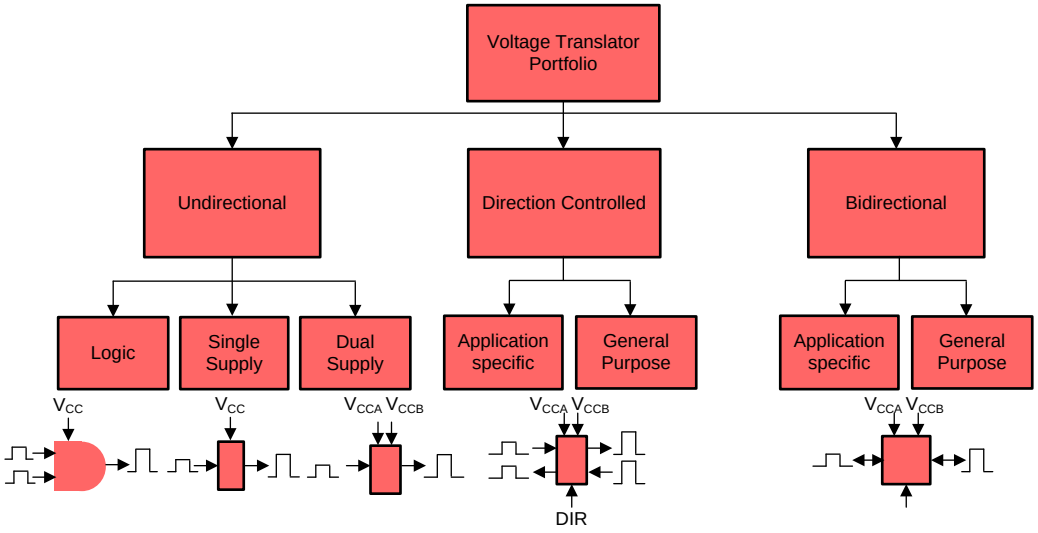

Figure 1. TI Translation Portfolio

For a comprehensive guide for understanding voltage translation, refer to the *Basics of Voltage-Level Translation* application report.

The AXC translation device family comes under the general-purpose direction-controlled translators category which also contain the existing AVC and LVC families as seen from Figure 1. Please watch the Introduction to AXC family video for more information about the AXC family.

Refer to the *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters* application report for information regarding LVC translator family.

Figure 2 shows the internal architecture of the AXC IO cell with the glitch suppression circuitry and power-up hi-Z circuitry controlled by the power on reset control block. The power-up hi-Z circuit is before the output drive stage and ensures that the IO ports are in high impedance until both supplies have reached a certain threshold required for operation. The power-on control block also ensures enough hysteresis to avoid oscillations during slow ramp up of power supplies due to supply droop. The control block senses the direction pin, output enable pin (not external in SN74AXC1T45) along with the two supplies. The glitch suppression circuit ensures there are no glitches once the IO cells are out of high-impedance state and are active.

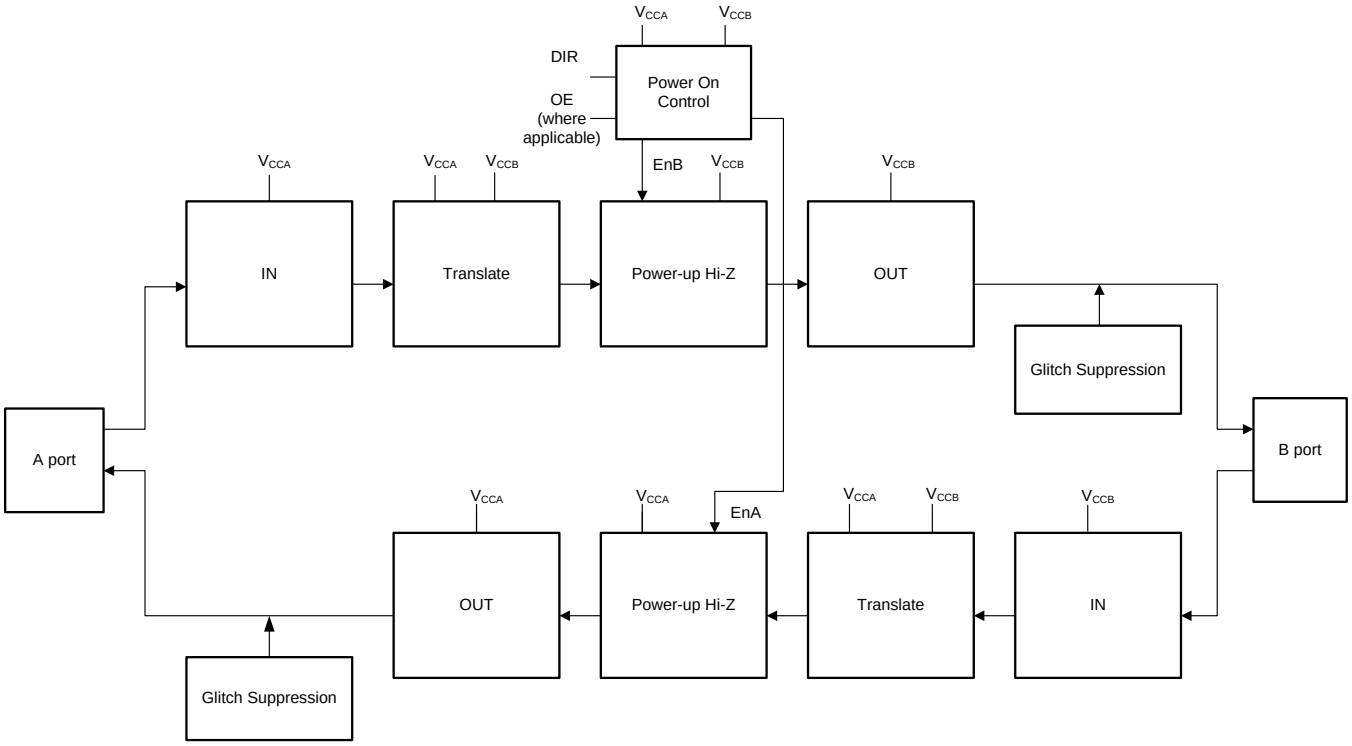

Figure 2. Internal Architecture of AXC IO

2 Bench Setup and Conditions

Extensive power sequencing for various power-up and power-down scenarios, which are typically expected in the system, have been tested in the lab to ensure reliable operation in the system application. Figure 3 shows the basic setup for the power sequencing testing. With DIR pin low, the signal flow is from B to A and when the DIR pin is tied high to V_{CCA}, the signal flow is from A to B. Each power supply pin (V_{CCA} & V_{CCB}) is forced to 0.65V and 3.6V along with the inputs which is set to ground. The faster ramp time is set to 50 µs and the ramp rate can be calculated as per the Table 1. When the V_{CCA} leads V_{CCB}, V_{CCA} supply pin ramps up first and once it reaches steady state, the V_{CCB} ramps next. When the V_{CCA} lags V_{CCB}, the ramp starts first on the V_{CCB} pin and once it reaches steady state, the V_{CCA} supply ramps. When V_{CCA} tracks V_{CCB}, both the supplies ramp together. Total combinations for single-channel power sequencing come to a total of 192 measurements.

Table 1. Ramp rate calculation

Transition Time	Supply Voltage (V)	Ramp Rate (s/V)
50 µs	0.65	77 µ
50 µs	0.80	62.5 µ
50 µs	3.60	14 µ

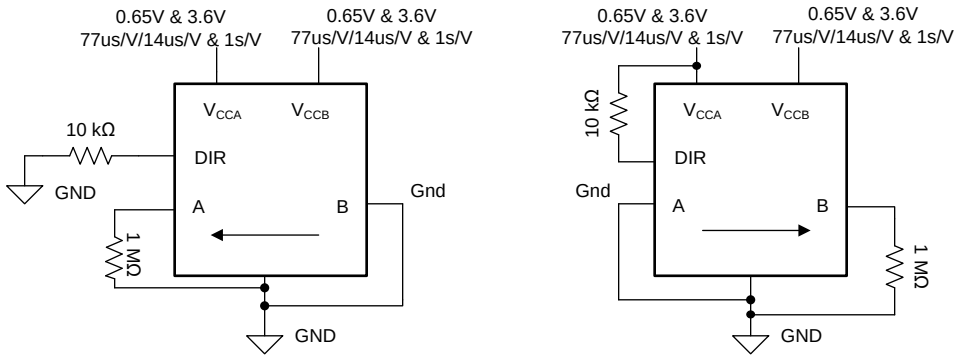

Figure 3. Power Sequencing Setup

The analysis compares the power sequencing performance of the SN74AXC1T45 to an existing competitor device which closely represents SN74AXC1T45 functionality. As the AXC device is rated to operate from 0.65 V, the lower voltage during the power sequence testing for the AXC device is set to 0.65 V; however, the lower voltage for the competitor device is set to 0.8 V to conform to the recommended operating specifications of the competitor. The higher voltage for both the SN74AXC1T45 and the competitor device is set to 3.6 V.

The results are shown and discussed in Section 2.1.

2.1 Heat Map of Competition vs AXC1T45

For the following tables:

- Green cell - No Glitch
- Red cell - Indicates Glitch either during startup or shutdown
- V_{OH} (logic output high) - V_{OL} (logic output low) = Glitch on the output that crosses the V_{OH} and V_{OL} threshold levels

Table 2. Heat Map Summary: Competition Device at 25°C

COMPETITOR				DIR =>	B to A			A to B		
Ramp Time		Supply Voltage		Ramp sequence=>	V_{CCA} lags V_{CCB}	V_{CCA} leads V_{CCB}	V_{CCA} tracks V_{CCB}	V_{CCA} lags V_{CCB}	V_{CCA} leads V_{CCB}	V_{CCA} tracks V_{CCB}
V_{CCA} Ramp Rate (s/V)	V_{CCB}Ramp Rate (s/V)	V_{CCA} (V)	V_{CCB} (V)	Input=>	GND	GND	GND	GND	GND	GND
1	1	3.60	3.60							
1	62.5 µ	3.60	0.80							
1	14 µ	3.60	3.60							
1	1	3.60	0.80							
62.5 µ	1	0.80	3.60			V_{OH} - V_{OL}				
14 µ	1	3.60	3.60							
62.5 µ	62.5 µ	0.80	0.80			V_{OH} - V_{OL} (1)				
62.5 µ	14 µ	0.80	3.60			V_{OH} - V_{OL}				
14 µ	62.5 µ	3.60	0.80							
14 µ	14 µ	3.60	3.60					Refer to Figure 5		
62.5 µ	1	0.80	0.80							
14 µ	1	3.60	0.80							
1	1	0.80	3.60							
1	62.5 µ	0.80	0.80							
1	14 µ	0.80	3.60							
1	1	0.80	0.80							

(1) Refer to Figure 4

Table 3. Heat Map Summary: SN74AXC1T45 at 25°C

SN74AXC1T45				DIR =>	B to A			A to B		
Ramp Time		Supply Voltage		Ramp sequence=>	V_{CCA} lags V_{CCB}	V_{CCA} leads V_{CCB}	V_{CCA} tracks V_{CCB}	V_{CCA} lags V_{CCB}	V_{CCA} leads V_{CCB}	V_{CCA} tracks V_{CCB}
V_{CCA} Ramp Rate(s/V)	V_{CCB}Ramp Rate (s/V)	V_{CCA} (V)	V_{CCB} (V)	Input=>	GND	GND	GND	GND	GND	GND
1	1	3.60	3.60							
1	77 µ	3.60	0.65							
1	14 µ	3.60	3.60							
1	1	3.60	0.65							
77 µ	1	0.65	3.60							
77 µ	1	3.60	3.60							
77 µ	77 µ	0.65	0.65			Refer to Figure 4				
77 µ	14 µ	0.65	3.60							
14 µ	77 µ	3.60	0.65							
14 µ	14 µ	3.60	3.60					Refer to Figure 5		
77 µ	1	0.65	0.65							
14 µ	1	3.60	0.65							
1	1	0.65	3.60							
1	77 µ	0.65	0.65							
1	14 µ	0.65	3.60							
1	1	0.65	0.65							

The numerous red cells shown in the Table 2 competition heat map indicate glitches in the output for the different power sequencing combinations. There are few glitches that only cross the output V_{OH} threshold, few glitches that cross the V_{OL} threshold, and some glitches that cross both V_{OH} and V_{OL}thresholds.

Test Cases Comparison:

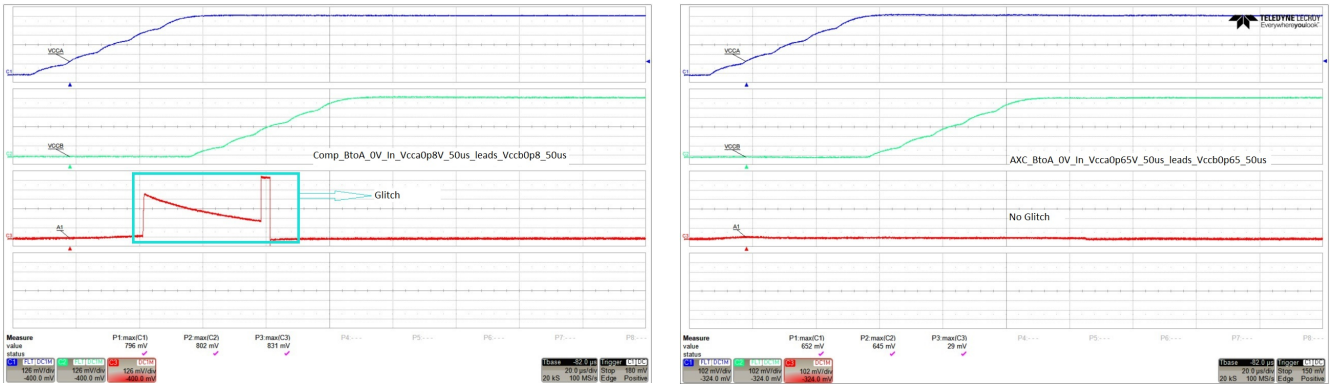

Figure 4. Competition (0.8 V) vs AXC (0.65 V), 50-µs (Fast) Ramp With 0-V Input

Figure 4 shows a comparison between competitor device and the AXC device when the input is at 0 V. V_{CCA} leads V_{CCB} with both the supplies at 0.8 V (0.65 V for the AXC) and ramping at 50 µs. The direction pin is set so the signal flow is from B to A. The glitch observed on the competition device ramps up, slowly ramps down, and shoots up to V_{CC} voltage for about 5 µs before shutting down. The AXC device remains at logic low throughout.

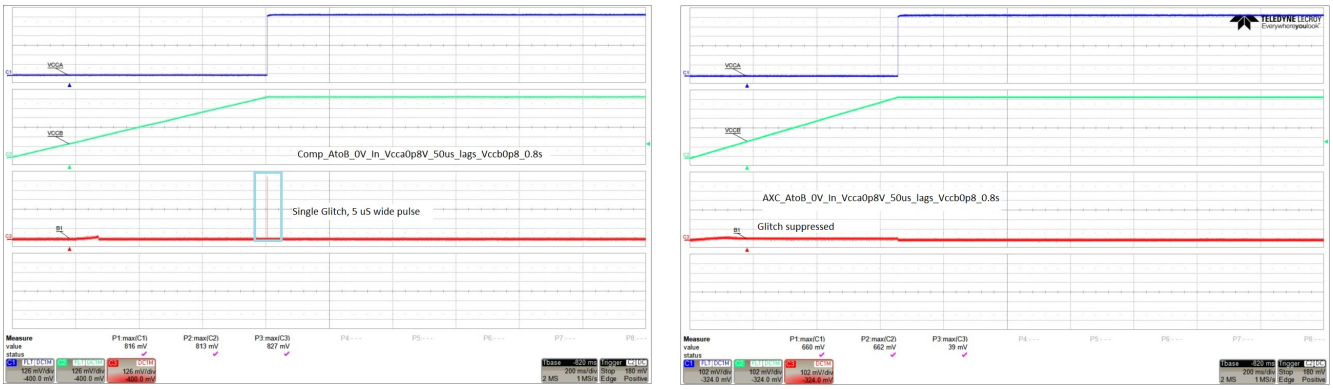

Figure 5. Competition (0.8 V) vs AXC (0.65 V), Slow Output Ramp 0.8 s (1 s/V) With 0-V Input

Figure 5 shows a comparison between competition and the AXC device when the input is at 0 V. V_{CCA} lags V_{CCB} with both the supplies at 0.8 V for the competition and 0.65 V for the AXC. V_{CCA} is ramping at 50 µs, and V_{CCB} is ramping at 0.8 s (0.65 s for AXC). The direction pin is set so the signal flow is from A to B. There is a single glitch observed on the competition device that stays at V_{CC} voltage for about 5 µs. The AXC device remains at logic low throughout.

The multiple transitions around the threshold region can lead to abnormal behavior such as unintentional reset, frozen operation due to false clocking, false interrupt and false reset in the user applications.

3 References

1. Texas Instruments, *Basics of Voltage-Level Translation*
2. Texas Instruments, *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*
3. Texas Instruments, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards*

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