Application Report
SLVA922–September 2017

Optimize DC-DC Layout for SOT Package to Improve Thermal and Voltage Spike

Edwin Zang, Nick Chen

ABSTRACT

An optimized layout is important to the performance of DC-DC regulators. This application report focuses on improving the impact of thermal and switching spike voltage. First, the layout rule is discussed. Next, three different kinds of layouts are created, depending on the layout guide, using the TPS565201. Lastly, by creating a PCB model, and testing thermal, switching ringing, and efficiency, an optimized layout of the TPS565201 is created. This layout can be used for the TPS56x20x series family.

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Trademarks

1 Introduction

The TPS56x20x series including: TPS561201/8, TPS562201/8, TPS563201/8, and TPS564201/8 are star parts, which have various applications such as DTV, STB, surveillance, networking home terminal, and so on. However, as loading current gets heavier and heavier, some performance is influenced, for example the thermal and switching spike voltage. In addition, when the IC temperature is very high, many parameters will seriously drift. Because of this, an optimized layout is more and more important. A good layout not only helps lower thermal resistance of the package, but also decreases spike voltage on the internal FETs. This application report mainly discusses the layout effect on thermal and switching spike voltage.

The TPS565201 is a simple, easy-to-use, synchronous step-down converter. The device is available in a 6-pin, 1.6 × 2.9 (mm), SOT (DDC) package.

2 Layout Guide

In general, all external components must be placed as close as possible to the power IC. The most important consideration is the placement of the input capacitors and output LC filter.

Placement and connection of the input capacitor is critical. The goal is to reduce parasitic inductance between the input capacitor and IC input voltage pin. Also, the input capacitor ground must be directly connected to the power ground to reduce induction of the ground connection.

High parasitic inductance increases spike voltage on the internal FETs during switching rise and fall time, as shown in Figure 1 (see Equation 1). Reducing the parasitic inductance is essential to prevent EOS events.

$$V_{inx} = V_{in} + L_{par} \times di / dt \quad (1)$$

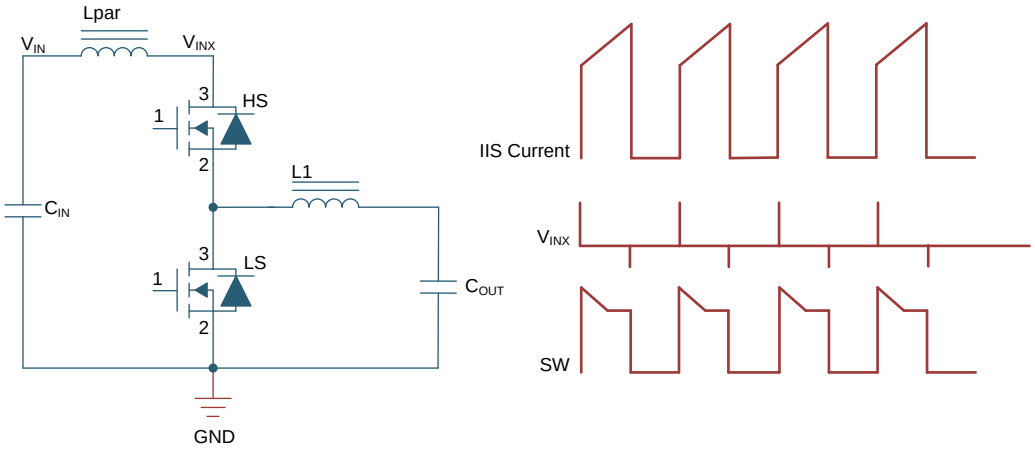


Figure 1. Spike Voltage of Internal FET

Parasitic inductance can be reduced by making the path from the input capacitor to the IC input voltage pin as short and wide as possible. The goal is to make the connection length around 0.05 inches.

Try to place the inductor close to the power IC to keep the switching trace as short and wide as practical, to minimize radiated emissions. Also, try to keep the switching trace on the same layer to avoid layer changes.

The output capacitors must be close to the inductor, at the same time, the ground path must provide enough short path between the input capacitors, output capacitors, and IC ground pin. During regulator on time, the AC current flows from the input capacitors, through the power IC high-side FET, inductor, and output capacitors, to the input capacitors ground. During regulator off time, the AC current flows from the IC low-side FET, inductor, and output capacitors to the IC ground (see Figure 2).

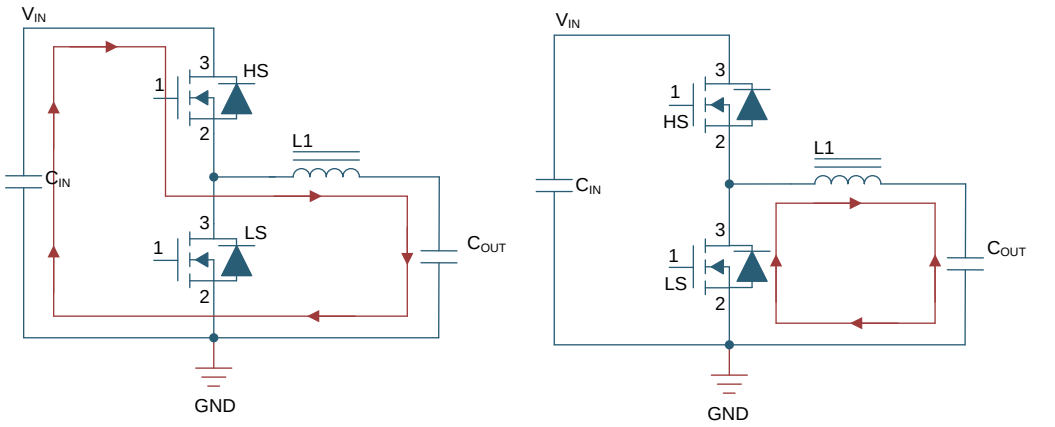


Figure 2. AC Current Flow

3 Device Description

3.1 Three Layout Types

The version 1 EVM is the same as released the TPS564201 EVM. The version 2 and version 3 EVM layouts are created according to the previous layout rules.

On the version 1 EVM, the input capacitor ground and output capacitor ground share the same ground area to guarantee enough short ground connection. The disadvantage of this layout is that the switching trace goes through from the top layer to the bottom layer then back to the top layer with the connecting inductor; and the input capacitor, C1, is not close enough to the IC (see Figure 3).

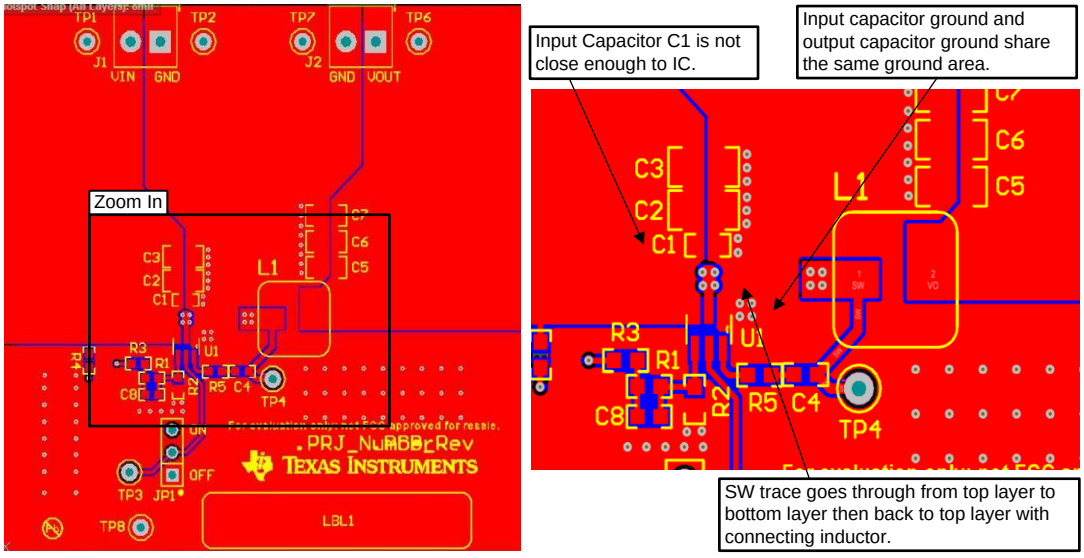


Figure 3. Version 1 EVM

On the version 2 EVM, the connection of the input capacitor ground and output capacitor ground is same as the version 1 EVM. The difference in this layout is that the switching trace is connected with the inductor at the back of the power IC, so the switching trace is short. The drawback is that the back part of the IC is not wide enough. C1 is placed as close as possible to the power IC. The disadvantage of this layout is that the FB pin is near the switching trace. The FB pin is much more sensitive to noise, so high-frequency noise is easily injected to the IC from the FB pin. At the same time, high-frequency switching voltage at the back of the IC has some influence on stability and performance (see Figure 4).

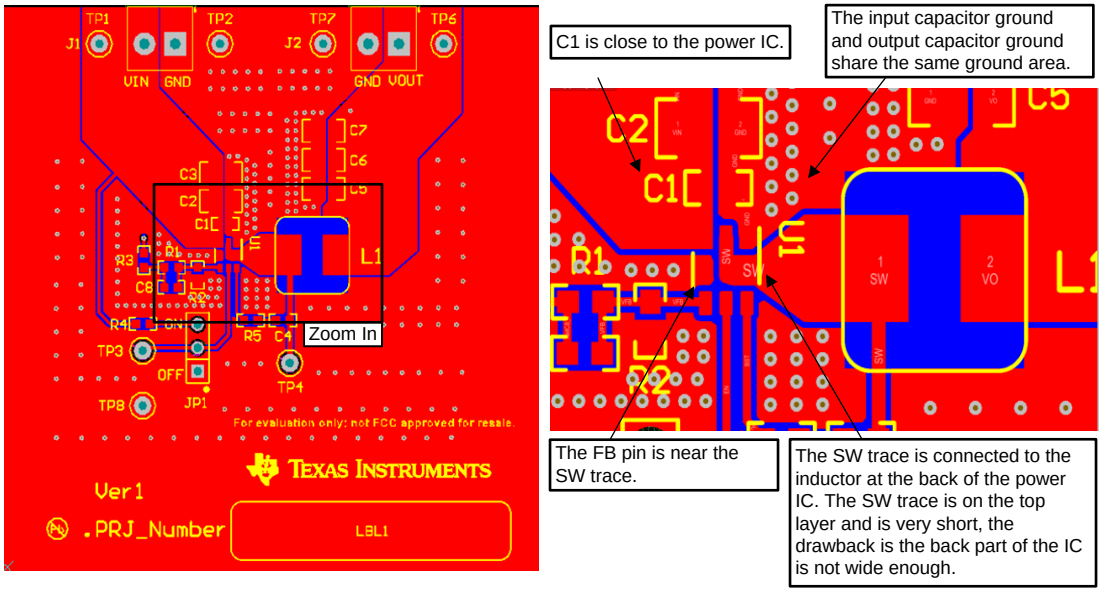


Figure 4. Version 2 EVM

Figure 5 shows the version 3 EVM. The switching trace connects to the inductor directly, which can keep the trace short and wide enough. The input capacitor, C1, is placed as close as possible to the power IC. The input capacitor ground and output capacitor ground are connected at the back of the IC. The disadvantage of this layout is that the distance between the input ground and output ground is larger than that of version 1 and version 2. However, the ground area at the back of the IC is helpful for thermal.

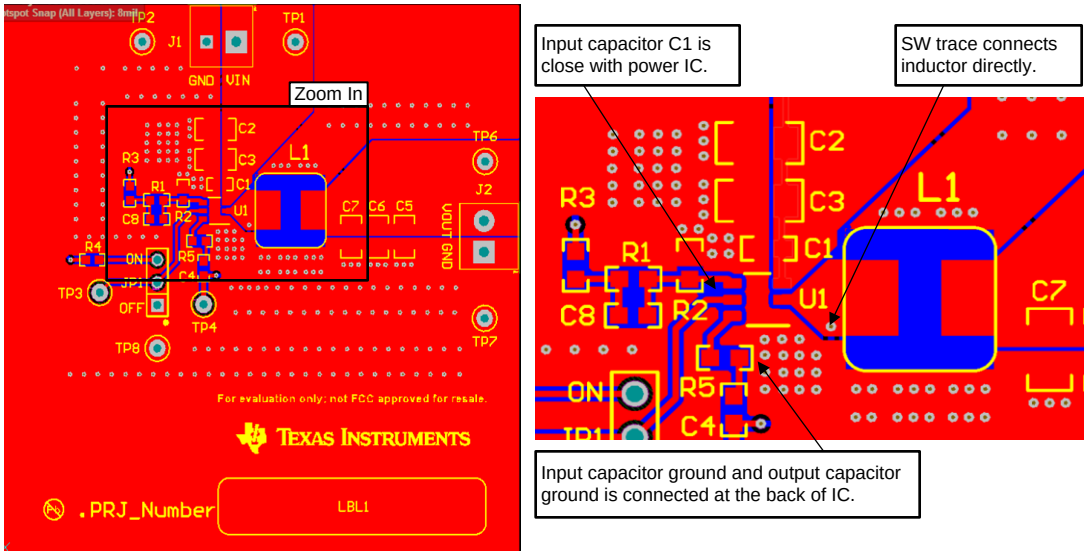


Figure 5. Version 3 EVM

4 Results

4.1 Model of EVM PCB Layout

Depending on the EVM layout printed line, electronic parasitic parameters can be generated.

Figure 6 shows the circuit schematic with major parasitic parameters. The inductors PL1 and PL2 are parasitic inductors between the input capacitor and IC. The switching spike voltage is influenced by the inductor PL1. The inductor PL2 causes ground bouncing at the moment when the low-side FET turns from on to off. due to clamp of low side bode diode, bouncing voltage is very small, so parasitic inductor PL2 has litter effect on the switching spike voltage. The inductor PL3 is the parasitic inductor between the IC switching pin and L1 inductor. The inductor PL3 is very small compared with the inductor L1, so it can be ignored. PR1, PR2, and PR3 are the parasitic resisters that have some effect on efficiency. PC1 is the parasitic capacitor between the FB pin and switching pin. This parasitic capacitor indicates that the FB is coupled with noise from the switching.

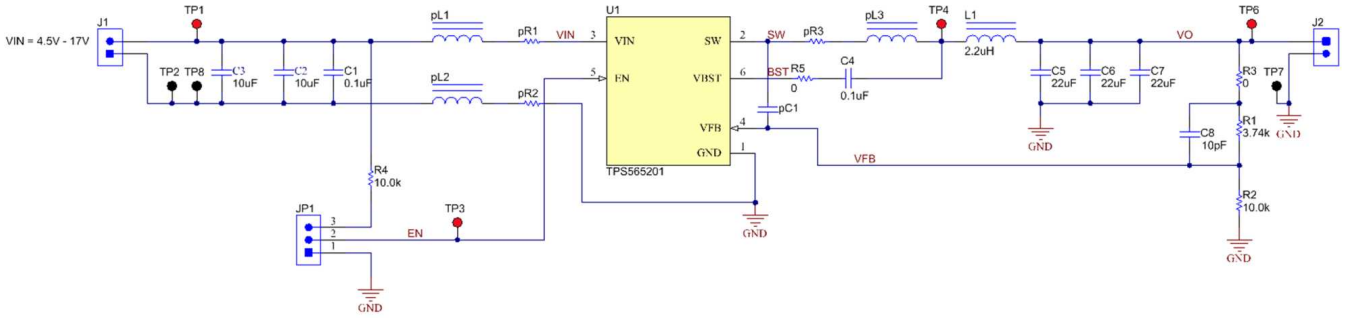


Figure 6. Schematic With Parasitic Parameters

Table 1 lists the major parasitic parameters of the three different versions of the EVM. From Table 1, users can see that the parasitic inductance, PL1, of version 2 and version 3 is smaller than that of version 1, so switching ringing of version 2 and version 3 should be smaller than that of version 1. The parasitic resisters, PR1 and PR2, of the three different EVM are about same. PR3 of version 3 is smallest and PR1 is biggest. PC1 of version 3 is the smallest compared with other two versions.

Table 1. Parasitic Inductance

Parasitic Parameter	Version 1	Version 2	Version 3
PL1 (nH)	1.4517	0.225	0.51491
PL2 (nH)	1.1839	0.221	1.133
PL3 (nH)	6.7	1.49	1.6
PR1 (mΩ)	0.393	0.217	0.256
PR2 (mΩ)	0.332	0.223	0.336
PR3 (mΩ)	1.98	0.882	0.479
PC1 (pF)	0.0045	0.0064	0.0009

4.2 Switching Ringing

For typical application, use a 12-V input voltage and 5-V, 5-A output to test the switching waveform (see Figure 7). For version 1, the spike voltage of the switching is 15.8 V, due to the large parasitic inductor PL1. For version 2 and version 3, the spike voltage of the switching is 13.1 V and 13.2 V, because the parasitic voltage is small.

Table 2. Switching Spike Voltage

Version	Switching Spike Voltage
Version 1	16.1 V
Version 2	13.1 V
Version 3	13.2 V

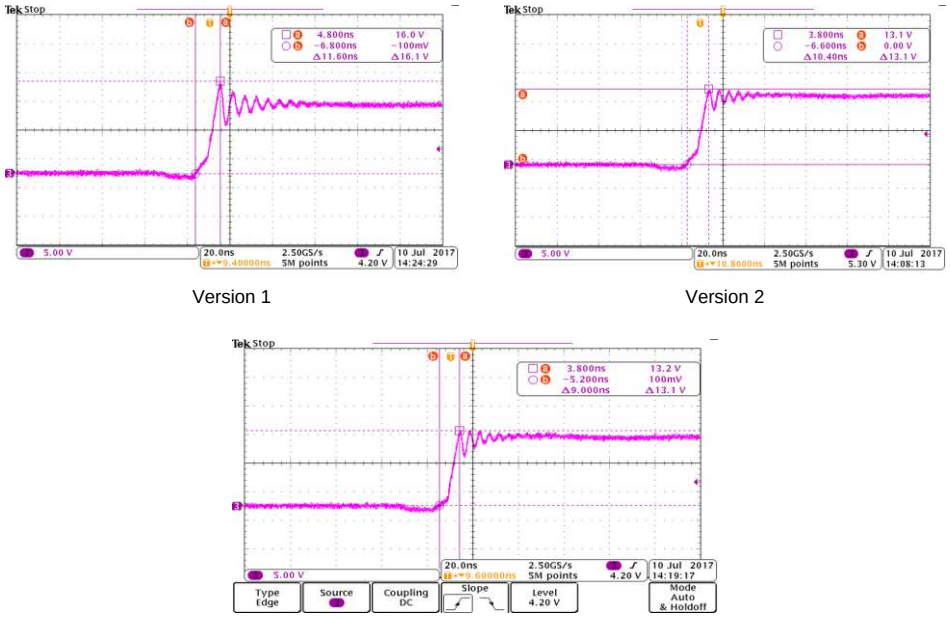


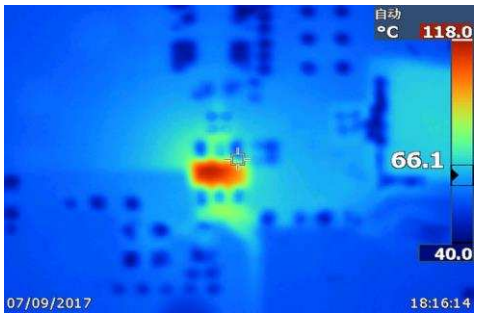
Figure 7. Switching Ringing

4.3 Thermal

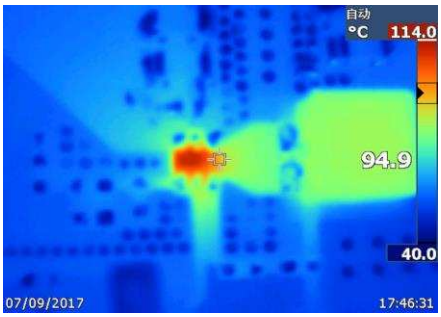
Table 3 lists the EVM thermal at typical application. For version 1, the temperature is the highest at 118°, because the bottom layer switching trace could not help the IC to dissipate heat. Due to the switching trace being at the back of the EVM board, its temperature could not be seen. For version 2, the temperature is 114° and for version 3 the temperature is 104°. For version 2, the temperature of the IC, switching trace, and inductor is high because the switching trace under the IC is narrow and the IC overlaps the switching trace. For version 3, there is ground area at the back of the IC. The ground responds well to the thermal pad, which is helpful to the thermal (Figure 8).

Table 3. Thermal

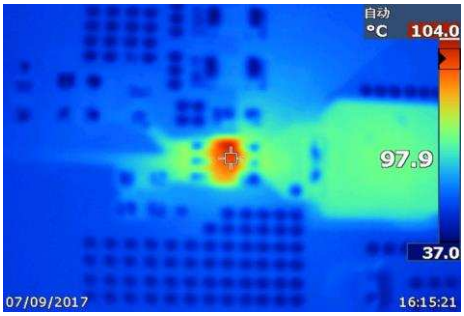
Version	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Temperature (°C)
Version 1	12	1.2	5	98
	12	5	5	118
Version 2	12	1.2	5	95
	12	5	5	114
Version 3	12	1.2	5	88
	12	5	5	104



Version 1



Version 2



Version 3

Figure 8. Thermal

4.4 Efficiency

Efficiency is tested at 5 V_{OUT} and 3.3 V_{OUT}, see Table 4. In version 3, the efficiency is slightly higher than version 2 and verison 1.

Table 4. Efficiency

Version	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Efficiency
Version 1	12	3.3	5	88.87%
	12	5	5	91.72%
Version 2	12	3.3	5	89.35%
	12	5	5	91.96%
Version 3	12 V	3.3	5	89.79%
	12	5	5	92.18%

5 Summary

According to the layout rule, two versions of the layout are created with the TPS565201 device; and three different layout versions are compared, by switching spike voltage, thermal, and efficiency. The most optimized layout is version 3, this optimized EVM layout is appropriate for any TPS56x20x series family part. The priorities of the layout guide are as follows:

- All external components must be placed as close as possible to the power IC.
- The input capacitor must be placed as close as to the device as possible to minimize parasitic inductance.
- Keep the switching trace as physically short and wide as practical.
- Try to minimize the distance from the output capacitor ground and input capacitor ground.

6 References

- Texas Instruments, TPS564201 4.5-V to 17-V Input, 4-A Synchronous Step-Down Voltage Regulator in SOT-, data sheet.

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