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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

How the voltage reference affects ADC performance, Part 3

By Bonnie Baker, *Senior Applications Engineer,*
and Miro Oljaca, *Senior Applications Engineer*

This article is Part 3 of a three-part series that investigates the design and performance of a voltage-reference system for a successive-approximation-register (SAR) analog-to-digital converter (ADC). Part 1 (see Reference 1) examined the ADC characteristics and specifications, with a particular interest in the gain error and signal-to-noise ratio, while assessing how the voltage reference impacts the ADC transfer function and DC accuracy. Part 2 (see Reference 2) examined the voltage-reference characteristics, focusing on how the voltage-reference noise produces the most error at the converter's full-scale range. Part 2 concluded by presenting a design for a voltage-reference circuit that is appropriate for 8- to 14-bit converters. This article, Part 3, tackles the challenge of designing a voltage-reference circuit that is appropriate for converters with 16+ bits. Part 3 examines methods of improving noise filtering and of compensating for losses caused by the improved filters.

Basics of reducing voltage-reference noise

As discussed in Part 2, the two sources of noise in the reference voltage are the internal output amplifier and the bandgap. The voltage-reference circuit from Part 2 that was configured with an 8- to 14-bit ADC can be used as a starting point to continue the discussion. The size of the least significant bit (LSB) of any converter in a 5-V system is equal to $5\ V/2^N$, where N is the number of converter bits. The 8-bit LSB size in this environment is 19.5 mV, and the 14-bit LSB size is 305 µV. The target value for voltage-reference noise should be less than these LSB values. The bandgap noise of the circuit from Part 2 was reduced by adding an external capacitor to the output to create a low-pass filter. This circuit's output noise can be further reduced by adding another capacitor as a passive low-pass filter. Figure 1 shows an example of such a design, which uses a voltage reference from the Texas Instruments (TI) REF50xx family. In this design, the 1-µF capacitor (C_1) provides a minimal 21-dB noise reduction at the internal bandgap reference. C_2, in combination with the open-loop output resistance (R_O) of the voltage reference's internal amplifier (see Reference 4), further reduces the output noise of the reference at the V_{REF_OUT} pin. In this case, the equivalent series resistance (ESR) of the 10-µF ceramic capacitor (C_2) is equal to 200 mΩ.

Figure 1. Voltage-reference design appropriate for 8- to 14-bit converter

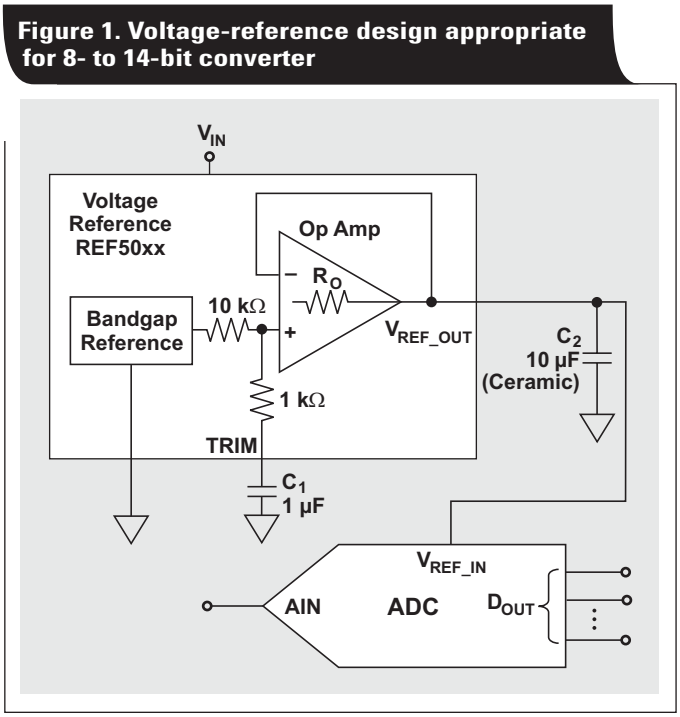


Figure 2 shows a fast-Fourier-transform (FFT) plot of the output signal of the circuit in Figure 1. Note that the output-noise level peaks at around 9 kHz because of the response of the circuit's internal amplifier to the capacitive load (C_2). This peaking is the main contributor to the overall measured noise. This output noise, measured with an analog meter over a frequency range of up to 80 kHz, is approximately 16.5 μV_{RMS}. If the voltage-reference circuit was connected to the input of an ADC, the measured noise across a 65-kHz frequency range would be 138 μV_{PP}. This noise level makes the solution in Figure 1 adequate for 8- to 14-bit converters.

Reducing voltage-reference noise for an ADC with 16+ bits

Since the voltage-reference circuit in Figure 1 would introduce too much noise into a converter with 16+ bits, another low-pass filter can be added to further reduce the reference's output noise. This filter consists of a 10-kΩ resistor (R_1) and an additional capacitor (C_3) as shown in Figure 3. The corner frequency of this added RC filter, 1.59 Hz, will reduce broadband noise as well as noise at extremely low frequencies.

Figure 2. FFT plot of V_{REF_OUT} signal of circuit in Figure 1

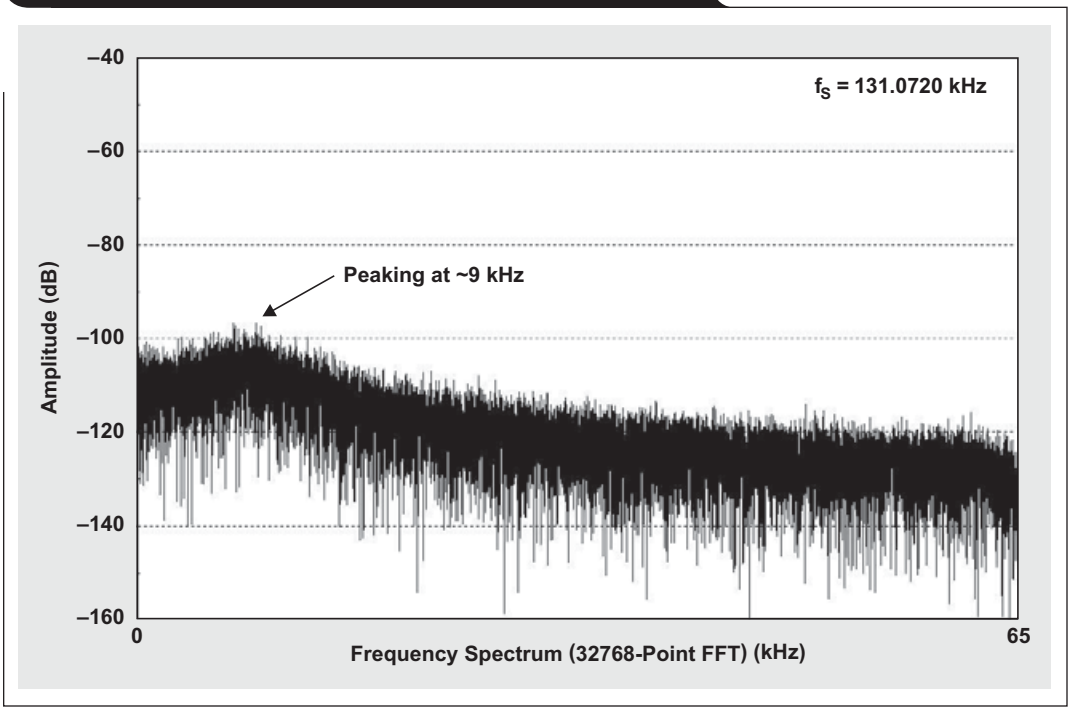


Figure 3. Voltage-reference circuit with R_1 and C_3 added as filters

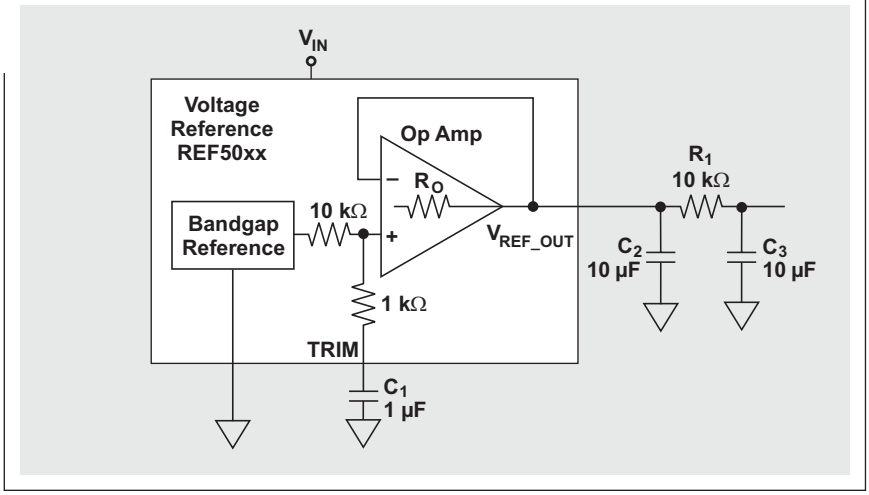


Figure 4. FFT plot of V_{REF_OUT} signal of circuit with RC filter added

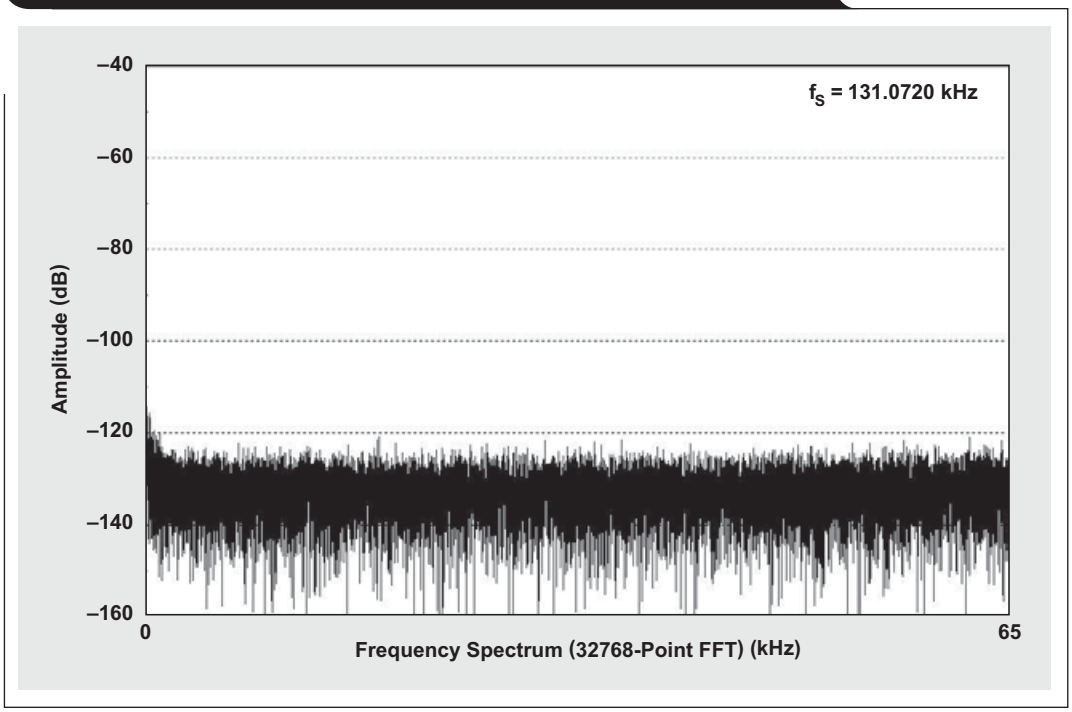


Figure 4 shows that the addition of R_1 and C_3 has a significant effect on the output noise for this system. The 9-kHz noise peak is gone. With this signal response, the output noise of the reference circuit in Figure 3 becomes 2.2 μV_{RMS} or 15 μV_{PP}, a reduction of nearly 90%. This improvement brings the noise level so well under control that the voltage-reference circuit is now appropriate for ADC resolutions of up to 20 bits.

This is encouraging; however, pulling current through R_1 from the ADC reference pin will corrupt the conversion by introducing a voltage drop equivalent to the average charge level from the reference pin of the ADC. Consequently, the output of this new circuit will not be able to adequately drive the ADC's voltage-reference input. To accomplish this, a buffer will need to be added to the low-pass filters.

Adding a buffer to the voltage-reference circuit

Figure 5 shows an example of the fluctuations in ADC reference drive current that can occur during a conversion. The signal was captured with a low-capacitance probe to show the voltage drop across the 10-kΩ resistor (R_1) between the input of the ADC voltage-reference pin and V_{REF_OUT}. The top trace in Figure 5 shows the trigger signal that the converter receives to initiate a new conversion. The ADC's voltage-reference circuit demands different amounts of current (bottom trace) for the initiation of the conversion and for each code decision. Therefore, the voltage-reference analog circuitry connected to the ADC must be able to accommodate these high-frequency fluctuations efficiently while maintaining a strong voltage reference for the converter.

Figure 5. Drive current required by ADC's reference input

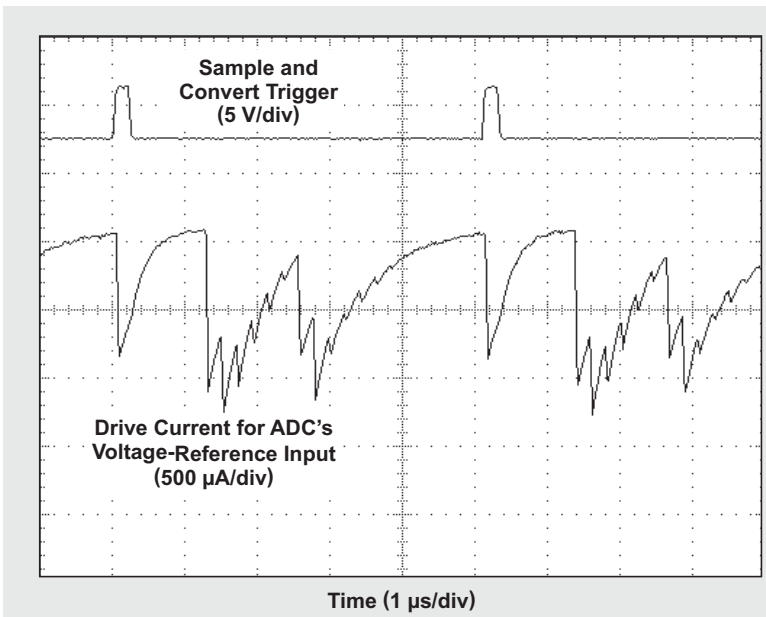


Figure 6. Voltage-reference circuit with added buffer and output filter

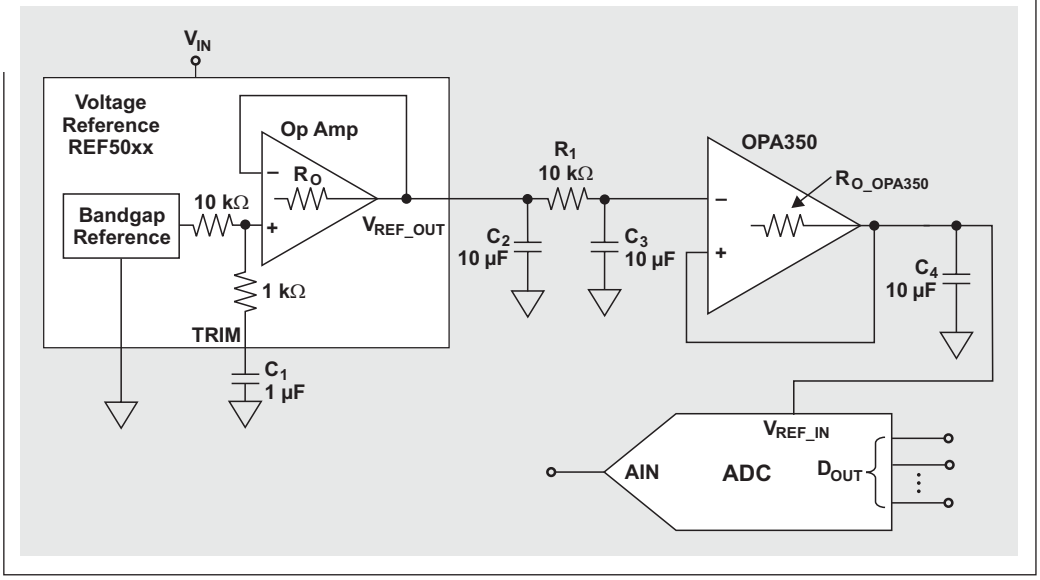


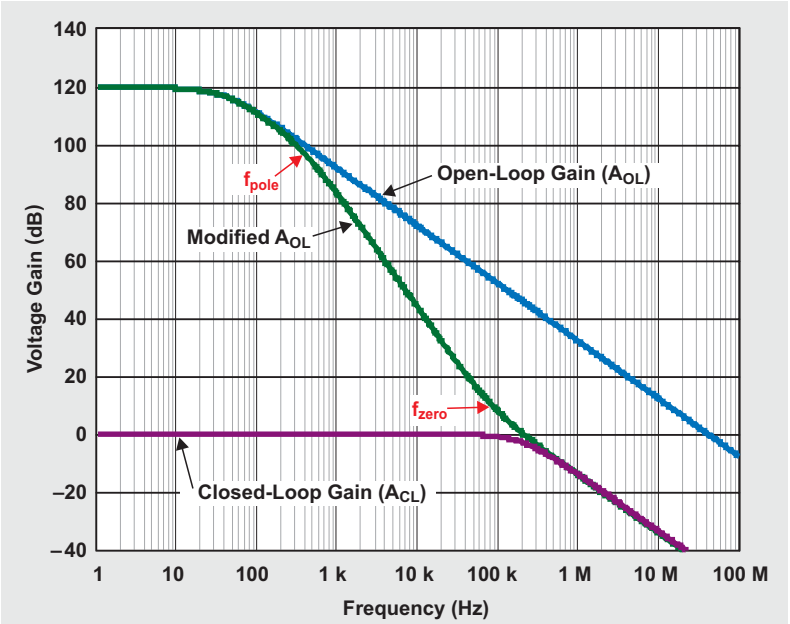
Figure 6 shows a voltage-reference circuit that will adequately drive a high-resolution ADC. In this circuit, the TI OPA350 is placed as a buffer after the low-pass filter that was constructed with R_1 and C_3 for the circuit in Figure 3. The OPA350 drives a 10-µF filter capacitor (C_4) and the voltage-reference input pin of the ADC. The noise measured at the output of the OPA350 in Figure 6 is 4.5 μV_{RMS} or 42 μV_{PP}. The input bias current of the OPA350 is 10 pA at 25°C. This current, in combination with the current through R_1, generates a 100-nV, constant-DC drop. Note that this voltage drop does not change with the ADC's bit decisions. It is true that the input bias current of the OPA350 changes over temperature, but a maximum current that is no more than 10 nA at 125°C can be expected. This value generates a change of 100 µV over a temperature range of 100°C.

It is useful to put the voltage drop across R_1 into perspective. This voltage drop is added to the errors contributed by the REF50xx and the OPA350. The initial error of the REF50xx output is ±0.05%, with an error over temperature of 3 ppm/°C. With a 4.096-V reference (REF5040), the initial reference error is equal to 2.05 mV at room temperature and an additional 1.23 mV at 125°C. Therefore, the reference output error is significantly larger than the errors produced by R_1 and variations in the OPA350's offset and input bias current.

Amplifier stability

There is a final word of caution about the circuit in Figure 6. The stability of the OPA350 can be compromised if C_4 and the OPA350's open-loop output resistance (R_{O_OPA350}) modify the open-loop voltage-gain (A_{OL}) curve to create a marginally stable state. To illustrate this phenomenon, Figure 7 shows how the output capacitor (C_4), with a 0.2-Ω ESR and the OPA350's open-loop output resistance (43 Ω), modifies the OPA350's A_{OL} curve. These curves can be used to quickly determine the stability of the circuit. A circuit with good stability would basically be one where the rate of closure of the operational amplifier's modified A_{OL} curve and closed-loop voltage-gain (A_{CL}) curve is

Figure 7. Frequency response of buffer with an RC load



20 dB/decade. This rule of thumb is presented in Reference 4. The open-loop output resistance of the OPA350 is 43 Ω, and the ESR of C_4 (R_{ESR_C4}) is 200 mΩ. The frequency locations of the pole and zero that are created by these values are

$$f_{pole} = \frac{1}{2\times\pi\times(R_{O\_OPA350} + R_{ESR\_C4})\times C_4} = 368 \text{ Hz and}$$

$$f_{zero} = \frac{1}{2\times\pi\times R_{ESR\_C4}\times C_4} = 79.6 \text{ kHz.}$$

Per Figure 7, the circuit in Figure 6 is stable.

Thinking ahead

Unfortunately, the voltage-reference designs in this article can degrade ADC performance by adding unwanted temperature drift and initial gain error. Higher-performance systems with 21+ bits may require a voltage-reference design that addresses these issues. Future articles will explore a new approach with auto-zero amplifiers that will compensate for these errors.

References

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Document Title	TI Lit. #
1. Bonnie Baker and Miro Oljaca, "How the Voltage Reference Affects ADC Performance, Part 1," *Analog Applications Journal* (2Q 2009)	slyt331
2. Miro Oljaca and Bonnie Baker, "How the Voltage Reference Affects ADC Performance, Part 2," *Analog Applications Journal* (3Q 2009)	slyt339
3. Bonnie Baker, "A Glossary of Analog-to-Digital Specifications and Performance Characteristics," Application Report	sbaa147
4. Tim Green. Operational amplifier stability, Parts 3, 6, and 7. *EN-Genius Network: analogZONE: acquisitionZONE* [Online]. Available: http://www.en-genius.net/includes/files/acqt_*000000*.pdf (Replace "*000000*" with "030705" for Part 3, "070405" for Part 6, or "052906" for Part 7.)	—
5. Bonnie C. Baker and Miro Oljaca. (2007, June 7). External components improve SAR-ADC accuracy. *EDN* [Online]. Available: http://www.edn.com/contents/images/6447231.pdf	—
6. Wm. P. (Bill) Klein, Miro Oljaca, and Pete Goad. (2007). Improved voltage reference circuits maximize converter performance. Analog eLab™ Webinar [Online]. Available: http://dataconverter.ti.com (Scroll down to "Videos" under "Analog eLab™ Design Support" and select webinar title.)	—
7. Art Kay. Analysis and measurement of intrinsic noise in op amp circuits, Part I. *EN-Genius Network: analogZONE: audiovideoZONE* [Online]. Available: http://www.en-genius.net/includes/files/avt_090406.pdf	—

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Using power solutions to extend battery life in MSP430 applications

By Michael Day
Applications Manager, Portable Power Products

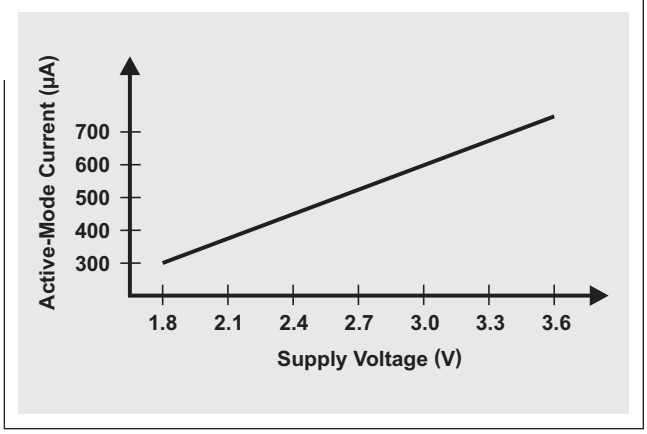
The MSP430 is the lowest-power microprocessor available in the market. Its inherently low-power operation is ideal for battery-powered applications where frequent battery replacement is undesirable. This article shows two simple but effective power solutions that further minimize MSP430 power consumption and extend battery life.

In an attempt to prolong battery life, software engineers go to great lengths to optimize code, minimize memory accesses, etc. Hardware engineers focus on ways to shut down unused circuitry, ensure that all quiescent currents and leakage paths are minimized, and maximize power-supply efficiency.

In most cases, engineers eliminate any DC/DC conversion altogether if the system's source voltage falls within the MSP430's input operating range. Many MSP430 designs do not need an input power supply because the MSP430 device family accepts extremely wide variations in input voltage. For example, the MSP430FG4618 operates with an input voltage of between 1.8 V and 3.6 V. Because of this wide input range, many MSP430 designs operate directly from a battery without additional power conversion. Examples of input sources that do not need power conversion are dual alkaline, nickel metal hydride, and nickel cadmium batteries, as well as primary lithium-ion coin cells.

An often overlooked technique for extending battery life is to add an input power supply, even if it is otherwise not needed. Adding a power supply between the input-voltage source and the MSP430 to increase battery life is contradictory to conventional thinking. This is because of two things that all power supplies have in common: They have quiescent current (I_q) at no load that sinks current from the battery to ground; and they have less than 100% efficiency, which dissipates power in the power supply. Even power supplies optimized for low-power and battery-powered applications have less than 100% efficiency, with quiescent currents that continually drain battery capacity. Typical power-supply efficiencies for an MSP430 application operating at 3.0 V from two AA batteries is 85 to 92%. Typical I_q values range from 15 to 50 µA. Conventional thinking says that removing this power supply and operating the application directly from the battery will extend battery life by an additional 8 to 15% because the effective efficiency will then be 100%.

Figure 1. MSP430FG4618's supply current versus its supply voltage



MSP430 supply current varies linearly with input voltage, so operating the system with lower voltages reduces both MSP430 input current and overall power consumption. Figure 1 shows the variation in the MSP430FG4618's 1-MHz active-mode supply current (I_{AM}) versus its supply voltage.

Operating at the lowest required input voltage minimizes battery current, but this requires the insertion of a power supply. Regardless of topology, this power supply will be less than 100% efficient. A common design scenario is an MSP430 operating from two series-connected AA alkaline batteries that supply 3.2 V when new and 1.8 V when discharged. The designer must choose between two power-system topologies. The first is to operate directly from the battery voltage, which results in a higher MSP430 input current. The second is to insert a power supply between the battery and the MSP430. After considering the power supply's efficiency and quiescent current, many designers quickly choose to operate directly from the input source. Few designers are aware that adding a power supply can actually provide significant improvements in battery life, even with efficiency and quiescent-current concerns.

Designers must deviate from conventional thinking that efficiency is the most important figure of merit in a power system. In a battery-powered system, battery current drain is the main concern. The examples in Figure 2 help make this point. System 1 in Figure 2a operates directly from two AA alkaline batteries. An equivalent power supply in this example has 100% efficiency and 0-µA quiescent current. All power delivered from the battery is available to the MSP430. For System 2 in Figure 2b, a TPS780xx LDO has been inserted. The LDO's efficiency is defined by V_{OUT}/V_{IN}, which averages to approximately 90% over the entire voltage range of the batteries. The LDO also draws 500 nA of quiescent current from the battery. When only efficiency and quiescent current are considered, System 1 clearly wins. However, System 2 draws less current from the batteries, which extends the system's operating time.

Figure 3 compares the two systems' battery currents. When the battery voltage is above 2.2 V, System 1 consumes more battery current because the MSP430 operating current is a linear function of input voltage. System 2 consumes a constant current because the LDO maintains a constant 2.2 V at the MSP430. As the battery voltage drops to 2.2 V and below, the two MSP430s consume the same current. System 2 consumes an additional 500 nA due to the TPS780xx's quiescent current (I_q). When the input voltage is above 2.2 V, System 2's reduced battery current results in longer system run time.

Two lab experiments were conducted with an MSP430FG4618 operating at 5 MHz while powered by two AAA alkaline batteries. These experiments were set up to correspond with the two systems in the previous example. In this second example, System 1, with the MSP430 powered directly from the batteries, operated for 223 hours before shutting down. System 2, which used a TPS780xx to drop the MSP430 operating voltage to 2.2 V, operated for 298 hours before shutting down. The addition of the TPS780xx LDO, which operates at 90% efficiency with these operating conditions, extended battery life by 30%.

An often underutilized method to extend battery life is dynamic voltage scaling (DVS). With DVS, the input supply is reduced if the MSP430 is operated at a lower clock speed or placed into a low-power mode. The examples presented earlier demonstrated that operating with lower input voltages reduces current consumption and extends battery life. For example, an MSP430 system operating with a 7-MHz maximum clock frequency may require the input voltage to be 3.3 V. If the clock speed is reduced to 4.6 MHz, the MSP430 requires only a 2.0-V input voltage. If the MSP430 is placed into low-power mode, the required input voltage is only 1.8 V.

Figure 2. Two alkaline-system configurations

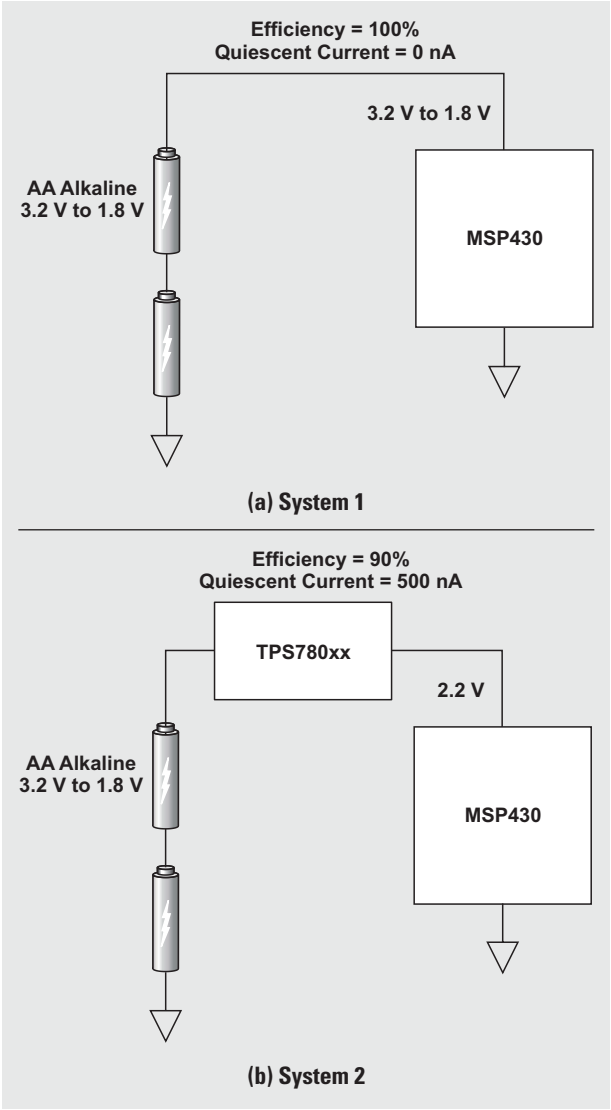


Figure 3. MSP430's operating current versus battery voltage

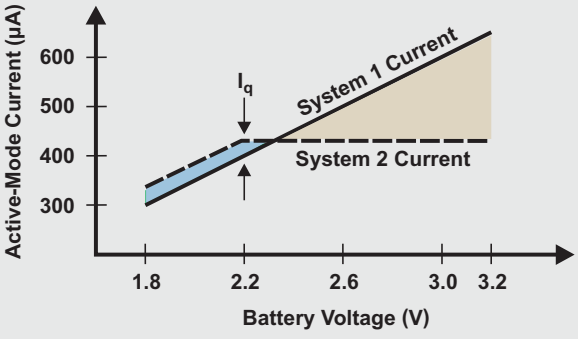


Figure 4 shows a battery-powered system that uses the TPS780xx to implement DVS to save battery power. The TPS780xx, which is an LDO with an ultralow quiescent current of 500 nA, contains a digital input (V_{SET}) that connects directly to the MSP430. The MSP430 pulls this pin high to set V_{OUT} at 2.2 V and pulls it low to set V_{OUT} at 3.3 V. This configuration allows the MSP430 to adjust its input voltage as its operating conditions change.

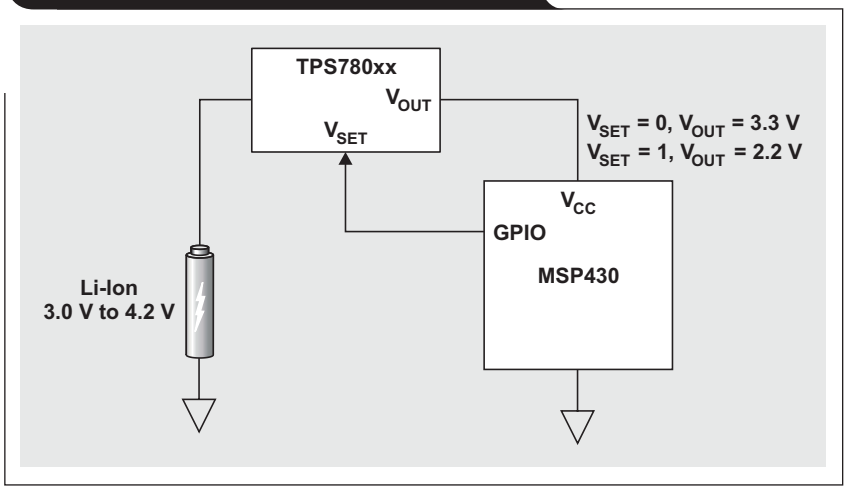
Even if the MSP430 is operated only at 7 MHz when active and placed into low-power mode when not active, DVS can significantly extend battery life. In low-power mode 3 (LPM3), the MSP430FG4618's operating currents at inputs of 3.3 V and 2.2 V are 2.13 µA and 1.3 µA, respectively. With the TPS780xx's 0.5-µA quiescent current added, the battery currents are 2.63 µA and 1.8 µA, respectively. DVS reduces battery current by 26% under these conditions. This reduction of LPM3 battery current is critical for systems that spend a significant amount of time in sleep mode.

When designing an MSP430 power system, an engineer should pay close attention to selecting the proper operating voltage. Minimizing the nominal operating voltage and implementing DVS when possible will provide significant improvements in a system's run time.

Related Web sites

power.ti.com
www.ti.com/msp430
www.ti.com/sc/device/MSP430FG4618
www.ti.com/sc/device/TPS78001

Figure 4. MSP430 with DVS implemented



Designing a multichemistry battery charger

By Keith Keller
Analog Field Applications/Power Management

The challenge

Designing a battery charger for nickel, lithium-ion (Li-ion) and lead-acid cells requires special considerations for proper charging and safety. A comprehensive charging algorithm must be created that is dependent on the chemistry that needs to be supported. The easiest way to accomplish this type of design is to use an integrated, flexible multichemistry battery charger in conjunction with a microprocessor. The microprocessor is used to identify the battery chemistry and adjust for proper charging conditions, including termination criteria. It also monitors operating conditions for safety.

Charging methods for different battery chemistries

There are fundamental differences in how cells of different chemistries are charged. Nickel-metal-hydride (NiMH) cells require constant current throughout the charging cycle. Li-ion cells require constant current followed by a constant voltage based on their maximum-rated individual voltage. Lead-acid cells also require a constant current followed by a constant-voltage stage, but a final float-charge stage must be added. Each of these will be discussed in turn.

NiMH cells

The accepted method of determining the full charge of a NiMH cell while it is being charged with a constant current is to monitor for either a voltage droop of approximately 8 to 16 mV or a rapid temperature increase of 10°C. In either case, a charging rate of greater than 0.5C (preferably 1C) is necessary for these conditions to occur. (A "C rate" is defined by the battery's capacity. If a cell is rated at 1500 mAh, then a 1C charging rate will be 1.5 A). In stand-alone chargers where the voltage-droop method is used, care must be taken in the layout to minimize noise on the battery sense line, which could cause a false full-charge indication. To implement constant-current charging with a multichemistry charger, the feedback resistors should be set for a charge-regulation voltage higher than the cells can reach.

Li-ion cells

The maximum-rated individual voltage for lithium-manganese-oxide ($LiMn_2O_4$) and lithium-cobalt-oxide ($LiCoO_2$) cells is typically 4.2 V, and for the newer lithium-iron-phosphate ($LiFePO_4$) cells, 3.7 V. When the maximum-rated voltage is reached, it is held steady and the current is allowed to decrease until the appropriate "taper" point is reached, indicating a fully charged cell. The taper point in stand-alone chargers is typically 1/10 the fast-charge rate. However, with a flexible microcontroller-based architecture, the designer can choose to end charging at any point in the charge cycle. If the design is charging a smart battery with "bypass" cell-balancing circuitry, longer charge times are required because the cell balancing happens only during the end of charge when the voltages are relatively constant and current is tapering.

Lead-acid cells

Like Li-ion cells, lead-acid cells require constant-current charging followed by a constant-voltage stage, but they also need a final float-charge stage. The speed at which lead-acid cells charge is much slower than that of nickel or Li-ion cells. Charging times can range from 12 to 36 hours, depending on the battery capacity. Based on some important trade-offs, the appropriate charging voltage of the individual cells is between 2.3 V and 2.45 V. Charging the cells to a lower voltage maximizes their service life but can lead to sulfation of the negative plate. Charging them to a higher voltage will shorten charging times but can cause the cells to overheat at higher temperatures. For the final float-charge stage, the voltage should be reduced to approximately 2.25 V per cell. There are a few exceptions to these specifications depending on the supplier, so cell datasheets and specifications for proper charging and safety conditions should be carefully studied.

The solution

Fortunately, all aspects of the charging algorithm for any battery chemistry can be implemented with a flexible multichemistry battery charger and a companion microprocessor. For portable applications where a Li-ion or nickel pack could be used interchangeably, other design aspects to consider are proper chemistry identification (ID), detection of pack insertion/removal, charging temperature range, charge thresholds, system monitoring and fault reporting, and loss of input power.

If there is a need to determine pack chemistry, an easy solution is to use an ID resistor on an additional pin that the microcontroller can read via its analog-to-digital converter's input. This setup not only monitors for the ID resistor but can also determine when the battery pack is inserted into the charging cradle. Different-size batteries, such as a double-capacity pack, can also be distinguished.

Cells are typically charged within a temperature window of 0 to 50°C, but this range can be extended if the cells are charged at a slower rate and a lower voltage. In extremely high ambient temperatures, active discharge of Li-ion cells to anywhere from 3.7 to 3.9 V per cell can also be considered. In all cases, high temperatures shorten battery life.

After determining the chemistry ID and an acceptable temperature range, the charger must determine if the cells are undervoltage (indicating a deeply depleted state) and therefore need to be charged slowly, typically at 1/10 the fast-charge rate. For nickel cells, the undervoltage safety threshold is considered to be 0.9 V or less per cell; for standard lithium cells, less than 3.0 V per cell; and for the newer $LiFePO_4$ cells, as low as 1.5 V. During trickle charge, if the cell's voltage does not increase above these safety thresholds within 30 minutes, the cell is deemed to be damaged, and charging stops.

After all these safety checks are complete, the batteries are deemed good, and the fast-charge mode begins. Throughout the charging process, the temperature, charge current, and battery voltage must be continuously monitored. Three arrays of values should be stored for each of these measurements. Each data point can be taken approximately every 100 ms, and an average of the values can be used for calculations. A watchdog safety timer is a good idea to protect against any unforeseen coding errors that could cause the microprocessor to enter an unknown state. Specific fault conditions can be stored as unique bits in a fault register that the system can read through interrogating the microprocessor or that can be indicated to the user through LEDs or a display. Finally, the charging algorithm should be designed so that if there is a loss of input power or the battery pack is removed and inserted, the whole identification and charging process will start again.

Texas Instruments (TI) offers several multichemistry battery ICs to meet different requirements for charger design. For example, the bq24703 multichemistry charger, along with an MSP430F2012 ultralow-power microcontroller, is used in the PMP3914 evaluation module to detect and charge either a NiMH or a Li-ion battery pack. Also included in the design is a 75-W off-line converter, with an input voltage of 108 to 132 V and an output voltage of 25 V, that uses TI's UCC28600 green-mode quasiresonant flyback PWM controller.

The bq24703 is a nonsynchronous charger with a high-side pFET control, which makes it ideal for charging a high-voltage (21-V) 5s2p Li-ion battery pack or a 25-V 15s1p NiMH battery pack. The letter "s" indicates how many cells are connected in a series string to achieve the desired pack voltage. The letter "p" indicates how many strings of cells are connected in parallel to achieve the desired pack capacity. With a nonsynchronous charger, the charge current is limited to around 3 A. Several other multichemistry chargers from TI, such as the bq24704 or bq24750A, are synchronous buck converters that can support 10 A or more of continuous-charge current.

Conclusion

Creating a multichemistry battery charger requires knowledge of individual cell characteristics and overall safety considerations. This article discussed differences between charging Li-ion, nickel, and lead-acid batteries and outlined how a charging algorithm can be implemented for a multichemistry charger and a microcontroller. Safety considerations were also discussed, including system monitoring for under- and overvoltage conditions, overcharging, and extreme temperatures.

Related Web sites

power.ti.com

PMP3914 Evaluation Module User's Guide:
www-s.ti.com/sc/techlit/sluu369

www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq24703, bq24704, bq24750A, MSP430F2012, or UCC28600

Efficiency of synchronous versus nonsynchronous buck converters

By Rich Nowakowski, *Power Management Product Marketing*
and Ning Tang, *Systems Engineer, SWIFT DC/DC Converters*

Choosing the right DC/DC converter for an application can be a daunting challenge. Not only are there many available on the market, the designer has a myriad of trade-offs to consider. Typical power-supply issues are size, efficiency, cost, temperature, accuracy, and transient response. The need to meet ENERGY STAR® specifications or green-mode criteria has made energy efficiency a growing concern. Designers want to improve efficiency without increasing cost, especially in a high-volume consumer electronics application where reducing power consumption by one watt can save megawatts from the grid. The semiconductor industry has recently developed low-cost DC/DC converters that employ synchronous rectification and that are thought to be more efficient than nonsynchronous DC/DC converters. This article will compare the efficiency, size, and cost trade-offs of synchronous and nonsynchronous converters used in consumer electronics under various operating conditions. It will be shown that synchronous buck converters are not always more efficient.

Typical application

To demonstrate the subtle differences between the two converter topologies, a typical point-of-load application was chosen. Many low-cost consumer applications use a 12-V rail that accepts power from an unregulated wall adapter or an off-line power supply. Output voltages usually range from 1 to 3.3 V, with output currents under 3 A. The Texas Instruments devices in Table 1 were chosen to compare actual efficiency measurements under various output-current and output-voltage conditions. The rated output current, which is the level of output current each device is marketed to deliver, was taken directly from the data sheets (see References 1 and 2).

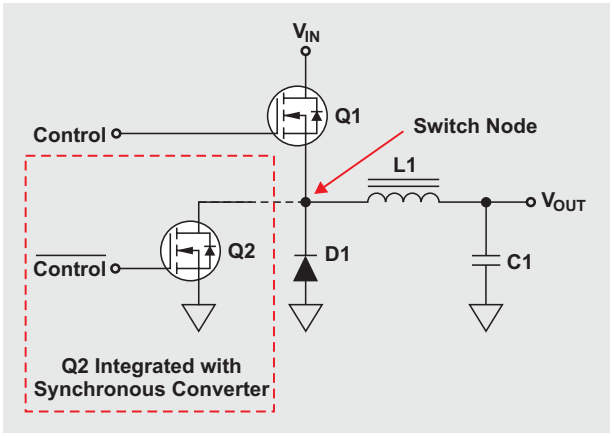
Table 1. Device comparison

PART NUMBER	TOPOLOGY	INPUT VOLTAGE RANGE (V)	RATED I_{OUT} (A)
TPS54325	Synchronous buck	4.5 to 18	3
TPS54331	Nonsynchronous buck	4.5 to 28	3

Basic operation

A typical block diagram for a step-down (buck) regulator is shown in Figure 1. The main components are Q1, which is the high-side power MOSFET; L1, the power inductor; and C1, the output capacitor. For a synchronous-buck topology, a low-side MOSFET (Q2) is used. In a nonsynchronous-buck topology, a power diode (D1) is used. In a synchronous converter, such as the TPS54325, the low-side power MOSFET is integrated into the device. The main advantage of a synchronous rectifier is that the voltage drop across the low-side MOSFET can be lower than the voltage drop across the power diode of the nonsynchronous converter. If there is no change in current level, a lower voltage drop translates into less power dissipation and higher efficiency.

Figure 1. Synchronous and nonsynchronous buck circuits



Choosing the power diode

Nonsynchronous converters are designed to operate with an external power diode (D1). The three key specifications a designer needs to consider when choosing a power diode are the reverse voltage, the forward voltage drop, and the forward current. First, the rated reverse voltage must be at least 2 V higher than the maximum voltage at the switch node. Second, the forward voltage drop should be small for higher efficiency. Third, the peak-current rating must be greater than the maximum output current plus one-half the peak-to-peak inductor current. When the duty cycle is low (i.e., at low output voltages), D1 operates as a catch diode that conducts more current than the high-side MOSFET. A fourth consideration is to make sure the package of the diode chosen can handle the power dissipation. The diode chosen for the TPS54331 was the B340A, which has a reverse voltage rating of 40 V, a forward voltage drop of 0.5 V, and a forward current rating of 3 A.

The TPS54325 does not need a power diode, since a 70-mΩ low-side MOSFET is integrated into the chip. The integrated MOSFET saves space; but the complexity of the control circuitry must be increased to ensure that both MOSFETs do not conduct simultaneously, which would result in a direct path from the input to ground. Any cross conduction would result in lower efficiency and could even overload and damage the system.

Efficiency calculations

To calculate the efficiency of a DC/DC converter, the total power dissipation needs to be computed. The key contributors to the power dissipation for a DC/DC converter in continuous conduction mode (CCM) are the high- and low-side switching losses and the IC's quiescent-current loss. The formulas for these losses are as follows:

$$P_{Conduction\_HS} = I_{OUT}^2 \times R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$P_{SW} = V_{IN} \times V_{OUT} \times 0.5(t_{Rise} + t_{Fall}) \times f_{SW} \quad (2)$$

$$P_{Quiescent} = V_{IN} \times I_q \quad (3)$$

Equations 1 through 3 apply to both the synchronous and the nonsynchronous converter in CCM. However, the losses in the low-side MOSFET for the synchronous buck converter (Equation 4) and in the low-side power diode (P_{D1}) for the nonsynchronous buck converter (Equation 5) need to be included:

$$P_{Conduction\_LS} = \underbrace{\left[I_{OUT}^2 \times R_{DS(on)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]}_{\text{Low-Side MOSFET}} + \underbrace{(2 \times t_{Delay} \times f_{SW} \times I_{OUT} \times V_{Fwd})}_{\text{Body Diode}} \quad (4)$$

$$P_{D1} = V_{D1\_Fwd} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

In Equation 4, the first component represents the conduction loss in the low-side MOSFET, and the second component represents the conduction loss in the body diode. The current flowing through the body diode is about an order of magnitude lower than the current flowing through the low-side MOSFET and is negligible at 2 A.

These equations make it evident that there are several factors influencing full-load efficiency, such as the drain-to-source resistance, drain-to-source forward voltage, duty cycle, frequency, and power MOSFET rise and fall times. The AC and DC losses of the inductor and the equivalent series resistance of the output capacitance are similar in the application, since the same LC filter can be used for both devices. For a DC/DC converter, the duty cycle is given, and only the drain-to-source resistance, forward voltage drop, and switching frequency can be chosen. Typically, the MOSFET rise and fall times are not stated in the data sheet but are important specifications to consider, since the faster they are, the less power is dissipated. The trade-off is noisy ringing at the switch node when a power MOSFET is turned on too quickly. Start-up time can be reduced to improve thermal performance so that a less costly package can be chosen to house the smaller power MOSFET with a higher drain-to-source resistance.

Efficiency results at high loads

Two circuits were built with the devices shown in Table 2 so that the efficiencies of the circuits could be compared. The devices used the same LC filter in the bill of materials. Even though the two devices had slightly different fixed switching frequencies, there was not enough impact on circuit efficiency to alter the conclusion of this demonstration. An input voltage of 12 V was chosen, and efficiency measurements were taken by simply varying the output voltages.

Table 2. Basic device characteristics

PART NUMBER	HIGH-SIDE $R_{DS(on)}$ (mΩ)	LOW-SIDE $R_{DS(on)}$ (mΩ)	FREQUENCY (kHz)
TPS54325	120	70	700
TPS54331	80	N/A (V_{D1_Fwd} = 0.5 V)	570

Figure 2 shows the efficiency of both devices with a 12-V input and a 1.5-V output. The figure clearly shows that the TPS54325 had higher efficiency at full load. Since the duty cycle was 12.5%, the power diode of the nonsynchronous solution with the forward voltage drop of 0.5 V dissipated more energy than the 70-mΩ MOSFET, despite the TPS54325's high-side drain-to-source resistance.

Figure 3 shows the efficiency of both devices with a 12-V input and a 2.5-V output. It is evident that the efficiency of the TPS54331 improved dramatically. In this case, the duty cycle was 21%, and the two full-load efficiencies were nearly the same. The power diode of the nonsynchronous device conducted less often, and the high-side MOSFET with low ON resistance conducted more often. When the dissipation of the low-side power diode was lower at higher duty cycles, the nonsynchronous solution became more efficient.

Figure 2. Device efficiencies with 12-V input and 1.5-V output

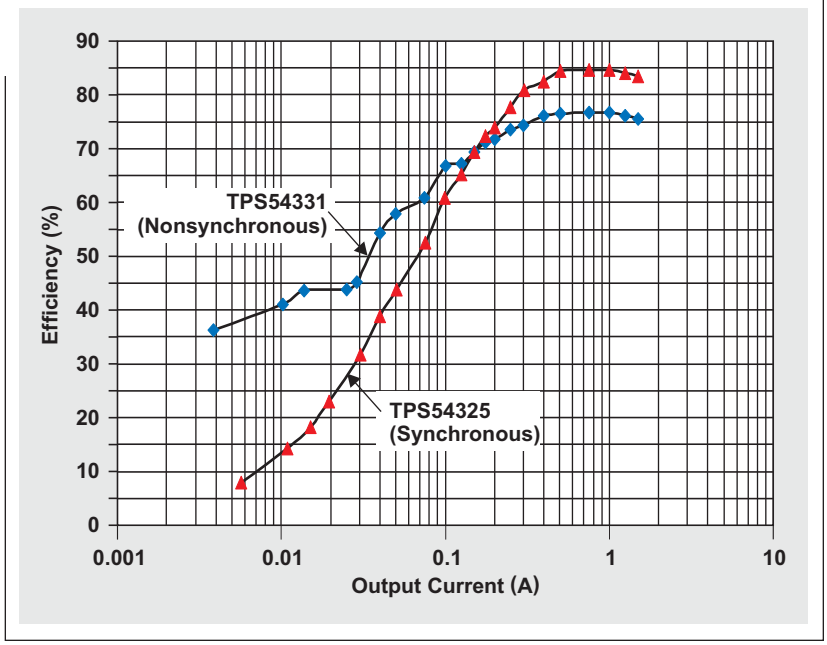


Figure 3. Device efficiencies with 12-V input and 2.5-V output

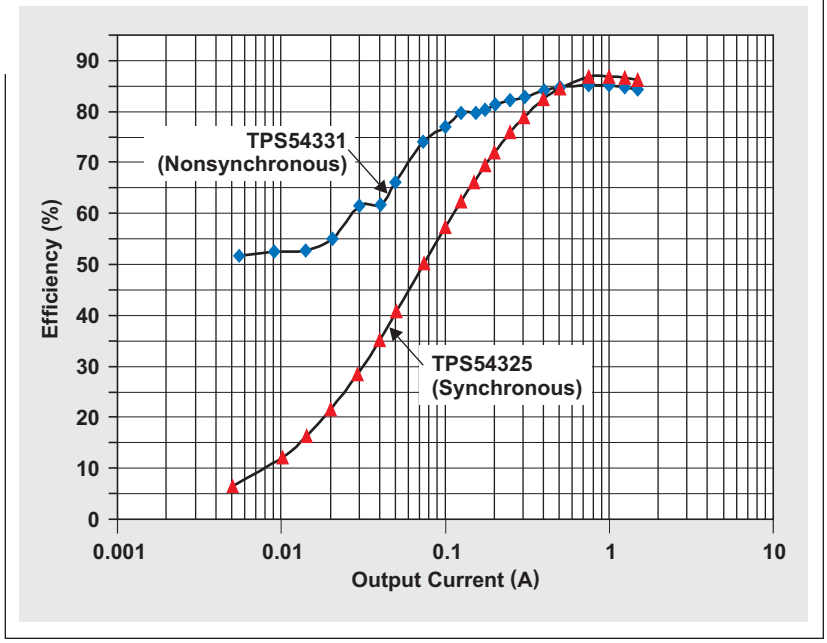
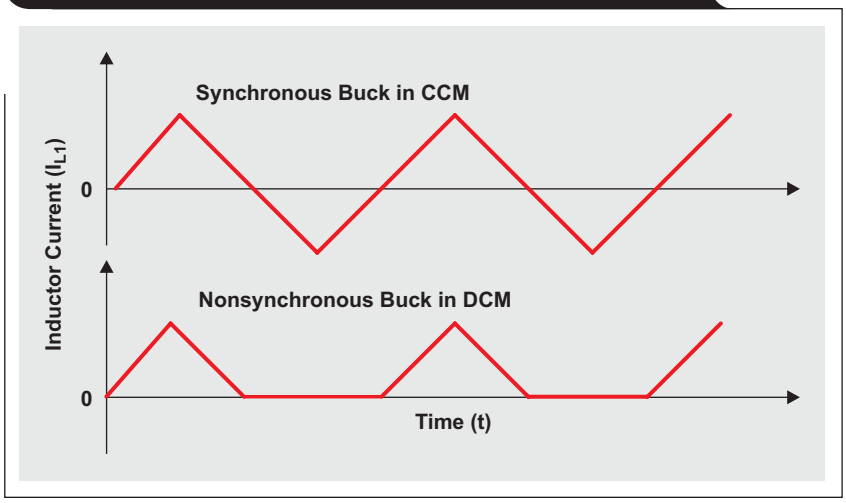


Figure 4. Inductor-current waveforms in CCM and DCM



Considerations for light-load efficiency

In some applications, the need for light-load efficiency outweighs the need for higher full-load efficiency. Nonsynchronous buck converters switch in discontinuous conduction mode (DCM) at light loads. In the nonsynchronous buck converter, the inductor current flows in only one direction. With the synchronous buck converter, current is allowed to flow in both directions, and power is dissipated when reverse current flows. Figure 4 illustrates the difference between inductor-current waveforms generated in CCM versus those generated in DCM.

The TPS54331 has a pulse-skipping feature called Eco-mode™ that improves light-load efficiency. This mode of operation turns on the power MOSFET less often, resulting in lower switching losses. The differences in light-load efficiency shown in Figures 2 and 3 are due to the TPS54331's Eco-mode feature and its low operating quiescent current. For more information on Eco-mode, please see Reference 1.

Cost and space considerations

A synchronous converter with an integrated low-side MOSFET offers benefits such as reduced size, lower parts count, and easier design. However, if reducing cost is the main objective, a nonsynchronous converter with an external power diode may be less expensive than a synchronous buck converter.

Conclusion

Synchronous buck converters have become very popular recently and are widely available. However, they are not always more efficient. Nonsynchronous buck converters may have adequate efficiency at higher duty cycles and lighter loads. By paying attention to the data-sheet specifications, especially the drain-to-source resistance and the quiescent current, the designer can make the best choice based on the goals of a specific design.

References

For more information related to this article, you can download an Acrobat® Reader® file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "4.5-V to 18-V, 3-A Output Synchronous Step Down Switcher with Integrated FET (SWIFT™)," TPS54325 Data Sheet	slvs932a
2. "3A, 28V Input, Step Down SWIFT™ DC/DC Converter with Eco-mode™," TPS54331 Data Sheet	slvs839b

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS54325
www.ti.com/sc/device/TPS54331

Using fully differential op amps as attenuators, Part 3: Single-ended unipolar input signals

By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Fully differential operational amplifiers (FDAs) can easily be used to attenuate and level-shift high-voltage input signals to match the input requirements of lower-voltage ADCs. This article is Part 3 of a three-part series. In Part 1 (see Reference 2) we considered a balanced, differential bipolar input signal and proposed an architecture utilizing an FDA to accomplish the task. In Part 2 (see Reference 3) we showed how to adapt the circuits presented in Part 1 to a high-voltage, single-ended (SE) bipolar input. In Part 3, we will show how to adapt the circuits presented in Parts 1 and 2 to the more complex case where the input signal is a high-voltage, SE unipolar input with arbitrary common-mode voltage. As mentioned in Part 1, the fundamentals of FDA operation are presented in Reference 1, which provides definitions and derivations.

Single-ended unipolar input

Using an input attenuator

Let's consider a high-amplitude, SE unipolar input signal that needs to be attenuated and level-shifted to the appropriate levels to drive a lower-voltage input ADC. We will use the same basic approach as for the SE bipolar input presented in Part 2; but, to offset the imbalance that would otherwise be caused by the signal's common-mode voltage, we will modify the signal to provide biasing on its alternate input. The proposed input-attenuator circuit for an SE unipolar input signal is shown in Figure 8. R_{S-} and R_{T-} have been added to the circuit in a manner that uses V_{REF} to provide biasing on the alternate input.

The circuit analysis of Figure 8 is very similar to that of Figure 6 in Part 2. For the moment, assume that R_{S-} on the alternate input is grounded instead of tied to V_{REF}. In that case, the only changes in the gain equation are due to changes in reference designators:

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_{T+}}{R_{S+} + R_{T+}} \times \frac{R_F}{R_{G+} + R_{S+} \parallel R_{T+}} \qquad (7)$$

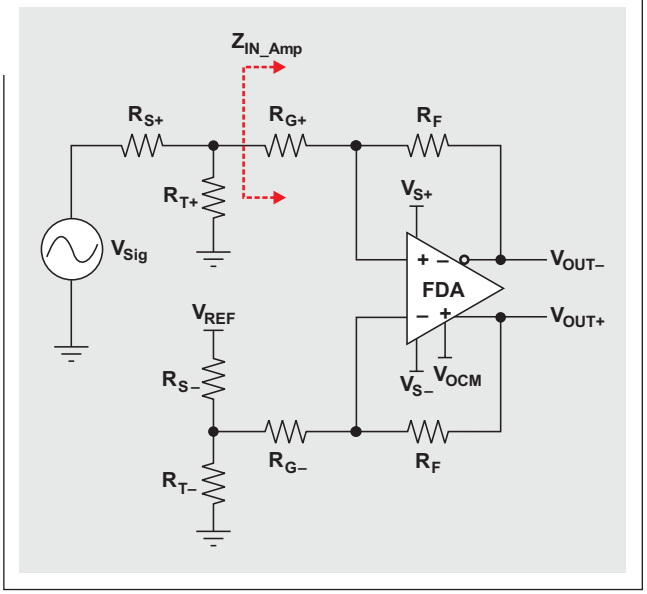
The noise gain of the FDA can be set to 2 by making the second half of Equation 7 equal to 1:

$$R_{G+} + R_{S+} \parallel R_{T+} = R_F \qquad (8)$$

With this constraint, the overall gain equation reduces to

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_{T+}}{R_{S+} + R_{T+}}. \qquad (9)$$

Figure 8. SE unipolar input-attenuator circuit



If we choose to keep R_F the same on both sides of the FDA, then we need to balance the gain-setting resistances by setting

$$R_{G-} + R_{S-} \parallel R_{T-} = R_{G+} + R_{S+} \parallel R_{T+}. \qquad (10)$$

In order to balance the offset due to the common-mode voltage of V_{Sig}, we multiply the common-mode voltage of V_{Sig} by the signal input attenuator (or voltage divider), which equals V_{REF} times the voltage divider on the alternate input:

$$V_{REF} \frac{R_{T-}}{R_{S-} + R_{T-}} = V_{Sig\_Com} \frac{R_{T+}}{R_{S+} + R_{T+}} \qquad (11)$$

The input impedance is given by $Z_{IN} = R_{S+} + R_{T+} \parallel Z_{IN\_Amp}$, which is approximated by $Z_{IN} = R_{S+} + R_{T+} \parallel R_{G+}$.

These basic design equations provide the freedom to choose one value in each of the following sets of interactive components:

1. Signal input-attenuator resistors, R_{S+} and R_{T+}
2. Gain-setting resistors, R_F and $R_{G\pm}$
3. V_{REF} voltage-divider resistors, R_{S-} and R_{T-}

We start the design as before by first choosing R_{S+} close to the desired input impedance. We then select R_F in the

recommended range for the device and calculate the value of R_{T+} required to provide the desired attenuation. The result can be used to calculate R_{G+}.

For the alternate side of the input signal, we start similarly by first choosing the value of R_{S-}, which will basically set the current in the voltage divider. It is generally best to keep the current small to conserve power; but, since we chose to keep R_F the same on both sides of the FDA, there are limitations because Equation 10 has to be satisfied. The required value of R_{T-} must be calculated to satisfy Equation 11, and then the results can be used along with R_F to calculate R_{G-}.

To see an example Excel® worksheet, go to http://www.ti.com/lit/zip/slyt359 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file FDA_Attenuator_Examples_SE_Unipolar_Input.xls and select the Unipolar SE FDA Input Atten worksheet tab.

Design Example 5

For Example 5, let's say we have a 20-V_{PP} SE unipolar input signal that goes from 0 V to +20 V, we need a 1-kΩ input impedance, and we want to use the ADS8321 SAR ADC with a 5-V_{PP} differential input and a 2.5-V common-mode voltage. We also are using a +5-V single supply to power both the FDA and the ADC, so we want to use that as our reference voltage, V_{REF}, on the alternate input. We choose R_{S+} = 1 kΩ and R_F = 1 kΩ. Rearranging Equation 9 and using substitution, we can calculate

$$R_{T+} = \frac{R_{S+}}{\frac{V_{Sig}}{V_{OUT\pm}} - 1} = \frac{1\ k\Omega}{4-1} = 333.3\ \Omega.$$

The nearest standard 1% value, 332 Ω, should be used.

Rearranging Equation 8 and using substitution, we can calculate

$$R_{G+} = R_F - R_{S+} \parallel R_{T+} = 1\ k\Omega - 1\ k\Omega \parallel 332\ \Omega = 750\ \Omega,$$

which is a standard 1% value. We then choose R_{S-} = 1 kΩ and calculate R_{T-} by rearranging Equation 11 and using substitution:

$$R_{T-} = \frac{R_{S-}}{\frac{1}{\frac{V_{Sig\_Com}}{V_{REF}} \times \frac{R_{T+}}{R_{S+} + R_{T+}}} - 1}$$

$$= \frac{1\ k\Omega}{\frac{1}{\frac{10\ V}{5\ V} \times \frac{332\ \Omega}{1\ k\Omega + 332\ \Omega}} - 1} = 1\ k\Omega,$$

which is a standard 1% value. By rearranging Equation 10 and using substitution, we can calculate

$$R_{G-} = R_{G+} + R_{S+} \parallel R_{T+} - R_{S-} \parallel R_{T-}$$
$$= 750\ \Omega + 1\ k\Omega \parallel 332\ \Omega - 1\ k\Omega \parallel 1\ k\Omega = 500\ \Omega.$$

The nearest standard 1% value, 499 Ω, should be used. These values will provide the needed function and keep the FDA stable. Again the V_{OCM} input on the FDA is used to set the output common-mode voltage to 2.5 V.

The input impedance is Z_{IN} = 1254 Ω, which is higher than desired. If the input impedance really needs to be closer to 1 kΩ, we can iterate with a lower value as before. In this case, using R_S = 787 Ω and R_F = 1 kΩ will yield Z_{IN} = 999 Ω, which comes as close as is possible when standard 1% values are used.

To see a TINA-TI™ simulation of the circuit in Example 5, go to http://www.ti.com/lit/zip/slyt359 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file FDA_Attenuator_ Examples_SE_Unipolar_Input.TSC to view the example (the top circuit labeled "Example 5"). The simulation waveforms are the same as those shown in Figure 3 of Part 1. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Using an FDA's R_F and R_G as an attenuator

The proposed circuit using gain-setting resistors to obtain an SE unipolar input signal is shown in Figure 9. In this circuit, the FDA is used as an attenuator in a manner similar to that described in Part 2 for the SE bipolar signal, and the design equations are the same:

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_F}{R_G},$$

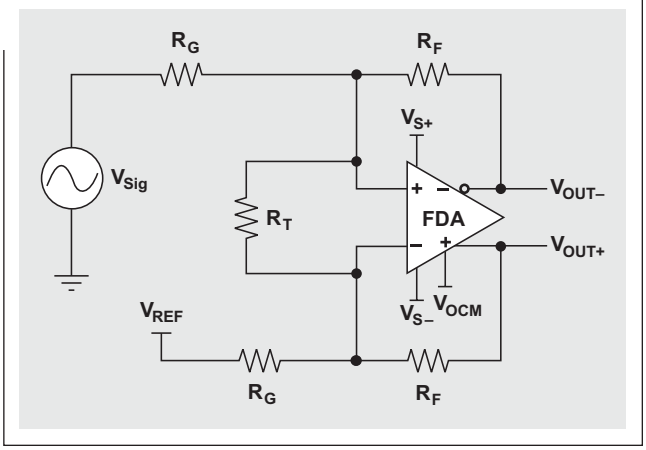
and for stability we set

$$R_F = R_G \parallel \frac{R_T}{2},$$

and $Z_{IN} \approx R_G$.

To avoid a DC offset in the output, V_{REF} is set to equal the common-mode voltage of V_{Sig}. Note that if a reference voltage higher than the input common-mode voltage is available in the system, a resistor divider can be used. This

Figure 9. Using FDA's R_F and R_G as attenuator for SE unipolar input



is accomplished by keeping the parallel combination equal to R_G while simultaneously setting the voltage divider to provide the input common-mode voltage at no load.

Design Examples 6a and 6b

For Example 6a, we will use the same approach as for Example 5, with R_F = 1 kΩ, and calculate R_G = 4 kΩ (the nearest standard 1% value is 4.02 kΩ) and R_T = 2.6666 kΩ (the nearest standard 1% value is 2.67 kΩ). This makes $Z_{IN} \approx$ 4.02 kΩ, and SPICE shows it to be more on the order of 4.46 kΩ. V_{REF} should be set to the common-mode voltage of the input signal and is calculated by

$$V_{REF} = \frac{V_{Sig\_min} + V_{Sig\_max}}{2} = \frac{0\ V + 20\ V}{2} = 10\ V.$$

The function is the same as before, but with this approach the only freedom of choice given the design requirements is the value of R_F.

To see an example Excel worksheet, go to http://www.ti.com/lit/zip/slyt359 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). Then open the file FDA_Attenuator_Examples_SE_Unipolar_Input.xls and select the Unipolar SE FDA RF_RG Atten worksheet tab. To see a TINA-TI simulation of the circuit in Example 6a, go to http://www.ti.com/lit/zip/slyt359 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file FDA_Attenuator_Examples_SE_Unipolar_Input.TSC to view the example (the middle circuit labeled "Example 6a"). To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

The simulation waveforms for Example 6a show that the signal is distorted. Further investigation will show that the input common-mode voltage range of the THS4509 used in the simulation has been violated at the most positive peaks of the input signal, causing nonlinear operation. In this case the SPICE model shows a problem; but care must be taken to double-check operation against the data sheet, as not all SPICE models will show this error. For instance, replacing the THS4509 model with the THS4520 will simulate fine, but the actual device has a similar input common-mode voltage range.

One way to correct the problem is to use pull-down resistors from the FDA input pins to ground as described in the THS4509 data sheet. In this case, instead of placing the full-value R_T across the inputs, we place half the value (1.33 kΩ) from each input to ground. These resistors will act to pull down the inputs and bring the common-mode voltage back into linear operation. To see a TINA-TI simulation of this corrected circuit (Example 6b), go to http://www.ti.com/lit/zip/slyt359 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file FDA_Attenuator_Examples_SE_Unipolar_Input.TSC to view the example (the bottom circuit labeled "Example 6b"). Note that the circuit provides the same results as those shown in Figure 3 of Part 1. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Another way to eliminate the problem with input common-mode voltage is to use the input attenuator to the FDA as the circuit's attenuator as described earlier.

Conclusion

We have analyzed two approaches that attenuate and level-shift high-amplitude, SE unipolar signals to the input range of lower-voltage input ADCs. The primary difference between the unipolar input design and the bipolar designs described in Parts 1 and 2 is that a reference voltage to the alternate input must be provided in the unipolar design to make sure the output swing is symmetrical about the common-mode voltage. For the first approach (Example 5), we chose input resistor values to provide the required attenuation and to keep the noise gain of the FDA equal to 2 for stability. This approach allows the use of a lower value for V_{REF}. The second approach (Example 6a) uses the gain-setting resistors of the FDA in much the same way as using an inverting op amp, then a resistor is bootstrapped across the inputs to provide a noise gain of 2. We saw in the simulation that this last approach caused a problem with the input common-mode voltage going too high on the positive peaks of the input signal, but this was easily compensated for by splitting the R_T resistor and tying the center to ground (Example 6b). The two approaches yield the same voltage translation that is needed to accomplish the interface task. Other performance metrics were not analyzed here, but the two approaches have substantially the same noise, bandwidth, and other AC and DC performance characteristics as long as the value of R_F is the same.

The input-attenuator approach in Example 5 is more complex but allows the input impedance to be adjusted independently from the gain-setting resistors used around the FDA. At least to a certain degree, lower values can easily be achieved if desired, but there is a maximum allowable R_{S+} where larger values require the R_{G+} resistor to be a negative value. For example, setting R_S = 4 kΩ results in R_{G+} = 0 Ω. The spreadsheet tool provided will generate "#NUM!" errors for this input as it tries to calculate the nearest standard value, which then replicates throughout the rest of the cells that require a value for R_{G+}; but this value will work.

The approach in Examples 6a and 6b is easier, but the input impedance is set as a multiplication of the feedback resistor and attenuation: $Z_{IN} \approx 2 \times R_F \times$ Attenuation. This does allow some design flexibility by varying the value of R_F, but the impact on noise, bandwidth, distortion, and other performance characteristics should be considered. Also, as mentioned before, voltages at the amplifier nodes should be checked against data-sheet specifications, because SPICE models will not always show problems.

One final note: The source impedance will affect the input gain or attenuation of either circuit and should be included in the value of R_{S+}, especially if it is significant.

References

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Document Title	**TI Lit. #**
1. Jim Karki, "Fully-Differential Amplifiers," Application Report	sloa054
2. Jim Karki, "Using Fully Differential Op Amps as Attenuators, Part 1: Differential Bipolar Input Signals," *Analog Applications Journal* (2Q 2009)	slyt336
3. Jim Karki, "Using Fully Differential Op Amps as Attenuators, Part 2: Single-Ended Bipolar Input Signals," *Analog Applications Journal* (3Q 2009)	slyt341

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Replace *partnumber* with ADS8321, THS4509, or THS4520

TINA-TI and spreadsheet support files for examples:
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Interfacing op amps to high-speed DACs, Part 2: Current-sourcing DACs

By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

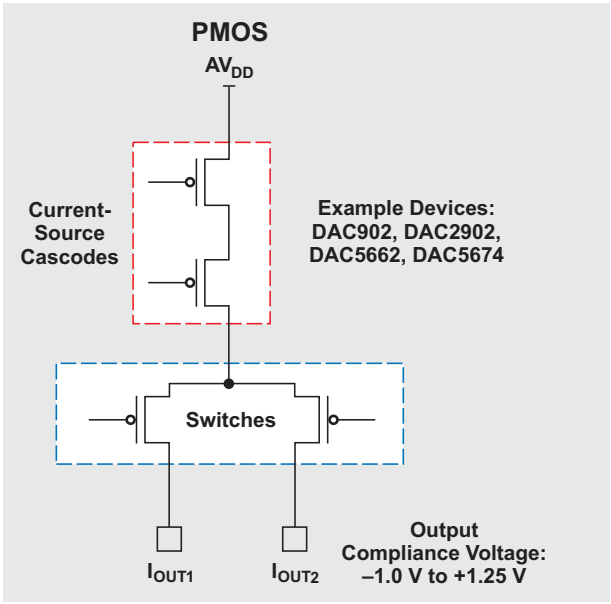
Most high-speed DACs are current-steering DACs that are designed with complementary outputs that either source or sink current. Part 1 (see Reference 1) of this three-part article series discussed the interface between a current-sinking DAC and an op amp. This article, Part 2, discusses the interface between a current-sourcing DAC and an op amp. This interface allows the designer to use the full compliance voltage range of the DAC. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will discuss interfacing a current-sourcing DAC and an op amp by using the more popular configuration that simply terminates to ground. This article series focuses on using high-speed DACs in end equipment that requires DC coupling, like signal generators with frequency bandwidths of up to 100 MHz and a single-ended output. In these cases, high-speed op amps can provide a good solution for converting the complementary-current output from a high-speed DAC to a voltage that can drive the signal output.

It is assumed that the reader is familiar with the operation of complementary-current-steering DACs. If further information is needed, please see Reference 1 for an overview. The design approach for Part 2 is the same as for Part 1, except that a current-sourcing DAC was used to derive the design equations instead of the current-sinking DAC used in Part 1. Because of this, about half of the equations are the same and about half are modified.

Architecture and compliance voltage of current-sourcing DACs

Figure 11 shows a simplified example of a PMOS current source and lists a few devices that use it. The compliance voltage shown is the voltage range at the DAC outputs within which a device will perform as specified. Higher voltages tend to shut down the outputs, and lower voltages have the potential to cause breakdown. Both of these should be avoided to provide the best performance and long term-reliability.

Figure 11. Simplified PMOS current source



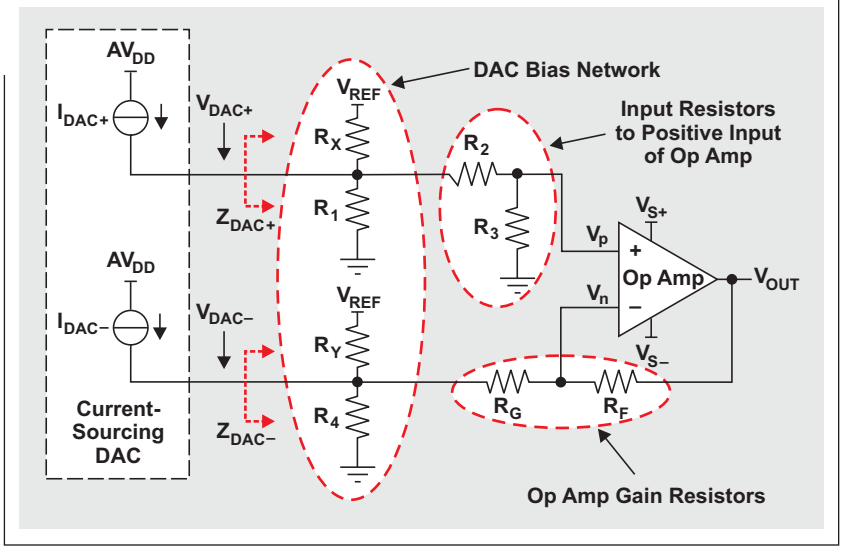
Generally the output is terminated via some impedance to ground. This impedance supplies a current path needed for the array, and the voltage drop across the same impedance can be used as a voltage output. The impedance can be constructed in various ways; it can be a simple resistor divider, a transformer-coupled impedance, or an active circuit like an op amp. This article focuses on the interface to an op amp.

Op amp interface

A proposed op amp interface is shown in Figure 12. This circuit will provide biasing of the DAC outputs, convert the DAC currents to voltages, and provide a single-ended output voltage. The op amp is the active amplifier element for the circuit and is configured as a difference amplifier.

- I_{DAC+} and I_{DAC-} are the current outputs from the DAC.
- R_2 and R_3 are input resistors to the positive input of the op amp.
- R_G and R_F are the main gain-setting resistors for the op amp.
- R_X, R_1, R_Y, and R_4 provide bias and impedance termination for the DAC outputs.
- V_{DAC+} and V_{DAC-} are the voltages at the outputs of the DAC.
- V_p and V_n are the input terminals of the op amp.
- V_{S+} and V_{S-} are the power supplies to the op amp.

Figure 12. Proposed circuit for an op amp interface



Proper component selection will provide the impedance required to maintain voltage compliance with maximum amplitude and balance for the best performance. The analysis of this circuit follows from Part 1 with only minor changes due to the change in polarity of the DAC current (sourcing versus sinking) and the change in compliance voltage range around ground instead of AV_{DD}. The circuit in Figure 12 enables the designer to use the maximum compliance voltage range of the DAC.

The motivation for this interface design is to balance the input voltages to the difference-amplifier circuit to suppress second-order harmonics, and little impact is expected on third-order harmonics. Also, because it allows higher voltage swings at the DAC output than simple termination to ground, the gain of the op amp will be lower given the same output-voltage requirement.

Analysis of positive side

Figure 13 shows the analysis circuit for the positive side. The node equation at the V_{DAC+} output is the same as in Part 1 but with a change in the polarity of I_{DAC+}:

$$\frac{V_{DAC+} - V_{REF}}{R_X} + \frac{V_{DAC+}}{R_1} + \frac{V_{DAC+}}{R_2 + R_3} - I_{DAC+} = 0 \quad \textbf{(20)}$$

The equation for the DAC output impedance stays the same:

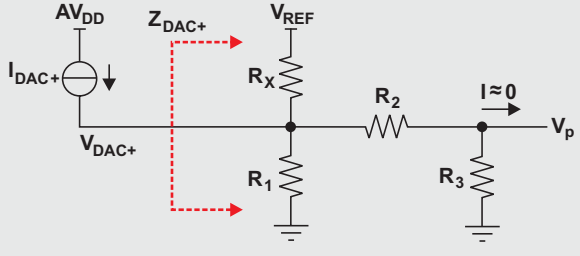
$$Z_{DAC+} = R_X \parallel R_1 \parallel (R_2 + R_3) \quad \textbf{(21)}$$

To solve Equations 20 and 21, which are simultaneous equations with more variables than equations, the designer must choose or identify values based on other design criteria. The following assumptions are made in this article:

1. The DAC output current, I_{DAC+}, and the voltage swing, V_{DAC+}, are defined by the designer to set a target value for Z_{DAC+}.
2. An existing circuit voltage or other known voltage is used for V_{REF}.
3. In a difference amplifier, R_3/R_2 needs to equal R_F/R_G to balance the gain of the amplifier.*
4. The equations will be solved for the condition where the DAC current on the positive side is zero (I_{DAC+} = 0 mA). This in turn will set the DAC voltage on the positive side to its minimum value, $V_{DAC+} = V_{DAC+(min)}$. Note that this value is different from that of the current-sinking DAC in Part 1, where setting I_{DAC+} = 0 mA led to $V_{DAC+} = V_{DAC+(max)}$.

*Note that in a voltage-feedback op amp, it is desirable to make the impedance at V_p equal to that at V_n in order to cancel voltage offset caused by the input bias current. In a current-feedback op amp, the input bias currents are not correlated; so it is acceptable not to balance these impedances, but it may be desirable to minimize them.

Figure 13. Positive side of analysis circuit



With these constraints, algebra and simultaneous-equation techniques can be applied to Equations 20 and 21 to solve for $1/R_1$:

$$\frac{1}{R_1} = \frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} - \frac{1}{R_2+R_3} \quad (22)$$

The known value for R_1 can be substituted into Equation 21, which can then be rearranged to find $1/R_X$. The result is exactly the same as in Part 1:

$$\frac{1}{R_X} = \frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2+R_3} \quad (23)$$

Analysis of negative side

Figure 14 shows the analysis circuit for the negative side. The node equation at the V_{DAC-} output is the same as in Part 1 except for the DAC current's change in polarity:

$$\frac{V_{DAC-}-V_{REF}}{R_Y} + \frac{V_{DAC-}}{R_4} + \frac{V_{DAC-}-V_n}{R_G+R_3} - I_{DAC-} = 0 \quad (24)$$

The equation for the DAC output impedance stays the same:

$$Z_{DAC-} = \frac{V_{DAC-}}{I_{DAC-}} \quad (25)$$

With substitution and rearrangement,

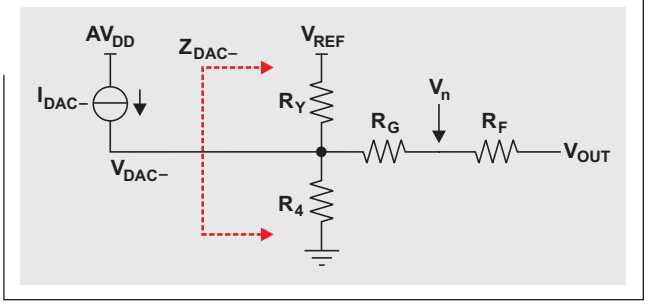
$$V_p = V_{DAC+} \times \frac{R_3}{R_2+R_3},$$

and $V_n = \alpha V_p$ can be used to rewrite Equation 25 as

$$\frac{1}{Z_{DAC-}} = \frac{1}{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}} \times \left(\frac{1}{R_Y}+\frac{1}{R_4}+\frac{1}{R_G}\right). \quad (26)$$

Using the same substitutions and general design constraints used on the positive side to drive values for Z_{DAC-}, V_{REF}, and R_G, simultaneous-equation techniques can be applied to Equations 24 and 26 to solve for $1/R_4$ (Equation 27 below). Note that the equations are solved for the condition where the DAC current on the negative side is zero: $I_{DAC-} = 0$ mA. This sets the DAC voltage on the negative side to its minimum value, $V_{DAC-} = V_{DAC-(min)}$, and sets the DAC voltage on the positive side to its maximum value, $V_{DAC+} = V_{DAC+(max)}$. The value of $1/R_4$ can then be used to find $1/R_Y$:

Figure 14. Negative side of analysis circuit



$$\frac{1}{R_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right) \quad (28)$$

Note that α, the multiplication factor from V_p to V_n, in essence expresses the difference between the input pins. In a voltage-feedback amplifier, α is set by the loop gain of the amplifier. In a current-feedback amplifier, α is the gain of the input buffer between the inputs. All that aside, α is typically close enough to 1 that it can simply be removed from the calculation.

Calculating output voltage

Superposition can be used to write equations for the separate terms referred to V_{OUT}. These equations are the same as those in Part 1. The difference is that now the DAC only sources current, which is by convention positive current flow, making the direction of the op amp's output-voltage swing match that of the DAC. In other words, when the DAC is sourcing current on the positive side, the output of the op amp tends to swing positive, and when the DAC is sourcing current on the negative side, the output of the op amp tends to swing negative. This means that in the following equations, I_{DAC+} and I_{DAC-} are always positive or zero.

$$\frac{1}{R_4} = \frac{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (27)$$

The output-referred DC bias from the positive side is

$$V_{OUT\_V_{p(DC)}} = \left(1 + \frac{R_F}{R_G + R_Y \parallel R_4}\right) \times \left[V_{REF} \times \frac{R_1 R_3}{R_1(R_2 + R_3) + R_X(R_1 + R_2 + R_3)}\right].$$

The output-referred DAC signal from the positive side is

$$V_{OUT\_V_{p(DAC)}} = \left(1 + \frac{R_F}{R_G + R_Y \parallel R_4}\right) \times \left[I_{DAC+} \times \frac{R_X R_1 R_3}{R_X R_1 + (R_1 + R_X)(R_2 + R_3)}\right].$$

The output-referred DC bias from the negative side is

$$V_{OUT\_V_{n(DC)}} = -\left(V_{REF} \times \frac{R_4}{R_Y + R_4} \times \frac{R_F}{R_G + R_Y \parallel R_4}\right).$$

The output-referred DAC signal from the negative side is

$$V_{OUT\_V_{n(DAC)}} = -\left(I_{DAC-} \times \frac{R_Y R_4 R_F}{R_Y R_4 + R_G R_4 + R_Y R_G}\right).$$

Adding these four equations provides an expression for V_{OUT}:

$$V_{OUT} = V_{OUT\_V_{p(DC)}} + V_{OUT\_V_{p(DAC)}} + V_{OUT\_V_{n(DC)}} + V_{OUT\_V_{n(DAC)}} \quad \textbf{(29)}$$

If it is assumed that $I_{DAC} = I_{DAC+} - I_{DAC-}$, $Z = Z_{DAC+} = Z_{DAC-}$, and $R_F/R_G = R_3/R_2$, the DC component of the DAC outputs will cancel and the AC signal's gain equation from the DAC output current to the voltage output of the op amp can be simplified and written as

$$\frac{V_{OUT}}{I_{DAC}} = 2Z \times \frac{R_F}{R_G}. \quad \textbf{(30)}$$

Design example and simulation

For an example of how to proceed with the design, assume that the PMOS DAC noted earlier, with a compliance voltage ranging from –1.0 V to +1.25 V, is being used. Also assume that the full compliance voltage range will be used to maximize the DAC output voltage, which in turn will minimize the gain required from the op amp and will require V_{REF} to be a negative voltage. The DAC full-scale output is set to 20 mA. To get a 5-V_{PP}, DC-coupled single-ended output signal, the circuit shown in Figure 12 can be used. Since a ±5-V power supply is being used for the op amp, it is convenient to make V_{REF} = –5 V. Given that $I_{DAC\pm}$ = 20 mA and $V_{DAC\pm}$ = 2.25 V_{PP}, the target impedance, $Z_{DAC\pm}$, can be calculated to equal 112.5 Ω.

With the starting design constraints given earlier, the Texas Instruments THS3095 current-feedback op amp is selected as the amplifier, where $R_3 = R_F$ = 750 Ω. The gain from $V_{DAC\pm}$ to the output is given by the resistor ratios $R_F/R_G = R_3/R_2$, so R_G can be calculated as

$$R_G = R_2 = R_F \times \frac{V_{DAC\pm}}{V_{OUT}} = 750\ \Omega \times \frac{2(2.25\ V)}{5\ V} = 675\ \Omega.$$

The nearest standard 1% value, 681 Ω, should be used.

Equations 22, 23, 27, and 28 can be used to find, respectively, R_1, R_X, R_4, and R_Y:

$$R_1 = \frac{1}{\frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)}-\frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{112.50\ \Omega\left(1+\frac{1}{\frac{-5\ V}{-1\ V}-1}\right)}-\frac{1}{681\ \Omega+750\ \Omega}} = 155.95\ \Omega$$

$$R_X = \frac{1}{\frac{1}{Z_{DAC+}}-\frac{1}{R_1}-\frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{112.5\ \Omega}-\frac{1}{155.95\ \Omega}-\frac{1}{681\ \Omega+750\ \Omega}} = 562.5\ \Omega$$

$$R_4 = \frac{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}}+\left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}$$

$$= \frac{\frac{-1\ V}{-5\ V+1\ V}+1}{\frac{1-\frac{112.5\ \Omega\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}}{681\ \Omega}}{112.5\ \Omega}+\left(\frac{1.25\ V\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}+1\ V}{-5\ V+1\ V}-1\right)\left(\frac{1}{681\ \Omega}\right)} = 206.84\ \Omega$$

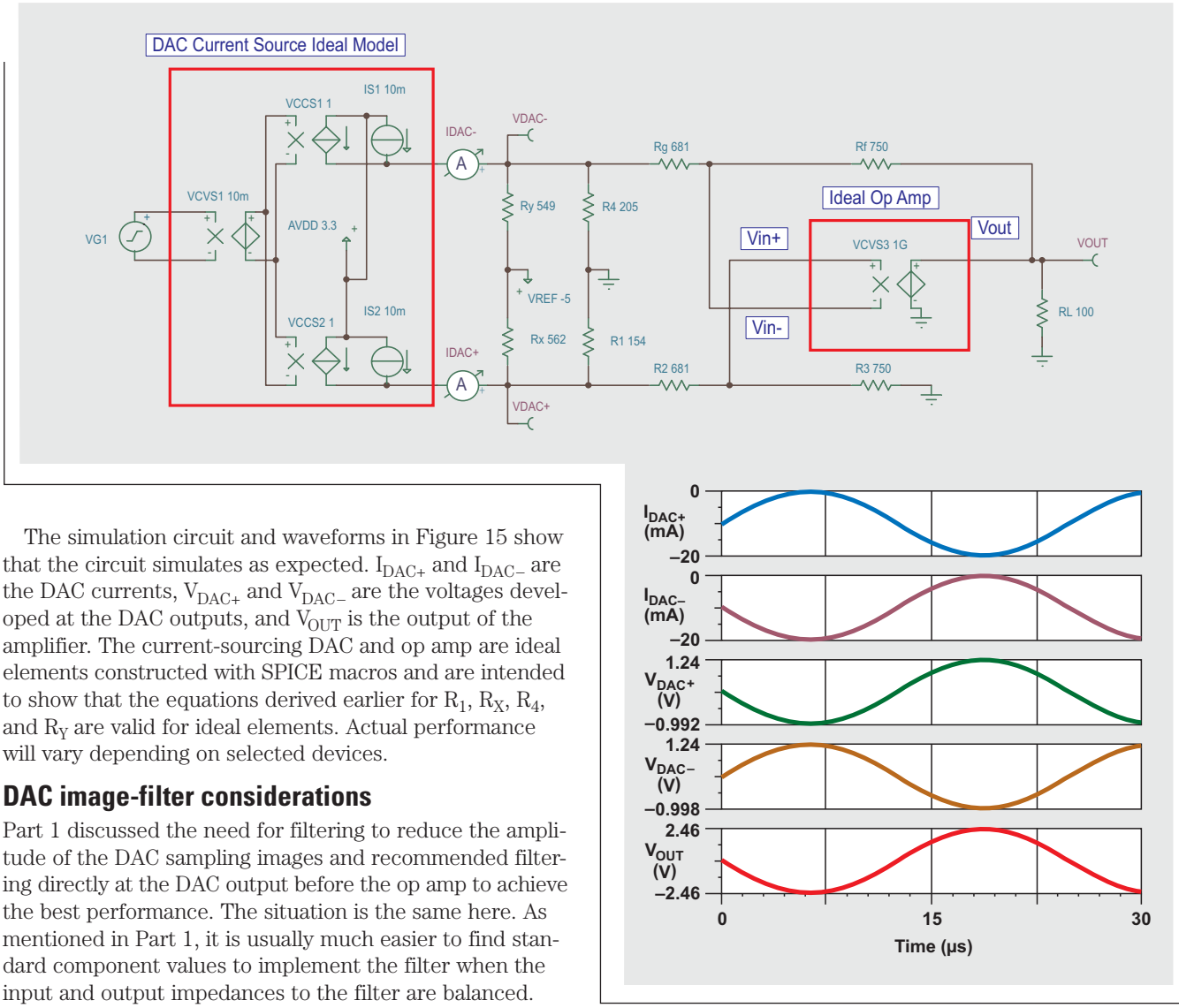
$$R_Y = \frac{1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}}-\left(\frac{1}{R_4}+\frac{1}{R_G}\right)} = \frac{1}{\frac{1-\frac{112.5\ \Omega\times1\times\frac{750\ \Omega}{681\ \Omega+750\ \Omega}}{681\ \Omega}}{112.5\ \Omega}-\left(\frac{1}{206.84\ \Omega}+\frac{1}{681\ \Omega}\right)} = 550.58\ \Omega$$

The nearest standard 1% values should be used: R_1 = 154 Ω, R_X = 562 Ω, R_4 = 205 Ω, and R_Y = 549 Ω.

These equations are easily solved when set up in a spreadsheet. To see an example Excel® worksheet, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht.xls and select the "DAC Source to Op Amp, No Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI™ simulation of the circuit in this example, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file DAC_Source_to_Op_Amp_No_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Figure 15. Simulation of current-sourcing DAC interfaced to op amp



The simulation circuit and waveforms in Figure 15 show that the circuit simulates as expected. I_{DAC+} and I_{DAC-} are the DAC currents, V_{DAC+} and V_{DAC-} are the voltages developed at the DAC outputs, and V_{OUT} is the output of the amplifier. The current-sourcing DAC and op amp are ideal elements constructed with SPICE macros and are intended to show that the equations derived earlier for R_1, R_X, R_4, and R_Y are valid for ideal elements. Actual performance will vary depending on selected devices.

DAC image-filter considerations

Part 1 discussed the need for filtering to reduce the amplitude of the DAC sampling images and recommended filtering directly at the DAC output before the op amp to achieve the best performance. The situation is the same here. As mentioned in Part 1, it is usually much easier to find standard component values to implement the filter when the input and output impedances to the filter are balanced.

Figure 16. Inserting DAC image filter

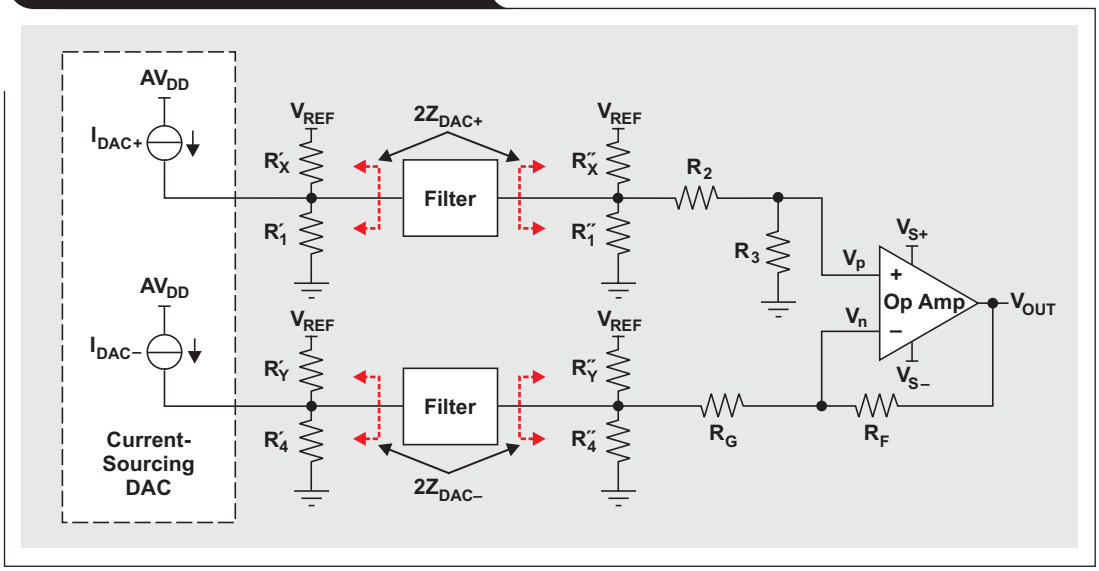


Figure 16 shows the proposed circuit implementation where R_1, R_X, R_4, and R_Y have been replaced with prime and double-prime components on either side of the filter, so that

$R_1 = R'_1 \parallel R''_1$,
$R_X = R'_X \parallel R''_X$,
$R_4 = R'_4 \parallel R''_4$, and
$R_Y = R'_Y \parallel R''_Y$.

At the same time, the impedance seen on each terminal of the filter is $2 \times Z_{DAC\pm}$. By use of algebra, the following equations can be derived:

$$\frac{1}{R'_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} \quad (31)$$

$$\frac{1}{R''_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(min)}}-1}\right)} - \frac{1}{R_2+R_3} \quad (32)$$

$$\frac{1}{R'_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R'_1} \quad (33)$$

$$\frac{1}{R''_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R''_1} - \frac{1}{R_2+R_3} \quad (34)$$

$$\frac{1}{R'_4} = \frac{\left[1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}}\right]}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (35)$$

$$\frac{1}{R''_4} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}} + \left[\frac{V_{DAC+(max)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(min)}}{V_{REF}-V_{DAC-(min)}}+1} \quad (36)$$

$$\frac{1}{R'_Y} = \frac{1 - \frac{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)}{R_G}}{2Z_{DAC-}} - \frac{1}{R'_4} \quad \textbf{(37)}$$

$$\frac{1}{R''_Y} = \frac{1 - \frac{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)}{R_G}}{2Z_{DAC-}} - \left(\frac{1}{R''_4} + \frac{1}{R_G}\right) \quad \textbf{(38)}$$

These equations are easily solved when set up in a spreadsheet. To see an example Excel worksheet, go to http://www.ti.com/lit/zip/slyt360 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht.xls and select the "DAC Source to Op Amp, Filtered" worksheet tab.

The performance is similar to that shown in the SPICE simulation for Part 1 (Reference 1). Please refer to that simulation to see the effects of balancing and matching the filter impedance versus using a filter with unmatched impedance.

Conclusion

This article has shown a circuit implementation using a single-stage op amp to convert complementary-current outputs from a current-sourcing DAC to a single-ended voltage. Equations were derived and a methodology presented for proper selection of component values to set the DAC's output-voltage compliance while maintaining balanced input signals to the op amp for best overall performance. Filter-design considerations were also included to explain proper insertion when filtering before the amplifier is desired.

Reference

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