LMK01000,LMK01010,LMK01020,LMK02000, LMK02002,LMK03000,LMK03001,LMK03002, LMK03033,LMK03200,LMK04000,LMK04001, LMK04002,LMK04010,LMK04011,LMK04031, LMK04033,LMK04800

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The Sight & Sound of Information

Clock Conditioner Owner's Manual

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The Sight & Sound of Information

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Chapter 1
Introduction to Precision Clock Conditioners

Introduction

In communication systems, audio systems, control systems, and data acquisition systems, Signal-to-Noise Ratio (SNR) is without question a key metric. Because clock noise contributes to the overall system noise, and because clocks are an essential part of all of these systems, controlling clock noise is an important part of the system designer's job. One of the tools available to the system designer is the precision clock conditioner. A clock conditioner is different from a timing device in that it gives the designer the capability to design a complete clock architecture (sub-system) that achieves the best possible performance for the cost. At a functional level, a clock conditioner gives the designer the capability to not only generate a precision clock, but also to re-condition and distribute a derived or externally generated clock. The purpose of this manual is to help the clock system designer understand the impact of noise on clock performance and understand the trade-offs that can be made for a given application.

Chapter 2 provides a fundamental introduction to phase noise and jitter and is intended to be a foundation for the discussion in the remaining chapters. **Chapter 3** discusses the fundamentals of PLL design and provides detailed design equations for a simple case. **Chapter 4** addresses the impact of noise in ADC clocks, and **Chapter 5** looks at clock jitter in serial data communications. Finally, **Chapter 6** covers some critical design issues for high-speed printed circuit board designs that contain clock conditioning circuits.

Precision Clock Conditioners

Precision clock conditioners are used to generate one or more clock frequencies from a given reference clock. Sometimes this reference clock may have excellent spectral purity and the function of the clock conditioner is to distribute this frequency, or some multiple of this frequency, throughout the system. This is a clock multiplier application. In other situations, this reference clock signal has very poor spectral purity, and the function of the clock conditioner is to clean up this signal; this is a jitter cleaner application. It is also possible that the clock conditioner could perform both functions simultaneously.

Strongly tied to the clock conditioner application are performance characteristics. ***The distinguishing characteristic of a precision clock conditioner is the noise performance.***

Aside from noise performance, other important performance characteristics can include skew between the outputs in a multi-output device, or clock distribution stage. Because the typical use of clocks is to provide a means for synchronizing events in a system, the ability to control and minimize skew and achieve well aligned clocks is vital.

Structure of a Clock Conditioner

Figure 1.1 shows a clock conditioner architecture. A clock conditioner conditions the clock signal that is applied to the Reference Oscillator (Ref Osc) input as shown in *Figure 1.1*. The Ref Osc input is routed to a Phase Locked Loop (PLL) that locks a Voltage-Controlled Oscillator (VCO) to a frequency that is typically equal to, or a higher multiple of the clock input frequency. This frequency can then be divided down to many different frequencies and distributed.

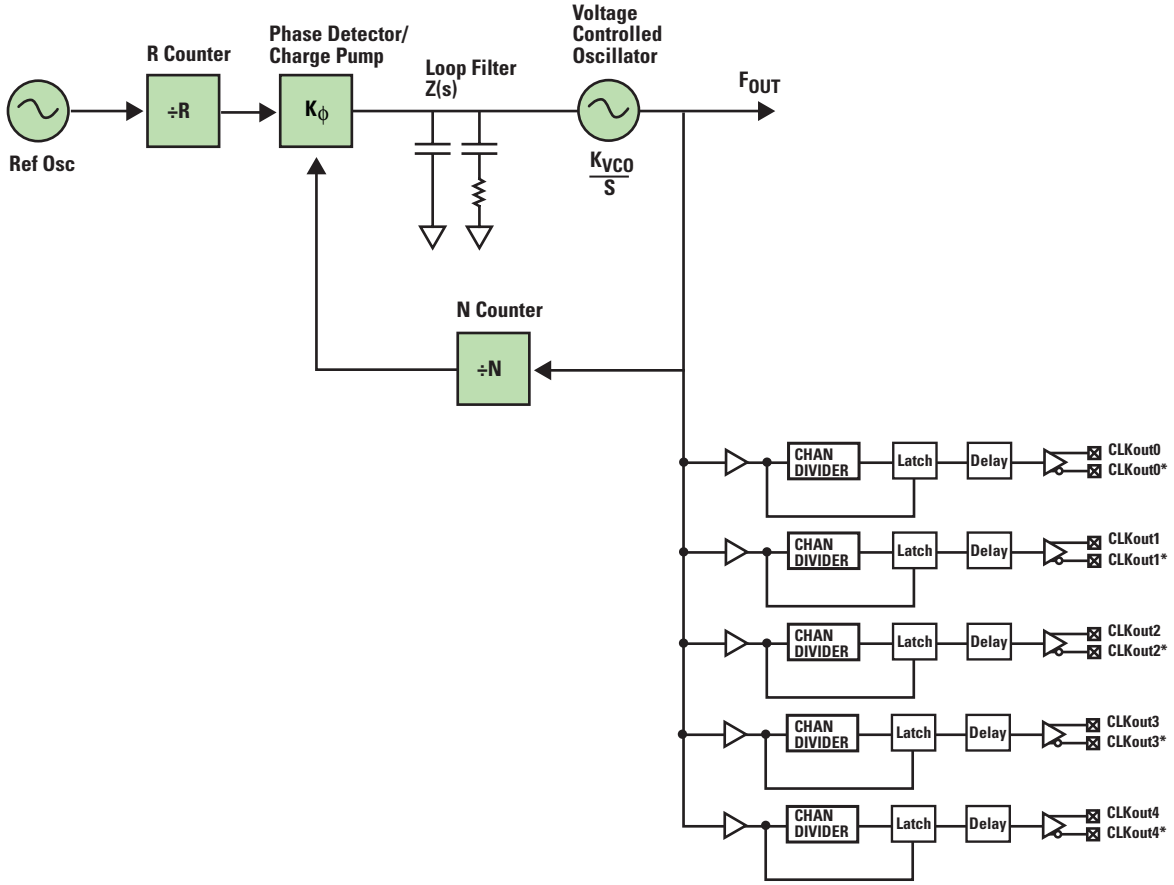


Figure 1.1 A Precision Clock Conditioner

There are several other features that may also be of importance in a clock conditioner. One such feature is hitless switching. In this feature, there are actually two clock inputs. If the primary input fails, then the device automatically switches to the secondary input. Ideally, the switching process would smoothly transition between the clocks without any discontinuities in phase. Hitless switching capability allows this to happen.

Clock Reconditioning

In a clock reconditioning application, the objective is to reduce the noise on an existing clock, sometimes referred to as jitter cleaning. For example, clocks distributed over a backplane can pick up noise and spurs through coupling with other signals, or become distorted as they pass through electrical interfaces. Another possibility is that a clock is intentionally made noisy through dithering in order to meet EMI requirements. Regardless of the cause, the function of the clock conditioner used in a jitter cleaner application is to reduce noise in the clock signal. The noisy clock signal is injected to the reference oscillator input of the clock conditioner device. The loop bandwidth of the PLL is designed to be relatively narrow, such that the noise on the input clock is filtered. Because the loop bandwidth is narrow, the VCO noise is dominant, and so jitter cleaner applications tend to have more stringent requirements for the VCO noise.

Another type of application where a clock conditioner could be used as a jitter cleaner is a Clock and Data Recovery (CDR) application, most often found in high speed serial data links. In this case, the clock must be recovered from the data stream itself. Consequently, the recovered clock will inherit the data jitter in the absence of jitter cleaning.

Clock Multiplier Applications

In clock multiplier applications, the VCO is locked to a multiple of the input clock signal, so that it can be divided down to several different frequencies and distributed. For example, a 30.72 MHz clock can be used to lock a VCO at 1536 MHz, which can be divided down to 30.72 MHz, 61.44 MHz, and many other desired frequencies.

If the input clock is a clean signal, then the PLL is typically designed for minimum jitter performance, which involves designing a loop bandwidth for the minimum integrated phase noise. This loop bandwidth is typically much wider than the one that is used for jitter cleaners. However, if the input clock is not clean, then the loop bandwidth can be made narrower so that the clock conditioner can function simultaneously as a jitter cleaner and a clock multiplier.

Creating a Fully Integrated Precision Clock Conditioner

Higher levels of integration are always desirable for cost and reliability reasons. There are two challenges that come with integrating this entire system. One is that the loop filter capacitor values can easily become too large to be practical to implement on silicon. Although capacitors can be integrated on silicon, it is a very expensive use of die area, and it is typically more feasible to keep the large capacitors external.

Integrating a VCO with good noise performance on silicon is also a challenge. Recall that it is noise performance that differentiates a precision clock conditioner from an ordinary timing device, and it is the VCO noise performance that is the dominant source of noise for the clock conditioner. For clock conditioners with a low noise VCO integrated, the VCO frequency is typically at a much higher frequency than the input clock or output clock frequency. The reason for this is that it is easier to create high frequency resonant circuits (in the GHz range) on silicon than low frequency resonators. For applications where the VCO noise performance requirements are too strict for an integrated VCO, clock conditioner chips that require an external VCO can be used. It is also generally true that as the tuning range of the VCO increases, the noise performance of the VCO degrades. This implies that the clock conditioner designer must make trade-offs between flexibility and performance.

Chapter 2
Phase Noise and Jitter

Introduction

In this chapter, we will examine the relationship between phase noise and jitter. Much of the material will be a basic review of oscillator concepts, sources of phase noise in oscillators, how they add to the phase noise profile of the oscillator, the relationship between phase noise and jitter, and measuring phase noise. Experienced designers may skip this chapter without loss of continuity with later material in this manual. Most of the material is presented with a minimum of derivation. For those that desire to develop a deeper understanding and derivation of the concepts presented here, the sources listed at the end of the manual provide excellent explanations on the selected topics.

Noise Sources and Noise Power

While the purpose of this manual does not include a comprehensive review of noise theory, it is useful to first review some noise basics. For a more thorough treatment of noise in oscillators, see [1] and [2]. Reference [3] provides a thorough review of noise in solid state devices in general.

A fundamental relationship that will appear repeatedly throughout this guide is the relationship between Power Spectral Density (PSD) in the frequency domain, denoted by S(f), and total power (P) measured over some bandwidth of interest:

$$P = \int_{f_L}^{f_U} S(f)\,df \tag{2.1}$$

where the limits of integration f_U and f_L define the power bandwidth, that is, bandwidth B = $f_U - f_L$.

Because we usually are concerned with Signal to Noise power Ratios (SNRs) in circuit design, we often work with noise PSDs when performing SNR analysis. This is because the relevant noise power is that which appears in the bandwidth of the desired signal (which has not been defined at this point), so we must understand the spectral shape of the noise in this bandwidth only. Noise outside this bandwidth is irrelevant.

Noise sources can be grouped into one of two general categories: device noise and interference [4]. Device noise is intrinsic to the components that make up the oscillator circuit and includes thermal noise, flicker noise and shot noise. External source examples include power supply noise and electromagnetic interference.

There are four basic noise types that appear in the semiconductor domain: thermal noise, shot noise, generation-recombination noise, and 1/f or flicker noise.

We normally think of thermal noise as being generated in a Resistor (R), being due to the random collision of charge carriers and proportional to the temperature of the device. It has a flat power spectral density, usually denoted as N_0:

$$S_T(f) = N_0 = 4kT\ W/Hz \tag{2.2}$$

where k = Boltzman's constant, T= Temperature (Kelvin), and R= Resistances in ohms. The power in thermal noise is $4kT$B, where B = the measurement bandwidth. Because the power spectral density does not depend on frequency and is constant for some temperature T, it is classified as white noise. This noise is not peculiar to semiconductors, and is found in most current-carrying devices.

---

1 W.P. Robins, *Phase Noise in Signal Sources*, Peter Peregrinus, Ltd., London, UK, 1982.
2 A. Van Der Ziel, " Noise in Solid State Devices and Lasers," *Proceedings of the IEEE*, Vol. 58, No. 8, August 1970, pp. 1178-1206
3 F. N Hooge, "1/f Noise Sources," *IEEE Transactions on Electron Devices,* Vol. 41, No. 11, November 1994.
4 A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid State Circuits,* vol. 33, pp. 179-194, Feb. 1998.

The cause of flicker noise, or 1/f noise in semiconductors is less well understood than other noise sources and there has been extensive discussion in the literature. It is low frequency in nature, with a power spectral density that is proportional to 1/f close to the oscillation frequency. The 1/f characteristic is eventually dominated by white (flat) noise at offset frequencies above 100 Hz.

Shot noise comes from the random movement of charge carriers across barriers of different potential, such as those found in diodes and transistors. Its power spectral density is proportional to the current flowing across the barrier, or:

$$S_I(f) \propto 2qI(f) \tag{2.3}$$

where I(f) is the current spectrum and q is the electron charge.

Generation-Recombination noise is due to the fluctuation in the number of free electrons in the conduction band of a semiconductor device. Its power spectral density is proportional to:

$$S_G(f) \propto \frac{4\tau}{1+4\pi^2 f^2 \tau^2} \tag{2.4}$$

where τ = relaxation time, a characteristic of the device construction and physics.
Note that this noise has a spectral density that has a low-pass characteristic with cutoff frequency $\frac{1}{(2\pi\tau)^2}$.

Oscillators and Phase Noise

A Mathematical Model of an Oscillator

Oscillators are electrical or electro-mechanical devices that output a voltage or current that alternates polarities with a stable (fixed) frequency and amplitude. Oscillators are typically used in applications when either precise timing or frequency of operation is required. Like any circuit, oscillators are afflicted by noise, the enemy of optimal performance for most electric circuits. This begs the question, "what is optimal?" Mathematically we can answer this question using the following equation:

$$v(t) = V_0 \sin(\omega_0 t) \tag{2.5}$$

In this case, the oscillator output is a perfect sinusoid of amplitude V_0 and frequency ω_0 radians/second. It is perfect in the sense that there is neither a time dependent phase term beyond the fundamental, nor a time dependent amplitude term. ***Figure 2.1*** and ***Figure 2.2*** illustrate a perfect sinusoid in the time domain and frequency domain.

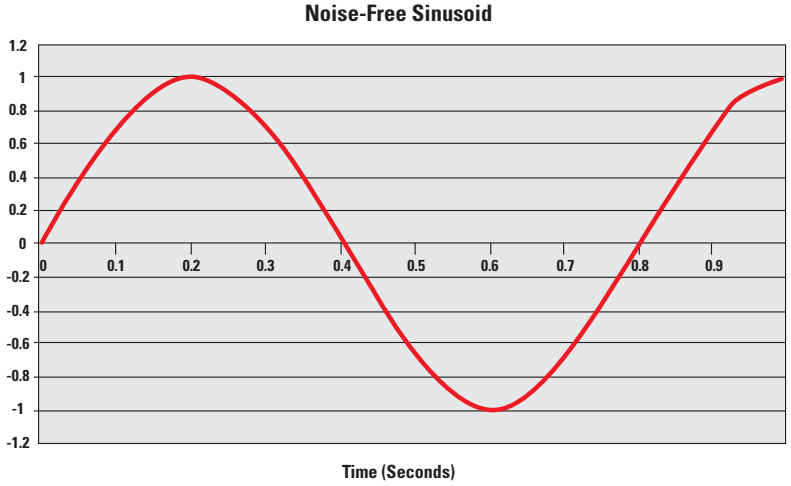


Figure 2.1 Time Domain Plot of a Noise-Free Sinusoid

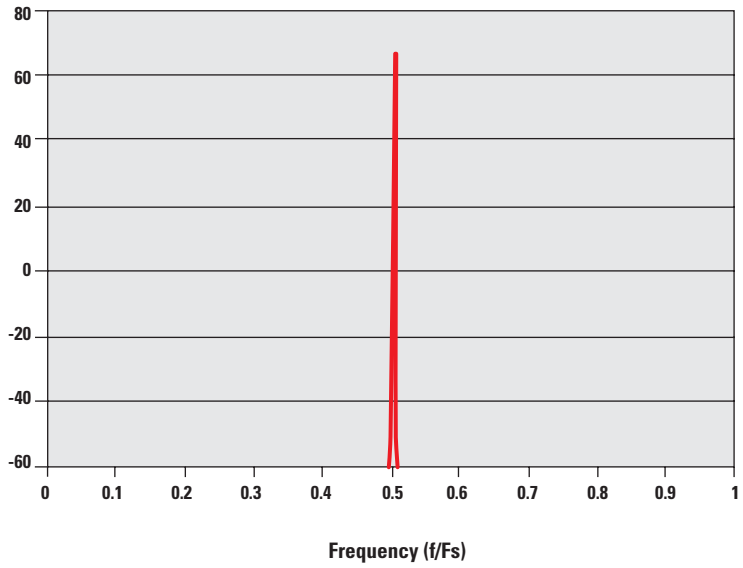


Figure 2.2 Frequency Domain Representation of a Noise-Free Sinusoid

Unfortunately, perfect oscillators do not exist in the real world. A noisy oscillator can be described mathematically as:

$$v(t) = V_0\left(1 + m(t)\right)\sin(\omega_0 t + \phi_N(t)) \quad (2.6)$$

This expression contains both additive amplitude noise [m(t)] and additive phase noise [$\phi_N(t)$]. These terms represent random amplitude modulation and random phase modulation on the fundamental. The instantaneous frequency is the derivative of the phase with respect to time:

$$\omega_{osc} = \omega_0 + \frac{d\phi_N}{dt} = \omega_0 + \Delta\omega(t) \quad (2.7)$$

Thus the instantaneous frequency is the fundamental plus some residual value, $\Delta\omega(t)$. When analyzing phase noise in an oscillator, both m(t) and $\phi_N(t)$ are usually modeled as a sinusoid, or sum of sinusoids:

$$\sum_m K_m \cdot sin\left(\omega_m t\right) \quad (2.8)$$

The amplitude constant K_m will represent either a modulation depth parameter for AM noise or peak deviation parameter for PM noise [5]. Substituting (2.8) into (2.6) yields a spectrum that includes the fundamental frequency term [ω_0] plus sidebands at [ω_0-ωm] and [ω_0+ωm] [6]. In reality, the modulating terms m(t) and $\phi_N(t)$ in (2.6) are random processes that can be modeled as the sum of a large number of sinusoidal sidebands spaced 1 Hz apart. The power in these sidebands is determined by the parameter K, denoted as K_m and β_n in ***Equation (2.9)***:

$$v(t) = V_0\left(1 + \sum_{m=1}^{\infty} K_m \sin\left(\omega_m t\right)\right)\sin(\omega_0 t + \sum_{n=1}^{\infty} \beta_n \sin(\omega_n t)) \quad (2.9)$$

where $m(t) = \sum_{m=1}^{\infty} K_m \sin(\omega_m t)$, and $\phi_N(t) = \sum_{n=1}^{\infty} \beta_n \sin(\omega_n t)$.

5 Martin S. Roden, *Analog and Digital Communication Systems,* 4th Ed., Prentice-Hall, Inc., Englewood Cliffs, NJ, 1995.
6 W.P. Robbins, *Phase Noise in Signal Sources*, Peter Peregrinus, Ltd. London, UK, 1982.

As shown in ***Equation (2.7)***, the instantaneous frequency of the noisy oscillator is the fundamental plus some residual value, Δω(t). This residual value appears as sidebands to the fundamental. Because Δω(t) is a random process, it spreads energy across frequency, above and below the fundamental. ***Figure 2.3, Figure 2.4,*** and ***Figure 2.5*** illustrate a noisy sinusoid in the time and frequency domains.

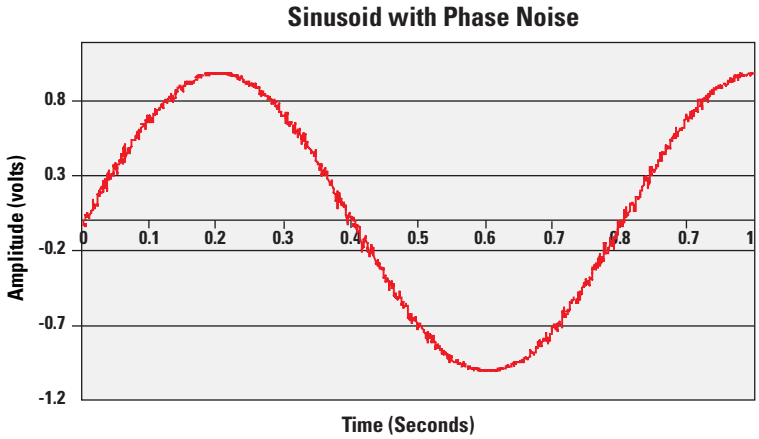


Figure 2.3 Time Domain Plot of a Noisy Sinusoid

Figure 2.4 shows the rising edge of the noisy sinusoid. The expected zero crossing on the time scale is 0.8, but the actual zero crossing does not occur at 0.8. This particular plot shows that there is a momentary crossing prior to 0.8, and the final crossing is delayed with respect to 0.8. If this waveform was used to clock a data converter and also assuming that the second zero crossing triggers the sampling process, then the resultant sample would reflect an additive error in the signal value. Depending on the slope of the sampled signal at this point time, this error may or may not be significant. The implications of noise on an ADC sampling clock will be covered in more detail in Chapter 4.

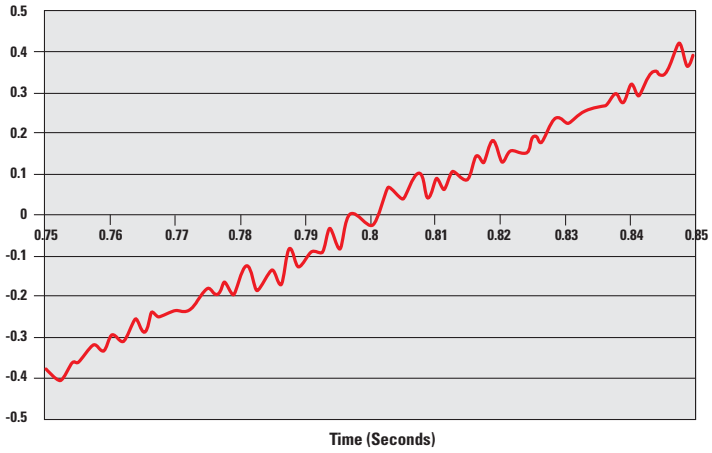


Figure 2.4 Noisy Sinusoid Magnified

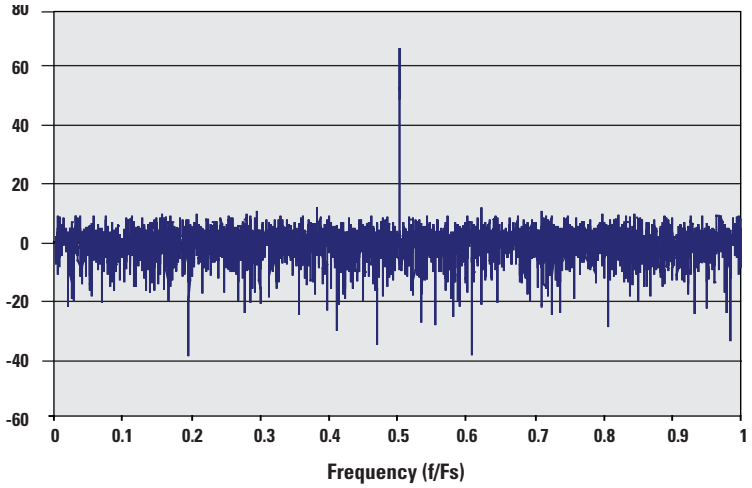


Figure 2.5 Frequency Domain Representation of a Sinusoid with Phase Noise

Comparing ***Figure 2.5*** to ***Figure 2.2***, we see that the noise floor has increased relative to the level of the oscillator power. In this example, the phase noise is Gaussian, so its PSD is flat.

A Simple Model of a Noisy Oscillator

Equations (2.6) and ***(2.9)*** are informative from a mathematical perspective and give us a means for abstracting the oscillator noise power spectrum mathematically, independent of noise mechanics. However, we need a more tractable approach for modeling and measurement, in order to more effectively understand and deal with phase noise in oscillators. To facilitate this, we will start from a fundamental model of an oscillator and examine how white noise is shaped by the transfer function of the oscillator so that it is no longer white (flat) at the output.

Oscillators can be constructed using several methods, but basically consist of a resonating element and an energy storage element. Two examples are L-C tank circuits and crystals. For this discussion we will use an L-C tank model, illustrated in ***Figure 2.6.*** [7] and [8] provide a good introduction to the basics of oscillator noise and form the basis of much of the following discussion.

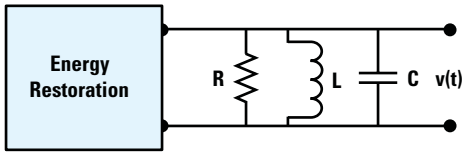


Figure 2.6 Simple RLC Oscillator Model

To begin, it is assumed that the only lossy element in the circuit is the tank resistance and that the energy restoration block is noiseless. From the preceding discussion of noise, we know that the noise power in the resistor is 4kTB. This is equal to the square of the RMS voltage across R divided by R:

(2.10)

$$P_{noise} = 4kTB = \frac{\overline{V_{noise}^2}}{R} \Rightarrow \overline{V_{noise}^2} = 4kTRB$$

7 T. H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial," IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000.
8 T.H. Lee and A. Hajimiri, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid State Circuits, Vol. 33, No. 2, February 1998.

Our interest is the power spectral density of the noise at the oscillator output. The flat noise spectrum of ***Equation (2.10)*** is filtered by the tank response, Z(f), which is the R/L/C parallel impedance. The noise spectrum of the oscillator is the noise current spectral density multiplied by the magnitude squared of the tank impedance:

(2.11)

$$\frac{\overline{V_{noise}^2}}{R \cdot B} = \frac{\overline{I_{noise}^2}}{B} \cdot \frac{|Z(f)|^2}{R}$$

An approximation of the tank impedance for a small offset Δω from the resonant frequency ω_0 is given by [5]:

(2.12)

$$Z(\omega_0 + \Delta\omega) \approx j\frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}} \Rightarrow |Z(f)|^2_{\Delta f = \frac{\Delta\omega}{2\pi} << \omega_0} = \left(\frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}}\right)^2$$

The Q of an oscillator circuit is proportional to the energy stored divided by the power dissipated. Q can also be defined in terms of circuit parameters, since both energy storage and power dissipation will also depend on them. Using the following expression for Q:

(2.13)

$$Q = \frac{R}{\omega_0 L}$$

Equations (2.11) and ***(2.12)*** can be combined to obtain an expression for the power spectral density of the output noise voltage:

(2.14)

$$S_{noise}(f) = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2$$

$$= \frac{4kTR\omega_0^2}{4 \cdot Q^2} \cdot \frac{1}{\Delta\omega^2}$$

From ***Equation (2.14)*** we see that the flat spectrum of the (white) thermal noise in the resistor has been shaped by the resonator response, exhibiting a $1/f^2$ behavior at the output of the oscillator. The second version of ***Equation (2.14)*** also says that maximizing Q minimizes the noise PSD. If we think in terms of SNR, maximizing Q pushes down the spectral density of the thermal noise, which in turn will improve SNR.

If we now consider how 1/f noise might be shaped by the oscillator response, by analogy with white noise, we would expect 1/f noise to be transformed into $1/f^3$ noise at the output. The process of noise transformation will be expanded in the next section where we discuss Phase Locked Loops (PLLs) combined with voltage-controlled oscillators.

Models for Voltage-Controlled Oscillators and Phase Locked Loops

Most clock conditioners consist of Voltage-Controlled Oscillators (VCOs) combined with Phase Locked Loops (PLLs) in order to synchronize the oscillator to a specific frequency reference source. In many applications, this is either required or provides certain benefits that cannot be obtained with a free-running oscillator (i.e., one not controlled by a PLL). Consequently, when we consider how noise is injected in to the circuit, our model will include a PLL. A model of a noiseless PLL and VCO, with a reference oscillator, is shown *Figure 2.7*.

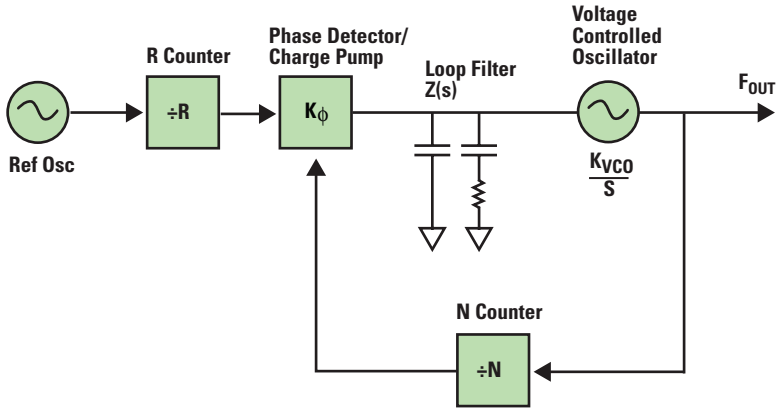


Figure 2.7 Model of Noiseless PLL and VCO

Noise can be injected into an oscillator and PLL in a variety of ways from a variety of sources, hence, the $\phi_N(t)$ term in *Equation (2.6)* is comprised of more than one noise source. A VCO/PLL model with various injection points for noise is illustrated in *Figure 2.8*.

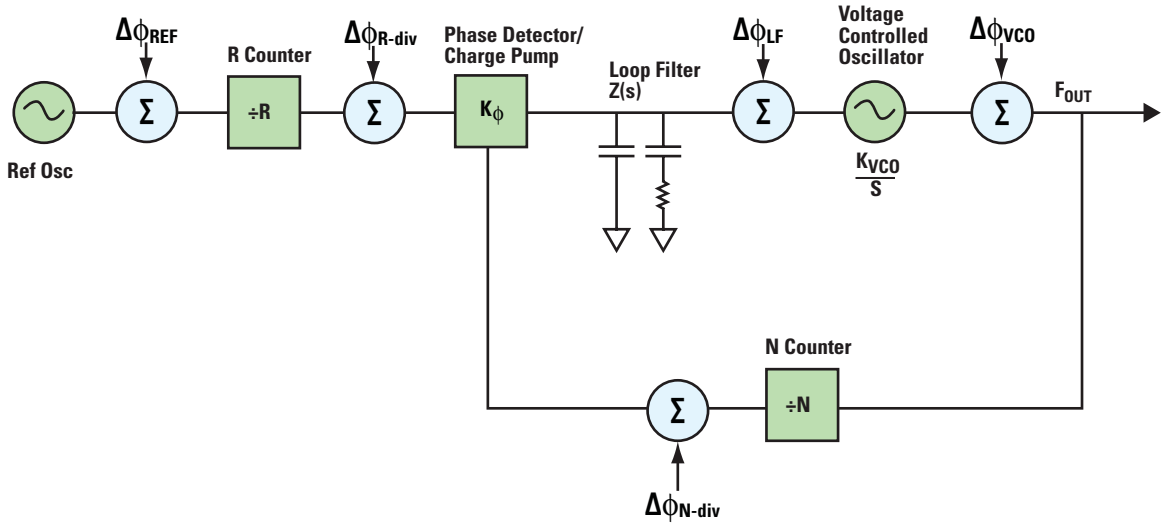


Figure 2.8 Noise Model for PLL/VCO

A discussion of the origin and characterization of each of the noise sources shown in ***Figure 2.8*** is beyond the scope of this guide. There has been extensive coverage in the literature of the types of noise induced in each of the functional blocks in the PLL and VCO – [9][10][11][12][13][14][15]. Regardless of the character of the noise appearing at each of the summation points in ***Figure 2.8,*** each will be shaped by the transfer function defined between the injection point and the VCO output. If we define the forward transfer function from the phase detector/charge pump to the VCO output as G(s):

$$G(s) = \frac{K_\phi \cdot Z(s) \cdot K_{VCO}}{s} \tag{2.15}$$

where s = j2π f, then the closed loop transfer functions from the various noise injection points in the circuit to the VCO output can be defined, as listed in ***Table 2.1***.

Table 2.1 Noise Transfer Functions

Noise Source	Transfer Function
Reference	$\frac{1}{R} \bullet \frac{G(s)}{1+G(s)/N}$
R Divider	$\frac{G(s)}{1+G(s)/N}$
N Divider	$\frac{G(s)}{1+G(s)/N}$
Phase Detector	$\frac{1}{K\phi} \bullet \frac{G(s)}{1+G(s)/N}$
VCO	$\frac{1}{1+G(s)/N}$

For example, if the noise appearing at the reference oscillator output has spectral density $S_{Ref}(f)$, then the same noise at the VCO output has a PSD of:

$$S_{Ref\text{-}out}(f) = S_{\mathrm{Re}}(f) \cdot \frac{1}{R^2} \left| \frac{G(s)}{1+\frac{G(s)}{N}} \right|^2 \tag{2.16}$$

Consequently, the reference oscillator noise appearing at the VCO output is transformed by the loop transfer function. If the transfer function has a low pass characteristic, then any reference oscillator noise higher than the cutoff frequency is removed. This leads to the conclusion that if we analyze each of the loop transfer functions in the table, we can determine the critical noise frequencies which get passed to the VCO output. Armed with this information, the circuit designer is given some capability for optimizing performance. In addition to having some control over loop characteristics, there is some guidance to be found in component selection. For example, as noted above, if the reference oscillator transfer function is low pass, then a reasonable approach is to choose a reference oscillator that has very good phase noise inside the loop bandwidth but whose phase noise outside the loop bandwidth may be relatively poor because any noise outside the loop bandwidth is eliminated. PLL operation and design will be covered in more detail in Chapter 3.

9 T. H. Lee, "Oscillator Phase Noise: A Tutorial," IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000.
10 A. Hajimiri, T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998.
11 E. Drucker, "Model PLL Dynamics and Phase-Noise Performance," Microwaves & RF, February 2000.
12 A. Mehrotra, "Noise Analysis of Phase-Locked Loops," IEEE Transactions on Circuits and Systems – I, Fundamental Theory and Applications, Vol. 49, No. 9, September 2002.
13 P. Heydani and M. Pedram, "Analysis of jitter due to power supply noise in phase-locked loops," *Proc. IEEE 2000 Custom Integrated Circuits Conf.*, May 2000, pp. 443-446.
14 J. Phillips and K. Kundert,"Noise in Mixers, Oscillators, Samplers, and Logic: An Introduction to Cyclostationary Noise," Proc. IEEE Custom Integrated Circuits Conf., May 2000.
15 C-H Lee, J. Cornish, K. McClellan, J. Choma Jr., "Design of Low Jitter PLL for Clock Generator with Supply Noise Insensitive VCO," Proc. IEEE International Symposium on Circuits and Systems, Vol. 1, 1998, pp. 233-236.

Phase Noise and Power Spectral Density

Ultimately we are interested in how the noise injected into the clock conditioner, as depicted in ***Figure 2.8*** combines to produce the side bands on the output. The relative power in these sidebands translates to an SNR which is usually the measure of circuit performance. Because the noise PSDs and transfer functions differ, the combined noise at the output results in a unique phase noise PSD. This combined PSD will be denoted as $S_\phi(f)$. It will have sideband regions which exhibit different characteristics, often distinguished by the slope of the PSD in each region. ***Figure 2.9*** shows an actual phase noise plot (single-sided) for a PLL/VCO captured with a spectrum analyzer. $S_\phi(f)$ is the double-sided PSD, but it is more common to work with the single-sided PSD, denoted $L_\phi(f)$. This is the spectrum depicted in ***Figure 2.9.*** Note that both amplitude and frequency scales are in the log domain.

Figure 2.9 Spectrum Analyzer Phase Noise Display

A Power Law Model of Phase Noise

Mathematically, the phase noise power spectrum characteristic, as shown in ***Figure 2.9*** is generally modeled using [16]:

$$S_\phi(f) = A_{\alpha 1}\left(\frac{\omega_{\alpha 1}}{\Delta\omega}\right)^{\alpha 1} + A_{\alpha 2}\left(\frac{\omega_{\alpha 2}}{\Delta\omega}\right)^{\alpha 2} \ldots + A_{\alpha M}, \quad \omega = 2\pi f \tag{2.17}$$

Equation (2.17) models the sum of noise sources that follow a power law. As noted above, each region of the spectrum in ***Figure 2.9*** has a different noise spectral density profile due to the origin and mechanism of the noise. The $\omega_{\alpha m}$ parameters in the numerators represent corner frequencies for the different noise sources, or the frequencies at which the PSD attributable to the source in question intersects the PSD of another contributor. Note that the frequency argument in the denominators cause the noise density to fall off geometrically for some order $\{\alpha_m\}$ of $1/\Delta\omega$, where $\Delta\omega$ is some offset frequency from the carrier, ω_0. The coefficients $\{A_m\}$ determine the noise power relative to the carrier. ***Equation (2.14)*** is an example of a term that can contribute to $S_\phi(f)$.

16 I. Mahboob, J. Lee, K. Kim, "Performance comparison of digital modulation schemes with respect phase noise spectral shape," 2000 Canadian Conference on Electrical and Computer Engineering, 7-10 March 2000, pp. 856-860.

Figure 2.10 is a log domain representation of how these individual sidebands combine to create the composite PSD. At low offset frequencies (<1 kHz), the noise with $1/f^3$ characteristic dominates, while at frequencies higher than 10 kHz, 1/f noise dominates.

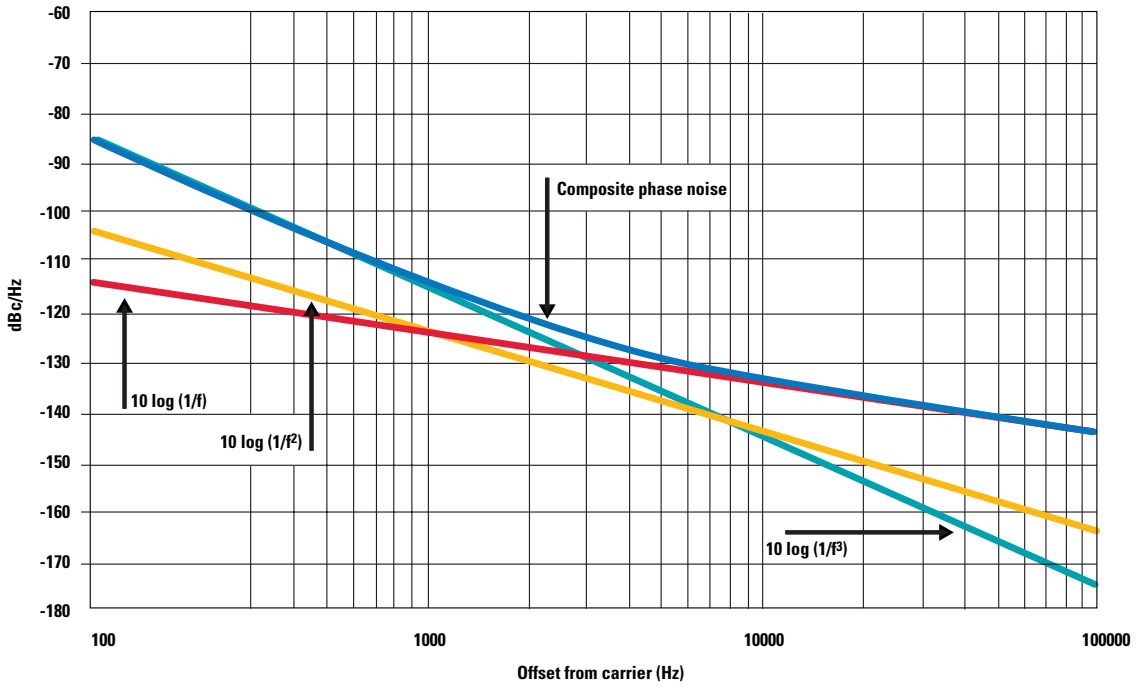


Figure 2.10 Single Side Band Logarithmic Plot of Phase Noise at Offsets from the Carrier

Ultimately, the designer's interest is in the total power of the phase noise because it will allow him or her to calculate SNR in certain applications. The total power in the phase noise is the integral of $S_\phi(f)$, or, the area under the phase noise PSD:

$$\sigma_\phi^2 = \int_{f_L}^{f_H} S_\phi(f)\,df = 2 \cdot \int_{f_C}^{f_H} L_\phi(f)\,df \qquad (2.18)$$

$S_\phi(f)$ has units of rad^2/Hz. The second version of ***Equation (2.18)*** assumes that $S_\phi(f)$ is symmetric about the carrier, which is reasonable for almost all cases. $L_\phi(f)$ therefore represents the one-sided PSD of the phase noise. Any expression for $L_\phi(f)$ that we are able to derive, measure, or otherwise define is always normalized to the carrier power so that the value of the noise PSD at any offset from the carrier is relative to the carrier power. In the log domain, the PSD carries units of dBc/Hz. It is important to understand that the measured power defined in ***Equation (2.18)*** is dependent on the integration bandwidth, defined by the integration limits. The lower limit of integration may not necessarily be the carrier frequency for a variety of reasons. When phase noise specifications are provided for oscillator circuits, they are typically stated for a small set of offsets from the carrier, usually at offsets of 1 kHz, 10 kHz, and 100 kHz, in units of dBc/Hz, i.e, in a 1 Hz bandwidth. Note that the parameter set $\{\alpha_m\}$ in ***Equation (2.17)*** is not restricted to integer values and that there is no fixed relationship of corner frequencies $\{\omega_{\alpha m}\}$ to $\{\alpha_m\}$. In a nutshell, this means that $S_\phi(f)$ can take on an infinite number of shapes. So, specifying a single value for phase noise, as in ***Equation (2.18)*** does not provide any information about the shape of the phase noise PSD or its value at specific offsets. Likewise, providing phase noise density values at specific frequency offsets does not provide any information about total phase

noise power, but it does begin to provide some information about the shape of the PSD. In ***Figure 2.9*** we see that the noise spectrum exhibits different slopes in different frequency regions offset from the carrier. The display starts at 100 Hz offset from the carrier at the low end (left side) and ends at 40 MHz offset from the carrier at the high end (right side). The first distinct region extends from 100 Hz to approximately 2 kHz, exhibiting a 1/f slope, or -10 dB per decade. The next region is flat (0 dB slope), running from 2 kHz to approximately 20 kHz. The next region exhibits a slope of -30 dB/decade from about 20 kHz to 6 MHz. Finally, at higher offsets, the plot begins to flatten to a 0 dB slope. Up to approximately 20 kHz, the response is determined by the combination of the reference signal's phase noise and the PLL, which in this case has a loop bandwidth of 20 kHz. Beyond the loop bandwidth, the VCO noise will dominate the PSD.

The shape of the phase noise spectrum and the total area under the curve (power) holds significance in several ways. First, the relative power at specific offsets can be critical, depending on the application. For example, in communication receivers that employ a superheterodyne architecture, excessive phase noise of a Local Oscillator (LO) can cause leakage of adjacent high-power signals into the desired signal band, severely degrading SNR. Second, the total RMS phase noise (or power) translates directly to a measure of jitter performance, as will be discussed in more detail in Chapter 4 and Chapter 5. The designer has some measure of control over the spectral shape and total RMS phase noise through the choice of reference oscillator, VCO and PLL characteristics. These aspects will be discussed in detail in Chapter 3.

Measuring the Phase Noise PSD with a Spectrum Analyzer

Equation (2.18) implies that we need to know the closed form expression for $L_{\phi}(f)$ in order to calculate RMS phase noise. However, we've already noted that $S_{\phi}(f)$ can take on an infinite variety of forms. Thus, directly measuring $L_{\phi}(f)$ is the most viable approach to finding σ_{ϕ}. This is often done with a spectrum analyzer. Some spectrum analyzers are capable of not only generating a spectral density plot of phase noise, but, can also directly calculate σ_{ϕ} from the measured spectrum. However, not all spectrum analyzers have this capability. Fortunately, there is exists a method for generating a reasonably accurate estimate of the area under $L_{\phi}(f)$ based on the spectral plot captured by such an analyzer. If $L_{\phi}(f)$ is plotted in the log domain, it can be characterized in different frequency regions by its slope. ***Figure 2.11*** replicates ***Figure 2.9*** with linearized slopes drawn for different regions.

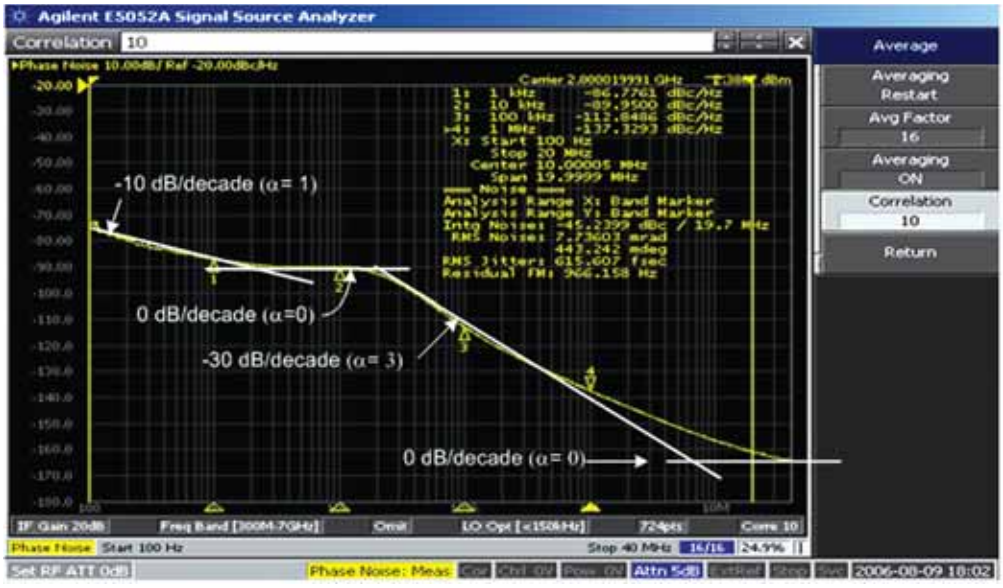


Figure 2.11 Log Domain Plot of L(f) with Linearized Slopes

An estimate of the area under $L_\phi(f)$ can be obtained by breaking it into regions that correspond to different terms from ***Equation (2.17)***, reading the relevant parameters from the spectrum analyzer display, and applying these parameters in the appropriate expressions that represent the integral of the area under the PSD. In order to do this, the one-sided phase noise spectrum $L_\phi(f)$ is expressed in a modified form of ***Equation (2.17)***:

$$L_\phi(\Delta f) = \sum_{\alpha=0}^{M-1} \frac{A_\alpha}{\Delta f^\alpha} = A_0 + \frac{A_1}{\Delta f} + \ldots + \frac{A_{M-1}}{\Delta f^{M-1}} \tag{2.19}$$

where the variable Δf represents the offset from the carrier. As shown in ***Figure 2.11***, each region corresponding to a different power of $1/f^\alpha$ will have a characteristic slope of -10log(α). For integer values of α {0,1,2…}, the corresponding slopes will be 0 dB, -10 dB/decade, -20 dB/decade, and so on. If we define regions on $L_\phi(\Delta f)$ by the end points Δf_U and Δf_L, where $\Delta f_U > \Delta f_L$, then the area under each region of the PSD is:

$$\int_{\Delta f_L}^{\Delta f_U} \frac{A_\alpha}{\Delta f^\alpha} d\Delta f \tag{2.20}$$

and,

$$\int_{f_L}^{f_U} L_\phi(f)\, df \approx \sum_\alpha \int_{\Delta f_L}^{\Delta f_U} \frac{A_\alpha}{\Delta f^\alpha} d\Delta f \tag{2.21}$$

Depending on the value of α, the solution of ***Equation (2.20)*** will take on one of the following forms:

$$\begin{cases} \alpha = 0, & A_\alpha \cdot \left(\Delta f_U - \Delta f_L\right), \\ \alpha = 1, & A_\alpha \cdot \ln\left(\dfrac{\Delta f_U}{\Delta f_L}\right), \\ \textit{otherwise} & \\ & A_\alpha \cdot \dfrac{1}{1-\alpha} \cdot \left(\Delta f_U^{1-\alpha} - \Delta f_L^{1-\alpha}\right) \end{cases} \tag{2.22}$$

We can estimate the value of A_α for each region of the log plot based upon ***Figure 2.12.***

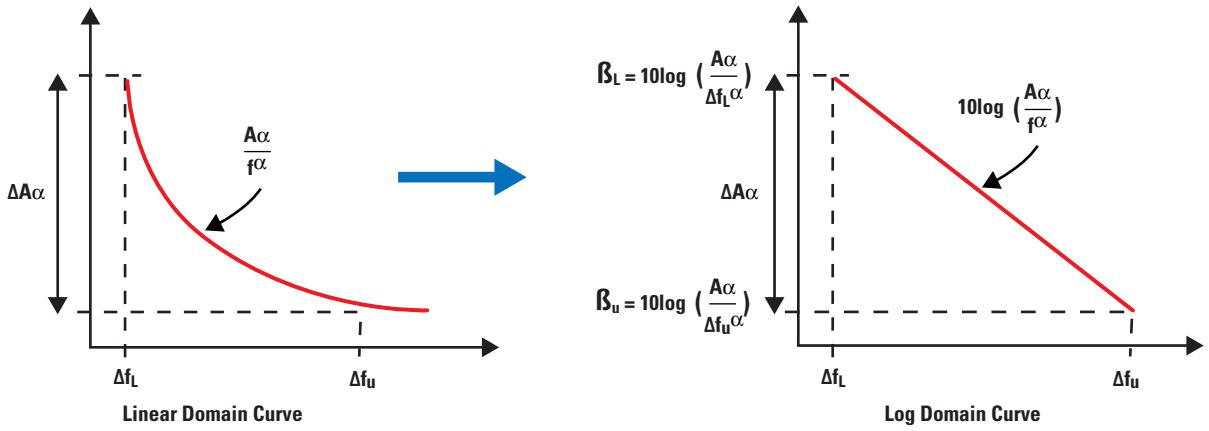


Figure 2.12 Estimating A_α Using Measured Values of $L_\phi(\Delta f)$

There are two methods we can use to find $\int L_{\phi}(\Delta f)d\Delta f$. They differ by the choice of α values and calculation of A_{α}.

Method 1:

1. Define linearized regions of $L_{\phi}(\Delta f)$ such that their slopes correspond to integer values of α {0,1,2,…}, meaning slopes with values of 0, -10 dB/decade, -20 dB/decade, and so on.
2. The intersections of the slope lines define the corresponding values of Δf_L and Δf_U for each region, where $\Delta f_U > \Delta f_L$. Measure/estimate the phase noise power at these frequency points (in dBc, in a 1 Hz bandwidth) to obtain β_U and β_L for each end point of the region.
3. For each region, calculate A_{α} using:

$$A_{\alpha} = \frac{\left(10^{\frac{\beta_L}{10}} - 10^{\frac{\beta_U}{10}}\right) \cdot (\Delta f_U \cdot \Delta f_L)^{\alpha}}{\Delta f_U^{\alpha} - \Delta f_L^{\alpha}} \quad (2.23)$$

4. Calculate the area of each region using the appropriate form of ***Equation (2.22)***.
5. Sum the areas and multiply the sum by 2. This gives σ_{ϕ}^2 , the integrated phase noise power in rad^2. Take the square root of this value to get RMS phase noise.

Method 2:

Method 2 is not only an alternative method for estimating total phase noise from spectrum analyzer measurements, it can be used to estimate total phase noise power for a VCO using data sheet values given for fixed offsets from the carrier.

1. Measure the phase noise at selected frequency points on the phase noise PSD. Though the spacing of these points is not critical, decade spacing is sufficient. Closer spacing improves accuracy but also increases the number of computations. The selected measurement points constitute region boundaries, Δf_U and Δf_L, where $\Delta f_U > \Delta f_L$. The measured powers at the boundary points are β_U and β_L (in dBc, in a 1 Hz bandwidth).
2. For each region, calculate α: $\alpha = \frac{\beta_L - \beta_U}{10\log\left(\frac{\Delta f_U}{\Delta f_L}\right)}$. (2.24)

Using α, calculate A_{α} for the region: $A_{\alpha} = \Delta f_L^{\alpha} \cdot 10^{\frac{\beta_L}{10}}$. (2.25)

3. Using α and A_{α} for the region, calculate the area using the appropriate form of ***Equation (2.22).***
4. Sum the areas from step 3 and multiply the sum by 2. This gives σ_{ϕ}^2 , the integrated phase noise power in rad^2. Take the square root of this value to get RMS phase noise.

An example of Method 1 using ***Figure 2.11*** is shown in ***Table 2.2***. ***Table 2.3*** contains an illustration of Method 2, based on the marker values shown in ***Figure 2.11.***

Table 2.2 Method 1, Estimation of RMS Phase Noise from Linearized PSD

α	β_L	A_α	f_L	f_U	Area
1	-75	3.223E-06	100	2000	9.66E-06
0	-90	1.00E-09	2000	20000	1.80E-05
3	-90	8.000E+03	20000	6000000	1.00E-05
0	-160	1.000E-16	6000000	20000000	1.40E-09
				Total phase noise power (rad^2)	7.53E-05
				Integrated phase noise (dBc)	-41.23
				Estimated RMS phase noise (rad.)	8.68E-03
				Measured RMS phase noise (rad.)	7.74E-03
				% error	12%

Table 2.3 Method 2, Solving for α and A_α From Measured Values

f_L	f_U	β_L	β_U	α	A_α	Area
100	1000	-75	-86.7	1.2	6.918E-06	6.03E-06
1000	10000	-86.7	-90	0.3	2.089E-08	1.17E-05
10000	100000	-90	-113	2.3	1.585E+00	7.31E-06
100000	1000000	-113	-137.3	2.4	7.079E+00	3.37E-07
1000000	20000000	-137.3	-160	1.7	5.478E-04	2.23E-08
					Total phase noise power (rad^2)	5.09E-05
					Integrated phase noise (dBc)	-42.94
					Estimated RMS phase noise (rad.)	7.13E-03
					Measured RMS phase noise (rad.)	7.74E-03
					% error	-8%

Comparing the estimated values with the measured value displayed by the spectrum analyzer, it can be seen that the estimated values are reasonably close, within +12 % and -8% of the measured value. One can also calculate an estimate with each method and take the average.

The topic of using a spectrum analyzer to measure phase noise deserves some discussion of certain measurement issues [17]. These issues can be loosely classified into two categories: instrument limitations and measurement limitations. These will be briefly introduced below. The reader is encouraged to consult the references listed at the end of this guide for more detailed exploration of phase noise measurement techniques.

17 P. Goyal, "*Theory and Practical Considerations for Measuring Phase Noise Better than -165 dBc/Hz: Part I,*" Microwave Journal, October 2004.

Instrument Limitations

Noise Floor of the Spectrum Analyzer - The spectrum analyzer itself is noise-limited in its measurement capability, i.e., its own noise floor can prevent it from measuring very low levels of noise. Since low levels are typically at offsets far from the carrier, the spectrum analyzer will be more accurate (less self-limited) measuring phase noise close-in to the carrier, and less accurate at offsets farther from the carrier, especially when the oscillator noise density is within 10 dB of the spectrum analyzer noise density. The spectrum analyzer user manual should be consulted to verify the analyzer's noise performance, which may vary depending on the measurement mode.

Resolution bandwidth – Older spectrum analyzers suffer from limited resolution bandwidth, in that they typically do not support resolution bandwidths of 1 Hz, which is the bandwidth in which phase noise is specified. However, ignoring other limitations to measurement accuracy, this particular handicap can be compensated by normalizing the power measured using a higher resolution bandwidth to a 1 Hz bandwidth using the following equation:

$$P(dBc/Hz) = P(dBc/RBW) - 10\log(RBW) \quad (2.26)$$

Simply stated, the phase noise power at some offset Δf_m from the carrier, normalized to a 1 Hz bandwidth, can be found by taking the level measured by a spectrum analyzer at Δf_m using a resolution bandwidth of RBW Hz, and subtracting 10log(RBW) from the measured value. The implicit assumption is that the noise is flat within the band $\Delta f_m \pm \frac{RBW}{2}$. While this is not strictly true, it is a reasonable assumption and does not adversely skew the measurement results. One note of caution is that measurements at frequencies less then one RBW away from the carrier will be biased. If measuring this close to the carrier is necessary, then another measurement method, as described in the references, may be more appropriate.

Equivalent noise bandwidth – Another factor associated with the limitations of resolution bandwidth filters is the concept of equivalent Noise Bandwidth (NBW). Given the output power of flat noise passed through some filter function H(f), the equivalent NBW filter is a rectangular filter (perfectly flat magnitude response and brick wall sides) whose area is equal to that of H(f) and therefore, passes the equivalent output power for flat noise. This is illustrated in ***Figure 2.13***. Consequently, the ratio of the equivalent NBW to the 3 dB BW of H(f) is not 1:1. Because H(f) passes power outside its 3 dB bandwidth, the latter must be narrower than the equivalent NBW. Hence, the ratio is always greater than 1:1. This also means that the noise power passed by the RBW filter is in excess, strictly speaking, of the power attributed to its bandwidth. Thus, a correction factor is applied to the measured power. For example, if the ratio of the equivalent NBW to RBW is 1.2:1, then the correction factor is -1.6 dB. Consult the spectrum analyzer user's manual to find the correction factor for equivalent NBW.

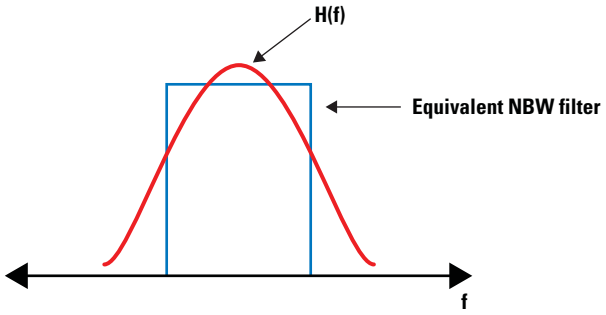


Figure 2.13 Gaussian Filter with Equivalent Noise Bandwidth Filter

Measurement Limitations

Detector response to noise – Spectrum analyzers may employ several different types of detectors. The detector output is a voltage whose level is proportional to the power of the input signal at the tuned frequency. Different detectors are better suited to different measurement scenarios. One must be aware of the detector being used and its response to noise. Many spectrum analyzers use a voltage envelope detector as part of the power measurement path. The true power in a noise signal is the time-averaged square of the voltage divided by the impedance, or:

$$P_{noise} = \frac{1}{T}\int_0^T \frac{v^2(t)}{R}dt \qquad (2.27)$$

However, because an envelope detector output is proportional to the voltage envelope v, squaring the envelope and averaging it is not the same as averaging the square. If the noise is Gaussian, its voltage envelope has a Rayleigh probability density function. The average voltage is proportional to its standard deviation, and is $\sigma\sqrt{\frac{\pi}{2}}$ [18]. However, the true average power (into R ohms) is $\frac{2\sigma^2}{R}$. The log ratio of the power computed from the average voltage envelope to the true average power is -1.05 dB. Hence, the power value obtained from the envelope detector under-estimates true power by 1.05 dB. Consequently, we would add this factor to measurements made with a spectrum analyzer using an envelope detector.

Logarithmic averaging – Another potential distortion of the noise power measurement is due to the log domain power display. Because noise measurements are "noisy", we often put the spectrum analyzer in averaging mode in order to get a stable measurement result. When a spectrum analyzer is operating in log domain mode, it may perform averaging of the logarithmic power values, rather then linear values. In this case, it can be shown that again, the true power is under-estimated, in this case by 2.5 dB [19].

Given these limitations, spectrum analyzer manufacturers often include built-in compensation factors. If a special noise measurement mode is available in the spectrum analyzer, it may automatically apply these corrections to the measured noise value reported to the user. The spectrum analyzer user's guide or manual should be consulted to verify the analyzer's noise measurement compensations.

Jitter and Phase Noise

Engineers that work in the world of oscillator design, precision timing, RF communications, and related specialties are usually concerned with the frequency domain characterization of phase noise and its value at specific offsets from the carrier. Engineers that work in the world of data communications more often work in the time domain and instead prefer jitter as the performance metric. Referring to ***Figure 2.14,*** jitter may be comprised of two primary components: bounded (or deterministic) jitter and unbounded (or random) jitter. Random jitter is directly related to phase noise that we have covered to this point. Because it is the aggregate result of stochastic noise processes, phase noise is quantified as an RMS value, and so, it is logical to extend this treatment to random jitter. On the other hand, deterministic jitter exhibits behavior that is predictable and repeatable, therefore, the range of the maximum phase deviations due to this type of jitter can be bounded and expressed as a peak-to-peak value. Peak-to-peak value is used because the probability of occurrence of the extremes of the range is 1 (one) within some finite time interval, so the designer knows that this design case is certain. Normally, deterministic jitter is not intrinsic to PLL/VCO outputs, i.e, random jitter is the dominant component. Because deterministic jitter is more often associated with clocked data streams, it will be covered in the chapter on Data Clocking.

18 A. Papoulis. *Probability, Random Variables and Stochastic Probability Processes.* McGraw Hill, New York, 1984.
19 Agilent Technologies, *Spectrum Analyzer Measurements and Noise,* Application Note 1303, 2002.

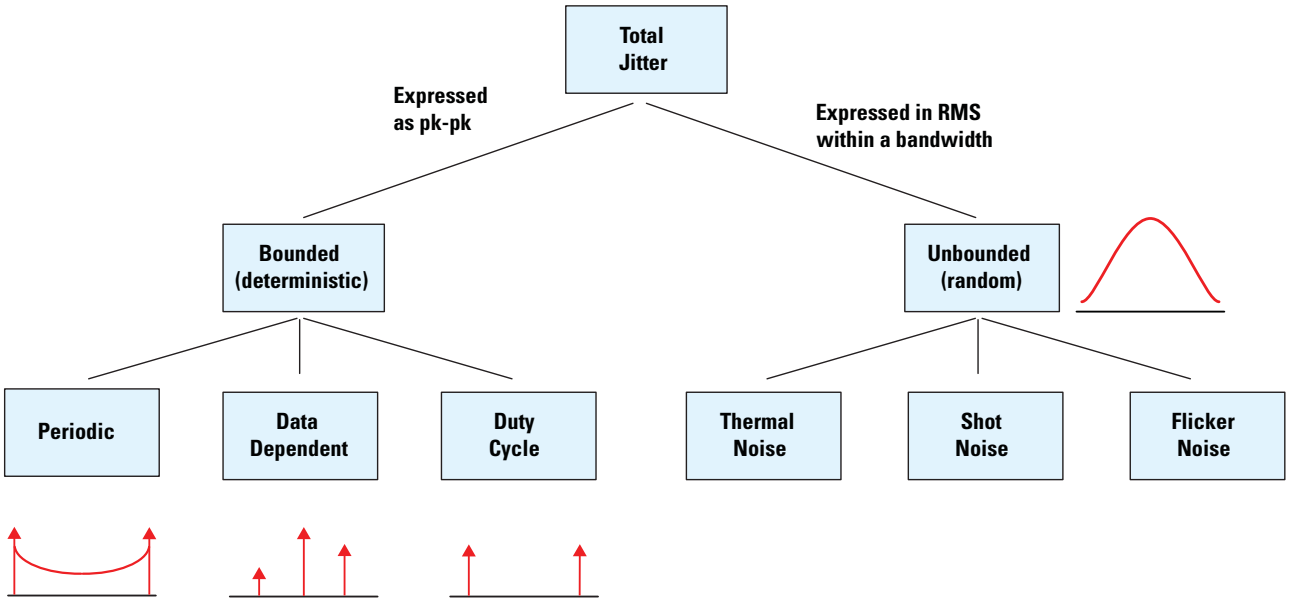


Figure 2.14 Jitter Family Tree

In ***Figure 2.14*** we see that deterministic jitter can be caused by phenomena such as data patterns, periodic components usually coming from interferers and spurious signals, and circuit non-linearities that can cause duty cycle distortion. These will be discussed in more detail in the Data Clocking chapter.

Jitter Definitions

In this section, we review some of the common jitter definitions. Different definitions exist for the purpose of establishing relevant metrics for different applications. Both the maximum and standard deviation statistics can be used with each of these jitter definitions. [20] is one source of formal definitions, some of which are presented below. They are not specific to deterministic or random jitter. As a starting point, a working definition for jitter is "short-term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time."[21] Long term variations are usually referred to as drift or wander and are not discussed in this section. Because we are concerned not just with digital signals but with clock signals in general, the word "clock' can be easily substituted for "digital" in the previous definition without distortion of the interpretation. These short term variations can be interpreted in different ways, as demonstrated in the following definitions.

Cycle-to-Cycle Period Jitter – This jitter is the variation in the cycle time of a signal between adjacent cycles. It is measured over an extended but finite time duration containing multiple cycles. ***Figure 2.15*** illustrates how this form of jitter is measured

20 JEDEC Standard JESD65B, "Definition of Skew Specifications for Standard Logic Devices," September 2003.
21 C. Miller and D. McQuate, "Jitter Analysis of High-Speed Digital Systems," *Hewlett-Packard Journal*, February 1995, attributed to the predecessor to the International Telecommunications Union, the International Telegraph and Telephone Consultative Committee.

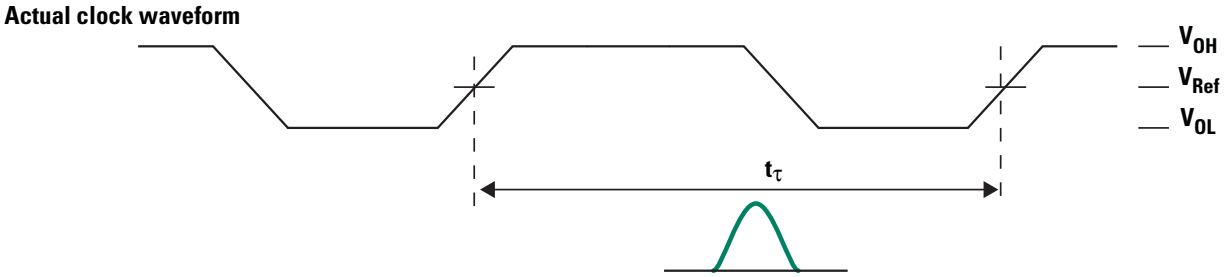


Figure 2.15 Cycle-to-Cycle Period Jitter

Period Jitter – Period jitter is the deviation of cycle time of a clock signal with respect to the ideal period, measured over a finite time duration containing multiple cycles. It is very similar to cycle-to-cycle period jitter, except that it has a deterministic component. For example, if the period of the actual clock waveform was consistently 5% high for every single period, then this would increase the period jitter, but not the cycle-to-cycle period jitter. ***Figure 2.16*** illustrates this definition.

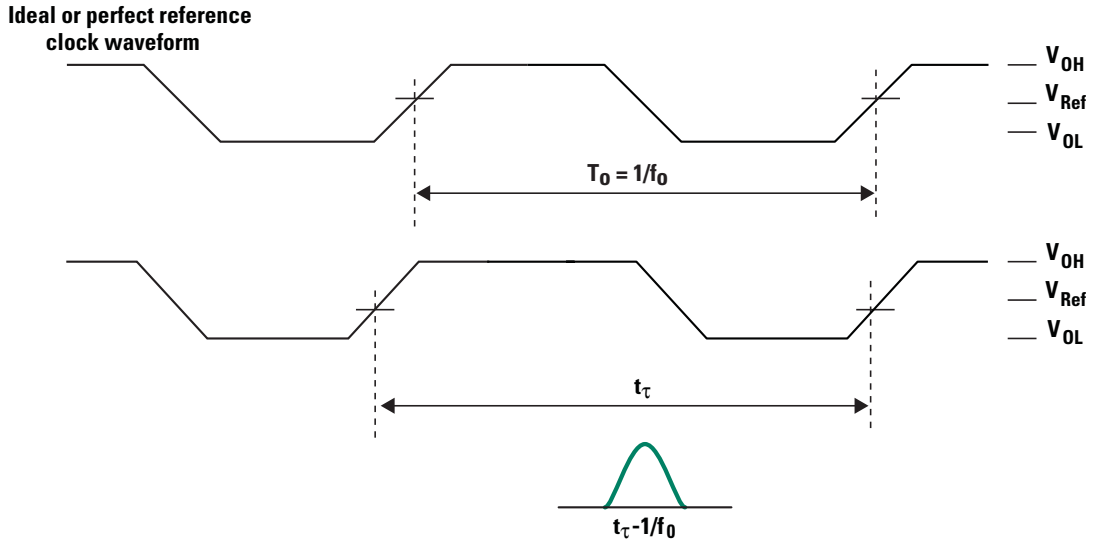


Figure 2.16 Period Jitter

Duty Cycle Jitter – This is the magnitude of the variation in the time duration between the rising edge and falling edge of the clock signal, where the rising edge and falling edge cross a defined threshold. ***Figure 2.17*** illustrates this definition.

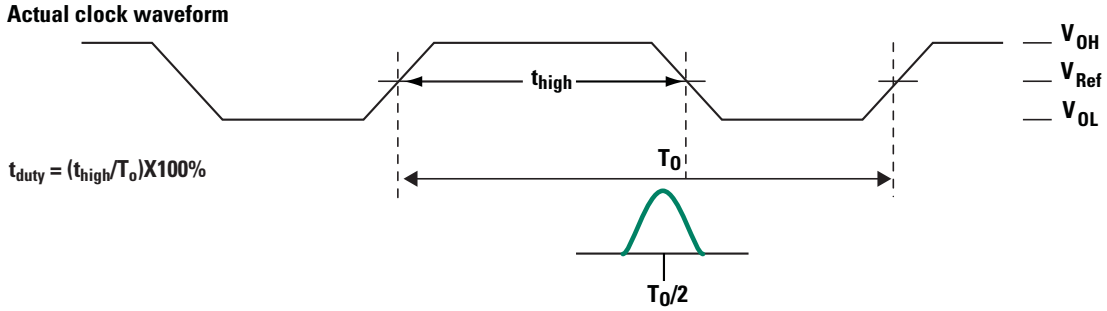


Figure 2.17 Duty Cycle Jitter

Accumulated Jitter – Accumulated jitter is the time displacement of a clock edge which is n cycles from its triggering edge, relative to the edge of an ideal or reference clock also displaced by n cycles relative to the trigger. Mathematically it is given by:

$$t_{ACC}(n) = (\Sigma T_{PER}(n)) - n/f_0,$$

$T_{PER}(n)$ is the rising edge of the n-th period of the clock under observation, and f_0 is the ideal reference clock frequency.

Figure 2.18 illustrates this concept.

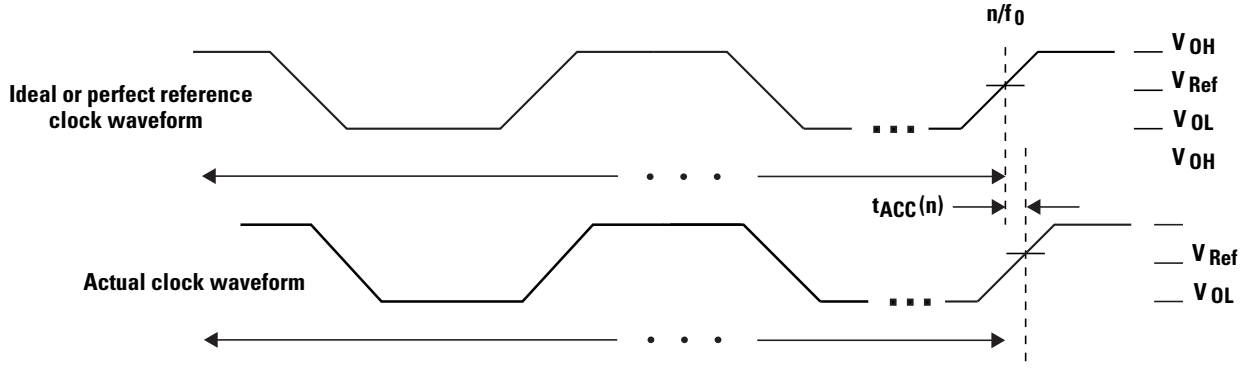


Figure 2.18 Accumulated Jitter

Phase jitter: The deviation in static phase offset $t_{(\phi)}$ for a controlled edge with respect to the mean value of $t_{(\phi)}$ in a random sample of cycles. The following figure illustrates this definition.

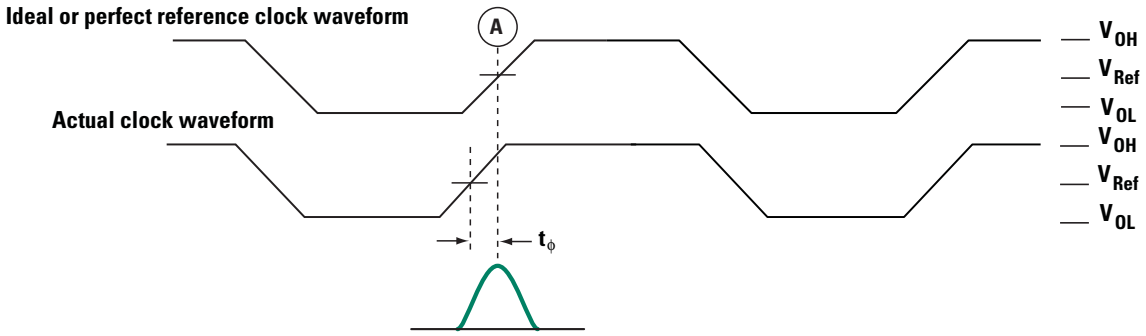


Figure 2.19 Phase Jitter

Though the waveforms shown in ***Figure 2.15*** through ***Figure 2.19*** are representative of digital clock waveforms, the definitions pertain to any periodic signal. In ***Figure 2.19*** a perfect or ideal clock is shown in the upper waveform, while a real-world clock is represented by the lower waveform. The reference edge of the ideal clock is denoted "A", and is used to define the phase jitter appearing in the real world waveform. Consequently, the phase jitter is the instantaneous deviation of the actual clock edge at some defined level (usually the zero crossing or V_{Ref} for a differential clock) from the location established by the ideal clock at the same level. The lower Gaussian-shaped curve depicts how the timing jitter value t_ϕ might be distributed about the reference edge if observed over a long period of time. Though an ideal clock will never exist in a real system, it can be statistically inferred by taking an average of the clock's period over a significant number of cycles. We expect the phase jitter to be zero-mean random process, so a "best-fit" waveform with a period equal to the statistical average thus becomes the virtual reference clock.

Despite the variety of definitions available to us, when each of these types of jitter is viewed through the lens of an "eye" diagram, they all appear as deviations from the ideal or expected threshold crossing point that constitutes the reference edge for the bit boundaries. Hence, in the remaining material in this chapter, the discussion will treat jitter in this way, without reference to a particular definition.

The jitter that we are concerned with here is phase jitter due to phase noise. The relationship between phase noise and jitter can be derived by manipulating a modified version of ***Equation (2.6)***, considering for the moment only the explicit impact of phase noise:

$$v(t) = V_0 \sin(\omega_0 t + \phi_N(t)) = V_0 \sin\left(\omega_0 (t + \frac{\phi_N(t)}{\omega_0})\right) = V_0 \sin\left(\omega_0 (t + \tau_j)\right)$$

$$\therefore \tau_j = \frac{\phi_N(t)}{\omega_0} = \frac{\phi_N(t)}{2\pi f_0} \qquad (2.28)$$

Equation (2.28) says that jitter is related to phase noise by a scalar factor, this being the inverse of the carrier frequency (in radians). The RMS jitter is easily found because it is simply the square root of the phase noise variance from ***Equation (2.18)*** scaled by the inverse of the carrier:

$$\sigma_j = \frac{\sqrt{\sigma_\phi^2}}{\omega_0} = \frac{\sqrt{\int_{f_L}^{f_H} S_\phi(f)\, df}}{\omega_0} \qquad (2.29)$$

Note that the value of RMS jitter is dependent on the integration limits of the phase noise PSD and on the oscillator frequency. Hence, given a jitter specification for an oscillator or clock conditioner, the specification should be accompanied by the integration bandwidth and the center frequency. Without these, it is impossible to compare the performance between two clock conditioners based on a single jitter specification. Referring back to ***Figure 2.9***, the displayed RMS phase noise measurement is 7.74 milliradians. The carrier frequency is 2 GHz, so this yields an RMS jitter value of 615 femto seconds.

Summary

In this chapter, we have examined noise as it affects the performance of oscillators. A mathematical model was presented, showing how noise appears as modulation sidebands in an oscillator frequency spectrum. We then derived the noise response in a simple oscillator model. For PLL/VCO circuits, we considered at a qualitative level how noise injected at different points in the PLL is shaped by specific transfer functions. This led to the conclusion that by analyzing the PLL transfer functions from potential noise sources to the VCO output, we can predict the range of noise frequencies that appear at the output. This also gave us guidance on the importance of noise characteristics of the major functional blocks in the PLL.

We next considered a model of the composite noise at the VCO output, and based on this model, examined two different methods for estimating total phase noise power based on measurements captured by a spectrum analyzer. Finally, we showed how phase noise and jitter are related and introduced some common jitter definitions.

Chapter 3
Phase-Locked Loop (PLL) Fundamentals

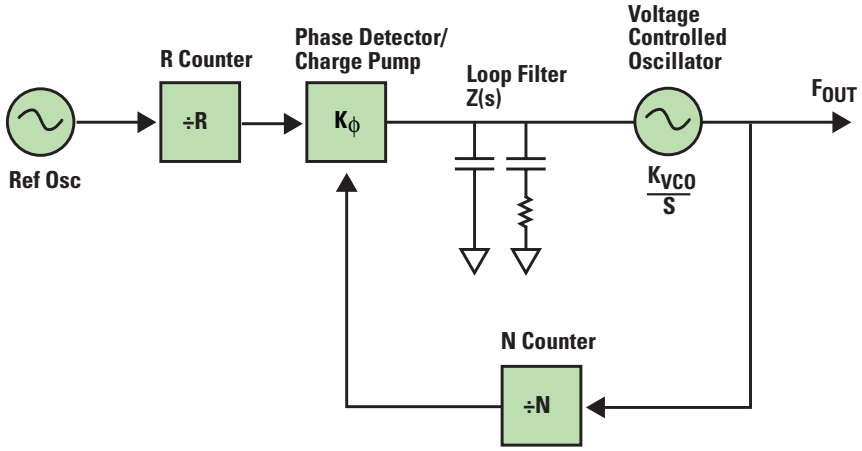


Figure 3.1 The Basic PLL

Basic PLL Operation and Terminology

In this chapter, we address the use of a Phase Locked Loop (PLL) to create a tunable frequency source from a fixed reference. This is accomplished using a VCO (Voltage Controlled Oscillator), which is a voltage to frequency converter. The output frequency of the VCO is divided by N and compared to the reference oscillator frequency, F_{ref}. The Phase Frequency Detector/Charge Pump (PFD) compares these two frequencies and puts out current correction pulses proportional to the phase and frequency difference between the two signals. The correction pulses from the PFD are filtered by the loop filter, which converts them into a voltage to steer the VCO frequency and phase. The N and the R counters are typically programmable. The output frequency, F_{OUT} is given by the following equation.

$$F_{out} = \frac{N}{R} \cdot F_{ref} \qquad (3.1)$$

Loop Filter

The loop filter is fundamental to PLL design and performance and therefore merits discussion. The loop filter is typically not fully integrated as are the other functional blocks due to the fact that it must be optimized for each design. The *order* of the loop filter is defined as one plus the number of non-zero poles. A second order loop filter is shown in ***Figure 3.2.***

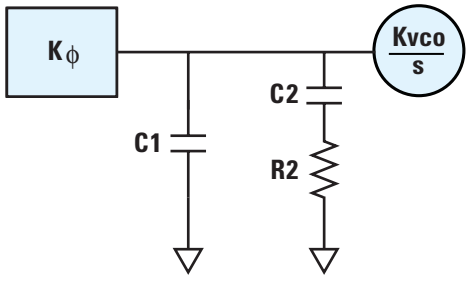


Figure 3.2 Typical Loop Filter Topology

In ***Figure 3.2,*** the transfer function of the passive loop filter can be calculated as follows:

$$Z(s)=\frac{1+s\cdot T2}{s\cdot(C1+C2)\cdot(1+s\cdot T1)}=\frac{1+s\cdot C2\cdot R2}{s\cdot(C1+C2)\cdot\left(1+s\cdot\frac{C1\cdot C2\cdot R2}{C1+C2}\right)} \quad (3.2)$$

In the above equation, the following time constants are defined:

$$T2=C2\cdot R2 \quad (3.3)$$

$$T1=\frac{C1\cdot C2\cdot R2}{C1+C2} \quad (3.4)$$

In general, the loop filter transfer function can be expressed in the following form:

$$Z(s)=\frac{1+s\cdot T2}{s\cdot A0\cdot(1+s\cdot T1)\cdot(1+s\cdot T3)\cdot(1+s\cdot T4)} \quad (3.5)$$

Equation (3.5) is for a 4th order loop filter. ***A0*** is the sum of the capacitor values in the loop filter, ***T2*** is the loop filter zero, and ***T1, T3,*** and ***T4*** are the loop filter poles. Note that in the case that the loop filter is less than 4th order, some of the poles may be zero.

Other Loop Transfer Functions

The open loop transfer function is defined as the transfer function from the phase detector output to the output of the PLL (F_{OUT}). Note that the VCO gain is divided by a factor of *s*. This is to convert output frequency of the VCO into a phase.

$$G(s)=\frac{K\phi\cdot K_{VCO}\cdot Z(s)}{s}$$

$$s=j2\pi f$$

$$|G(s)|=\frac{K\phi\cdot K_{VCO}\cdot|Z(s)|}{2\pi f} \quad (3.6)$$

Note that |G(s)| is a decreasing function in *f*; in other words, as the frequency increases, |G(s)| decreases. The feedback path contains the N counter, so the transfer function in the feedback path is:

$$\boldsymbol{H}=\frac{1}{\boldsymbol{N}} \quad (3.7)$$

Chapter 2 introduced a PLL/VCO model that included noise sources. This model is reproduced in *Figure 3.3.*

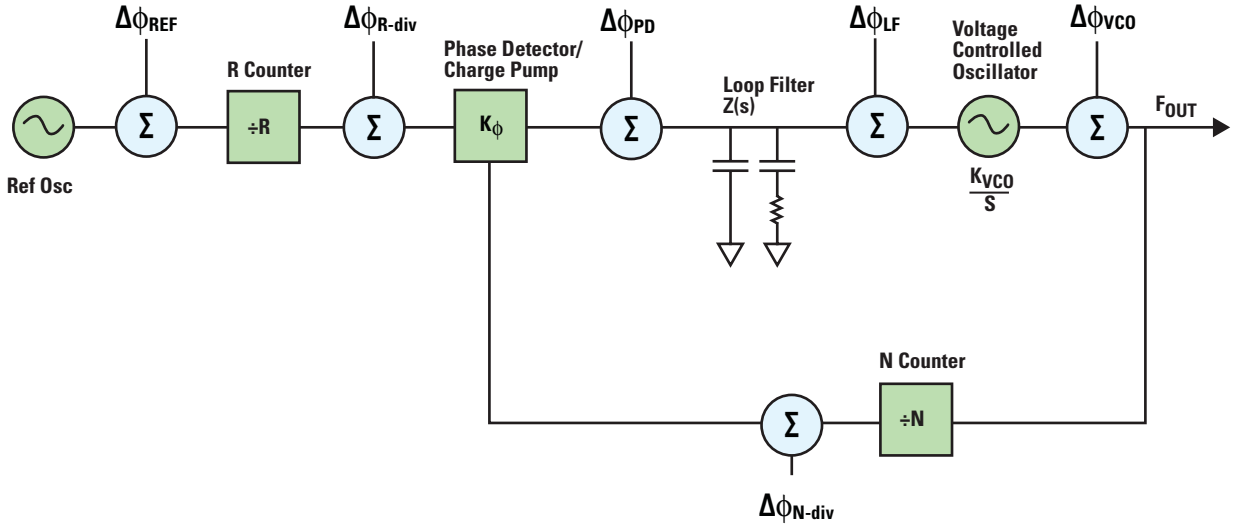


Figure 3.3 VCO/PLL Model with Noise Sources

If one considers noise sources as shown at the VCO, Reference oscillator, R divider, N divider, and phase detector, then the resulting noise at the VCO output can be derived as shown in ***Table 3.1,*** which contains the noise transfer function for each possible injection point. In this table, all sources of the VCO share a same common term, the closed loop transfer function:

$$CL(s) = \frac{G(s)}{1 + G(s) \bullet H} \qquad (3.8)$$

Table 3.2 Transfer Functions for Various Parts of the PLL

Source	Transfer Function	Low Frequency Approximation	High Frequency Approximation
VCO	$\frac{1}{1 + G(s) \bullet H}$	1/G(s)	1
Reference Oscillator	$\frac{1}{R} \bullet CL(s)$	N/R	G(s)
R Divider	$CL(s)$	N	G(s)
N Divider	$CL(s)$	N	G(s)
Phase Detector	$\frac{1}{K\phi} \bullet CL(s)$	N/K_ϕ	G(s)

Note that the reference oscillator transfer function has a factor of *1/R* and the phase detector transfer function has a factor of *1/Kϕ*. The phase detector noise, *N* divider noise, *R* divider noise, and the reference noise are all low pass functions that contain the common factor *CL(s)* in their transfer functions. The VCO is the only block that has a high pass transfer function. The cutoff frequency that determines what is considered low frequency and high frequency is called the loop bandwidth and will be discussed in greater depth later in this chapter.

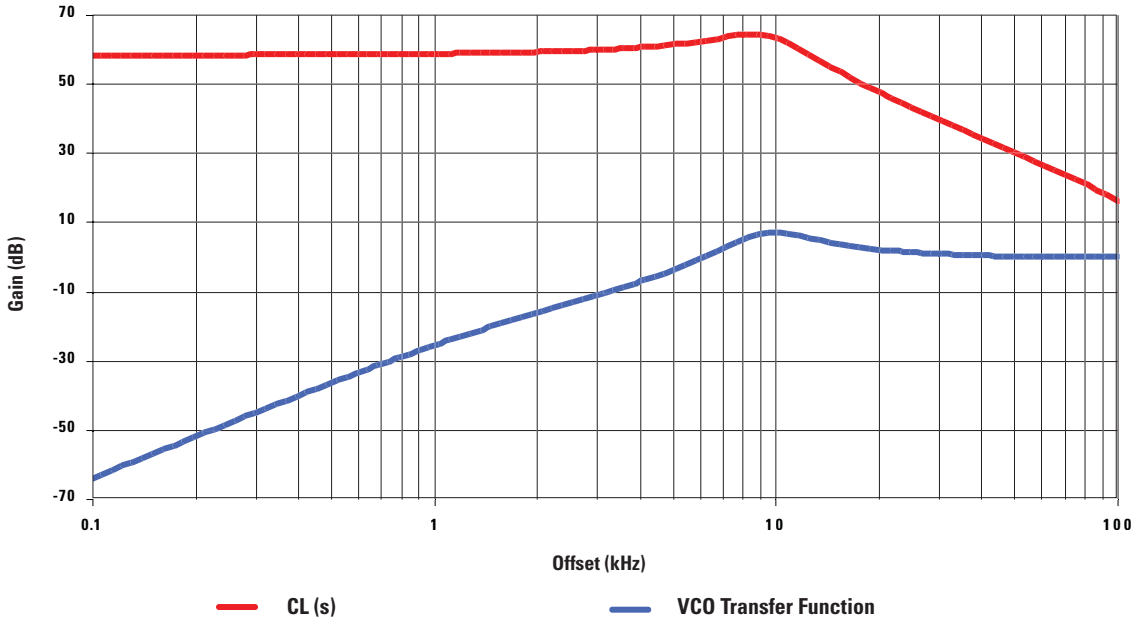


Figure 3.4 Transfer Functions

Properties of PLL Transfer Functions- Loop Bandwidth, Phase Margin, and Gamma

There are a few important figures of merit for the transfer function that are both useful in understanding the PLL design as well as designing the PLL. In order of importance, loop bandwidth, phase margin, and gamma are three properties of PLL transfer functions that are useful in their understanding, and necessary for their design. This section discusses these parameters.

Loop Bandwidth

Definition and Importance of Loop Bandwidth

The function in *Equation (3.8*) is important because it determines the loop bandwidth. Looking at the denominator of *Equation (3.8)*, it should be intuitive that since the function |G(s)| is monotonically decreasing, the loop bandwidth,ω_c, is defined as the frequency that satisfies the following constraint.

(3.9)

$$\left\| G(j \cdot \omega_C) \cdot H \right\| = 1$$

where the operator || * || is the norm operator, in this case equivalent to magnitude.

Table 3.1 contains a low frequency approximation and a high frequency approximation for each of the transfer functions. The loop bandwidth determines what is considered low frequency and high frequency. In Chapter 2, we explained that the phase noise appearing at the VCO output was the combined, shaped noise from all sources illustrated in *Figure 3.3*. Because the transfer function of *Equation (3.8)* appears in most of the noise transfer functions, it will influence the power spectral density of the combined noise sources appearing at the VCO output, $S_\phi(f)$. This is one reason that loop bandwidth is important. Recall that the integrated phase noise (total phase noise power), σ^2_ϕ, is the integral of the power spectral density of the noise at the VCO output over some frequency interval $[f_L, f_H]$:

(3.10)
$$\sigma_\phi^2 = \int_{f_L}^{f_H} S_\phi(f)\,df = 2 \cdot \int_{f_C}^{f_H} L_\phi(f)\,df$$

In *Figure 3.4*, the loop bandwidth is approximately 10 kHz. The loop bandwidth has a large impact on the performance. The lock time is defined as the time that it takes for the PLL to change from one frequency to another to a given tolerance. This lock time is inversely proportional to the loop bandwidth. Although simulations give a more accurate result, a good rule of thumb is:

(3.11)
$$\textit{Lock Time (in seconds)} \approx \frac{4}{\textit{Loop Bandwidth (in Hz)}}$$

Loop Bandwidth Impact on Spurs

For a given phase detector comparison frequency, as the loop bandwidth is made wider to decrease the lock time, then spurious noise caused by the PLL will increase. Simulations are necessary to get a good estimate but a very coarse rule of thumb is that the spurs caused by the PLL will increase by 12 dB for every doubling of the loop bandwidth.

The designer should take note that not all spurs are cause by the PLL. They can be caused by noise on the VCO power supply line, spurs on the reference oscillator, or by EMI. For these other types of spurs, narrowing the loop bandwidth may not necessarily improve the spurs.

Loop Bandwidth Impact on Integrated Phase Noise

Looking at *Figure 3.4,* we see that the PLL transfer function is relatively flat for frequencies less than the loop bandwidth and then rolls off. The VCO transfer function increases up to the loop bandwidth and then asymptotically approaches a gain of 1 (or 0 dB). Note that the PLL transfer function rolls off after the loop bandwidth, so eventually, the VCO noise will dominate. Even though the PLL transfer function seems to overwhelm the VCO transfer function, the PLL noise floor is typically far less than the VCO noise so the total shaped PLL noise does not dominate everywhere.

To really understand this concept, one first needs to know the frequency where the unshaped PLL noise and the free-running VCO noise intersect. The phase noise due to the unshaped PLL noise corresponds to an infinite loop bandwidth. The phase noise due to the free-running VCO noise corresponds to a loop bandwidth of zero Hz.

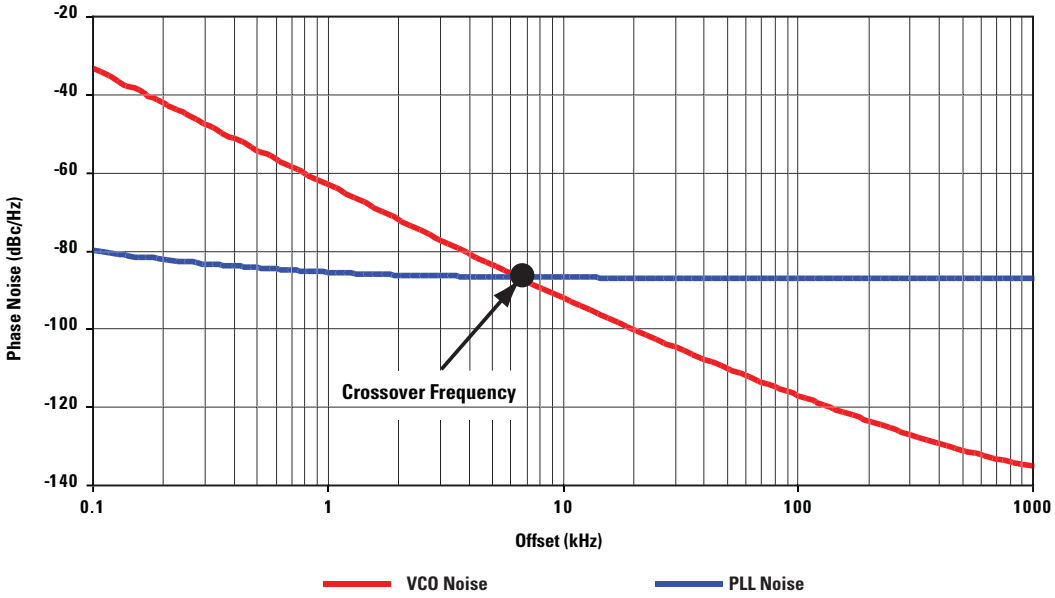


Figure 3.5 Unshaped PLL and VCO Noise

In ***Figure 3.5*** the frequency where the VCO and PLL noise are equal is about 6.3 kHz. This is the crossover frequency. If the VCO noise is unchanged and the PLL noise improves, this frequency becomes larger. If the VCO noise improves and the PLL noise remains unchanged, the crossover frequency becomes smaller. Once the crossover frequency point is known, then the impact of the loop bandwidth on phase noise can be understood.

For example, if the metric of interest is phase noise at a certain offset, and this offset is less than this crossover frequency, then increasing the loop bandwidth improves the phase noise, because it decreases the VCO noise contribution. If this phase noise offset was greater than this crossover frequency, then decreasing the loop bandwidth improves the phase noise, since it decreases the PLL noise contribution. In ***Figure 3.6,*** the crossover point is 6.3 kHz. Note that when the loop bandwidth is less than 6.3 kHz, the phase noise at offsets less than 6.3 kHz is degraded relative to the case of having a 6.3 kHz loop bandwidth, but it is improved for offsets greater than 6.3 kHz. The reverse is true when the loop bandwidth is greater than 6.3 kHz.

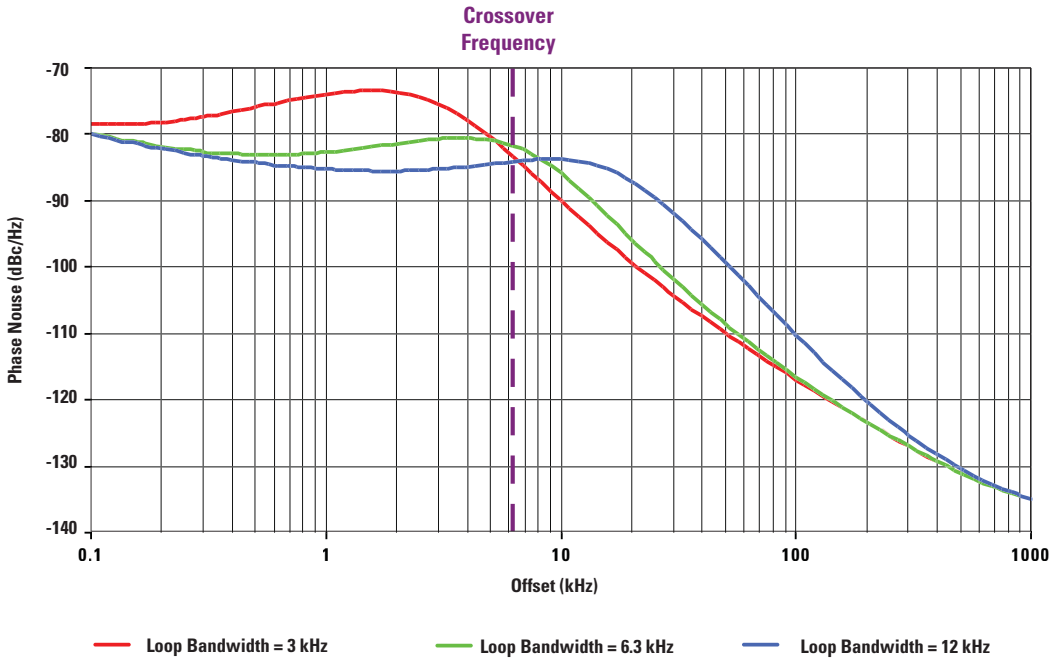


Figure 3.6 Impact of Loop Bandwidth on Phase Noise

The case in which the loop bandwidth is the crossover frequency (6.3 kHz in this case) is approximated by the minimum area under the curve. This integrated phase noise is also very important to performance and can be interpreted in terms of jitter or RMS phase error (σ_ϕ). There are lower and upper integration limits that can apply, which are specific to the application. If we simply model the PLL transfer function as a low pass brick wall function that cuts off sharply at the loop bandwidth frequency, and the VCO transfer function as a high pass function that starts at the loop bandwidth, it follows that designing for a loop bandwidth equal to this crossover frequency would minimize the area under the curve and therefore minimize jitter and RMS phase error.

In reality, the transfer function is not a brick wall function, and it is very difficult to analytically predict the impact of noise from sources such as the phase detector or reference oscillator, so a simulation is the best tool for understanding how to optimize under these conditions. In practice, it often turns out that making the loop bandwidth about 20% wider than the crossover frequency accounts for most of these factors. This bandwidth of interest that minimizes the integrated phase noise as defined by the application will be referred to as the optimal integrated noise bandwidth. ***Figure 3.7*** shows a full simulation that accounts for the true shaping of the loop filter. In this example, it turns out that the minimum RMS phase error loop bandwidth, which corresponds to the minimum integrated noise bandwidth, is around 8 kHz, as opposed to the crossover point value of 6.3 kHz. It also shows that if one is going to err, it is better to err on the side of being too wide.

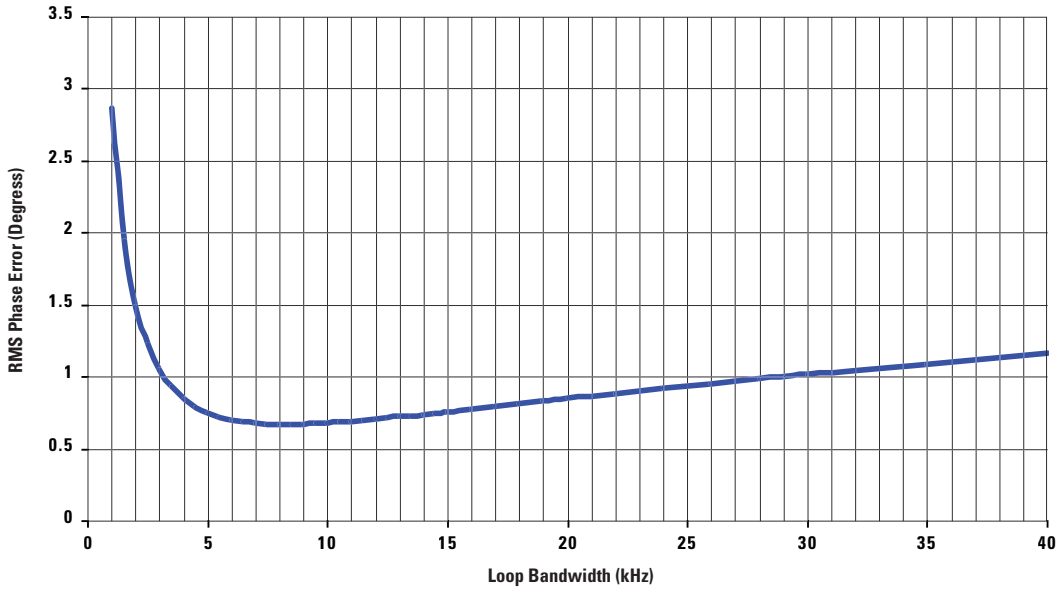


Figure 3.7 RMS Phase Error vs. Loop Bandwidth

If the limits of integration for the integrated phase noise quantity are not zero to infinity, then this can change this optimal loop bandwidth. If the lower limit is greater than the crossover frequency, then minimizing the loop bandwidth optimizes the phase noise. If the upper limit is less than the crossover frequency, then maximizing the loop bandwidth optimizes the integrated phase noise. If the crossover frequency falls between the minimum and maximum integration limits, then a simulation or more detailed analysis is required to determine the optimal loop bandwidth.

Design Limitations for Loop Bandwidth

Aside from the design trade-offs discussed above, there are also design limitations on how narrow and how wide the loop bandwidth can be.

1. Minimum Loop Bandwidth Limitation Due to Capacitor Sizes
   As the loop bandwidth approaches zero Hz, the loop filter capacitors approach infinity. The capacitor sizes are inversely proportional to the square of the loop bandwidth. Because there are practical limitations on how large capacitors can be, this sets the lower limit on how narrow the loop bandwidth can be. If the phase detector frequency or the charge pump current are decreased, this decreases the capacitor sizes and allows one to get a narrower loop bandwidth with the same capacitor sizes.

2. Minimum Loop Bandwidth Limitation Due to Lock Time Degradation
   Although narrowing the loop bandwidth is understood to increase the lock time, if it is made two narrow, the lock time can be further degraded beyond this due to capacitor dielectric issues and cycle slipping. As capacitance increases, the quality of the dielectric material tends to be worse. Bench measurements show that NP0 and Film type capacitors tend to have no degradation in lock time due to these effects, but X7R, X5R, and Tantalum can have significant degradations in lock time.

   A second issue with narrow loop bandwidths is called cycle slipping. If the comparison frequency is more than about 100 times the loop bandwidth, a phenomenon known as cycle slipping also can further degrade the lock time from what one would expect.

3. Maximum Loop Bandwidth Limitation Due to Capacitor and Resistor Values
   Because loop filter capacitor values are inversely proportional to the loop bandwidth, as the loop bandwidth increases, the capacitor values become very small. At some point, the VCO input capacitance and board parasitics will dominate the loop filter capacitors, so for a robust design, the capacitor value closest to the VCO should be kept at least 4X the VCO input capacitance value.

   The loop filter resistor values are proportional to the loop bandwidth. At some point, they might become unrealistically large and parasitic leakages could overwhelm the value. But a much greater consideration is the thermal noise. This thermal noise is proportional to the square root of the resistor value and adds to the other noise sources. It often has the greatest impact near the loop bandwidth frequency of the system.

4. Continuous Time Approximation Effects
   Recall that the phase detector puts out discrete pulses of current, which have a duty cycle proportional to the phase error presented to the phase detector. Provided that the loop bandwidth is $1/10^{th}$ of the phase detector frequency or less, then it is sufficient to model the charge pump as a continuous current. This is known as the continuous time approximation, and is used as a basis for the design equations. As a rule of thumb, if the loop bandwidth is between $1/10^{th}$ and $1/5^{th}$ of the phase detector frequency, the PLL will still lock, but the performance might be a little different than predicted by simulation. If the loop bandwidth is more than $1/5^{th}$ of the phase detector frequency, not only will the measured results likely be off from simulation, but at some point, the PLL will not lock at all.

Loop Bandwidth Criterion for Different Applications

Because the choice of loop bandwidth can involve trade-offs between lock time, spurs, reference noise, and integrated phase noise, there is no one loop bandwidth that is optimal for every application. And even for a given application, things like the PLL spur performance and the VCO noise performance can impact the most desirable loop bandwidth. That being said, ***Table 3.2*** shows some typical criterion for loop bandwidths for various applications.

Table 3.3 Typical Applications and their Implication on Loop Bandwidth

Application	Driving Factors for Loop Bandwidth Consideration	Typical Loop Bandwidth Criterion
Cellular Telephones	Lock time, spurs	Choose loop bandwidth to meet lock time requirements with margin, but not larger, because spurs are also very important
GSM Basestation	RMS phase error, spurs	Optimal integrated noise bandwidth
Jitter Cleaners	Minimize noise from reference source	Loop bandwidth must be narrow enough to reject noise on the reference.
CDMA Basestation	Minimize RMS phase error at an offset greater than the crossover frequency. Minimize phase noise at far offsets	Narrow loop bandwidth, but still has lock time requirements (5 kHz is a typical value)
A/D Converters	Minimize jitter from 0 Hz to infinity	Optimal integrated noise bandwidth
Clock Multipliers	Minimize jitter from 0 Hz to infinity	Optimal integrated noise bandwidth

Phase Margin

Definition of Phase Margin

At the loop bandwidth, the magnitude of GH is 1, but the phase is important too. If this phase is 180 degrees, then the denominator becomes zero and this is sure instability. If one considers ***Equation (3.8)***, then phase margin is defined as:

$$180 - \angle G(j \cdot \omega_C) \cdot H = \phi \tag{3.12}$$

Phase margin also impacts performance, but far less than the loop bandwidth. Although a poor phase margin can cause a design not to lock at all, a constant value of 50 degrees is a good starting point, and design software can be used to fine tune the optimal value.

The phase margin can be related to the damping factor, ζ, of a second order system as shown in the following rule of thumb.

$$\sec \phi - \tan \phi = \frac{1}{4\zeta^2} \tag{3.13}$$

A higher phase margin implies a larger damping factor, and a phase margin of 37 degrees relates to a damping factor of $1/\sqrt{2}$.

Impact of Phase Margin on Performance

For optimal lock time, the phase margin is around 45 degrees. If the phase margin is too low, there will be excessive ringing, or even instability. If the phase margin is too high, there will be no ringing, but the frequency will settle in much slower. ***Figure 3.8*** illustrates this point.

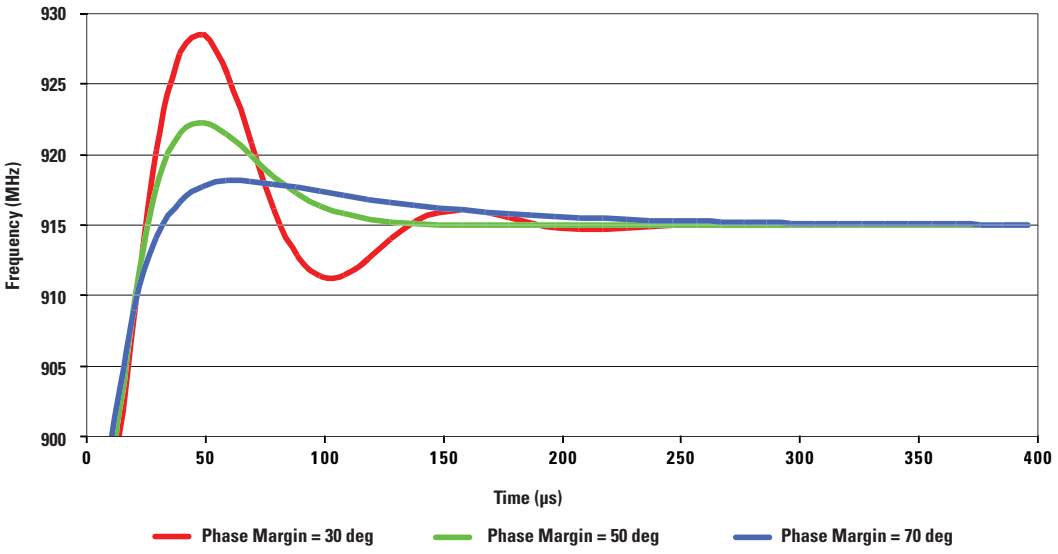


Figure 3.8 Impact of Phase Margin on Lock Time

For designs involving minimizing the integrated phase noise, it is important to try to minimize the peaking in the phase noise near the loop bandwidth. In designs for optimal integrated phase noise, it makes sense to choose something higher, up to 80 degrees. This causes the transfer function to be more flat at the expense of lock time. It also increases the VCO noise suppression near the loop bandwidth (see ***Figure 3.9***). The reason for this is that this peaking can significantly increase the integrated phase noise. The PLL is guaranteed not to work for phase margins of zero degrees or less and 90 degrees or more, so the phase margin should be chosen such that the loop operates somewhere between these points.

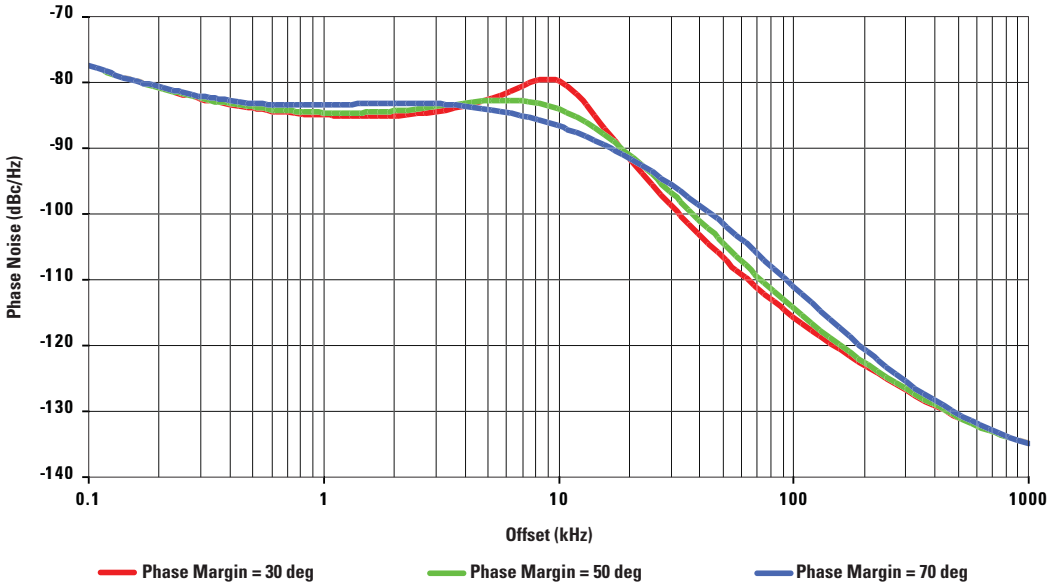


Figure 3.9 Impact of Phase Margin on Peaking and Integrated Phase Noise

In summary, the choice of the phase margin has far less impact than the choice of the loop bandwidth, but it is still important. ***Table 3.3*** gives some guidelines for choosing phase margin.

Table 3.4 Phase Margin Guidelines

Design Target	Phase Margin
Minimum Integrated Phase Noise	Very high, about 80 degrees
Fastest Lock Time	About 45 degrees
General Purpose Applications	About 50 degrees

Gamma Optimization Parameter

The loop bandwidth and phase margin are the most important properties of the PLL transfer function. That being said, there is a third property, γ, which also needs to be specified in order to design the loop filter. This is defined in terms of the loop bandwidth and time constants of the loop filter as follows:

$$\gamma = \omega_C^2 \cdot T2 \cdot (T1 + T3 + T4) \tag{3.14}$$

This parameter is based on the concept of maximizing the phase margin at the loop bandwidth. The gamma optimization parameter, γ, quantifies this property of maximizing the phase margin at the loop bandwidth. Reference [22] suggests that this is a good constraint to apply. ***Figure 3.10*** shows a plot of phase margin and forward loop gain versus frequency for a second order filter and γ=1. The phase margin in this case is approximately 42^0.

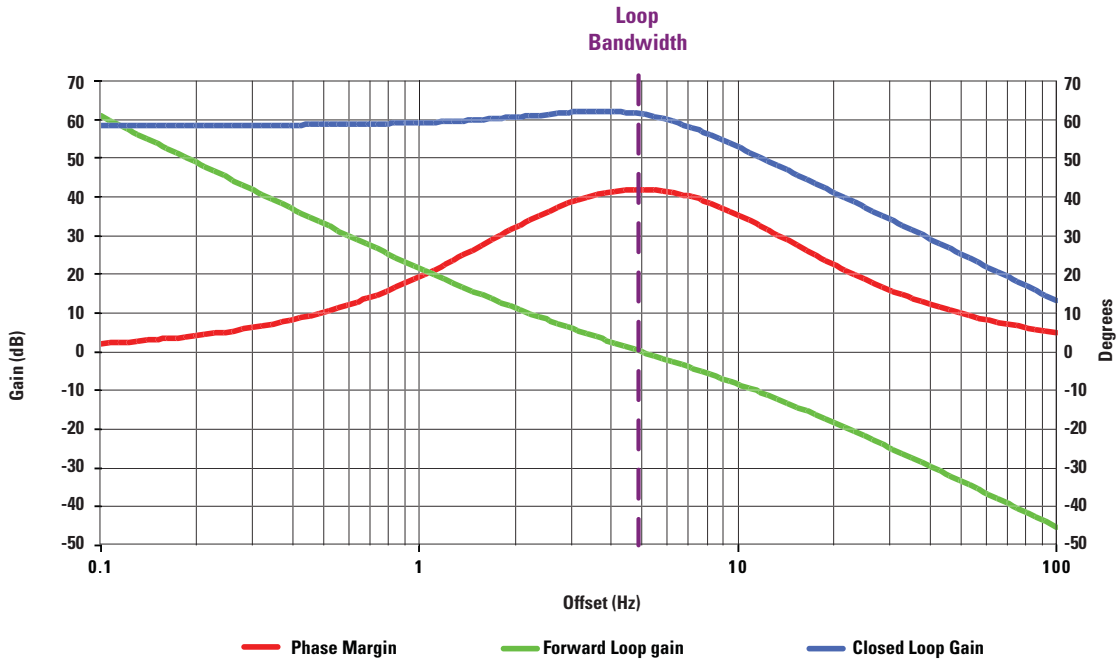


Figure 3.10 Optimizing Phase Margin at the Loop Bandwidth

It turns out that γ=1 is a pretty good rule of thumb for minimizing the switching speed of the PLL for a given phase margin and loop bandwidth. However, it is not exact. By allowing γ values other than one, the lock time can be decreased on the order of 30%, depending on the phase margin. A gamma value slightly greater than one corresponds to maximizing the phase margin at a frequency less than the loop bandwidth, and a gamma value of less than one corresponds to maximizing the phase margin at a frequency greater than the loop bandwidth. The gamma optimization parameter is discussed in greater detail in Reference [23].

In conclusion, choosing the gamma optimization parameter equal to one is a good starting point. ***Table 3.4*** provides a range of gamma values based on the phase margin.

22 W. O. Keese, *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump PLLs.* National Semiconductor Application Note 1001.
23 Dean Banerjee, *PLL Performance, Simulation and Design.* 4th Edition. Dogear Publishers, 2006

Table 3.5 Guidelines for Choosing Gamma

Phase Margin	Recommended Gamma
30	1.40
35	1.41
40	1.29
45	1.09
50	0.94
55	0.85
60	0.70
65	0.49
70	0.24
75	0.05
80	0.08

Loop Filter Design

A Second Order Loop Filter Design

Now that the transfer function parameters of loop bandwidth, phase margin, and gamma optimization parameter are understood, the framework for actually designing a loop filter can be understood. The design of loop filters is actually very involved. National Semiconductor has excellent software for designing and simulating PLL performance [24]. Much more detail on how to design loop filters is given in Reference [23]. Although these tools are very powerful and effective, over dependence on such tools can cheat one of a valuable understanding. This section describes the general process that is followed for designing a loop filter. To start, the topology of a loop filter is shown below:

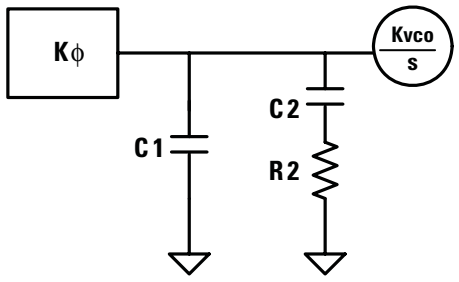


Figure 3.11 Typical Loop Filter Topology

From ***Figure 3.11***, the transfer function of the passive loop filter can be calculated as follows:

$$Z(s)=\frac{1+s\cdot T2}{s\cdot(C1+C2)\cdot(1+s\cdot T1)}=\frac{1+s\cdot C2\cdot R2}{s\cdot(C1+C2)\cdot\left(1+s\cdot\frac{C1\cdot C2\cdot R2}{C1+C2}\right)} \quad (3.15)$$

24 EasyPLL Simulation Tool at wireless.national.com.

In the above equation, the following time constants are defined:

$$T2 = C2 \cdot R2 \tag{3.16}$$

$$T1 = \frac{C1 \cdot C2 \cdot R2}{C1 + C2} \tag{3.17}$$

Applying the constraints developed previously to the phase margin (ϕ) yields the following equation:

$$\phi = 180 - \arg\left(G(s)/N \Big|_{s=j\bullet\omega c} \right) = \arctan(\omega_C \cdot T2) - \arctan(\omega_C \cdot T1) \tag{3.18}$$

Applying the Gamma value (γ) definition, the following constraint is derived

$$T2 = \frac{\gamma}{\omega_C^2 \cdot T1} \tag{3.19}$$

Equations (3.18) and ***(3.19)*** can be combined to express the time constant, T1, in terms of phase margin, loop bandwidth, and Gamma Optimization Factor. After this, the time constant T2, can also be solved for.

$$T1 = \frac{\sqrt{(1+\gamma)^2 \cdot \tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot \tan\phi}{2 \cdot \omega_C} \tag{3.20}$$

Note that there are two time constants, but three components to solve for. The third constraint is the loop bandwidth, which gives the sum of the capacitances in the loop filter, which will be defined as A0.

Applying the constraint of the loop bandwidth yields the following constraint:

$$1 = \left| G(s)/N \right| = \left| \frac{K\phi \cdot Kvco}{N \cdot s} \frac{1 + s \cdot T2}{s \cdot (C1 + C2) \cdot (1 + s \cdot T1)} \right| = \frac{K\phi \cdot Kvco}{N \cdot \omega_C^2 \cdot (C1 + C2)} \frac{1 + \omega_C^2 \cdot T2^2}{(1 + \omega_C^2 \cdot T1^2)}$$

$$\Rightarrow A0 = C1 + C2 = \frac{K\phi \cdot Kvco}{N \cdot \omega_C^2} \frac{1 + \omega c^2 \cdot T2^2}{1 + \omega_C^2 \cdot T1^2} \tag{3.21}$$

Combining ***Equations (3.16), (3.17),*** and ***(3.21)*** yield the solutions for the component values:

$$C1 = A0 \cdot \frac{T1}{T2} \tag{3.22}$$

$$\boldsymbol{C2 = A0 - C1} \tag{3.23}$$

$$\boldsymbol{R2 = \frac{T2}{C2}} \tag{3.24}$$

Choosing the Design Parameters for Higher Order Loop Filters

The design process for third and fourth order loop filters is similar, but more complicated than the 2nd order case and is described in Reference [23]. Because there are additional poles resulting in added components, more constraints can be applied. An example of a 4th order loop is illustrated in ***Figure 3.12.*** ***Table 3.5*** lists the design constraints for loop filter orders 2, 3, and 4.

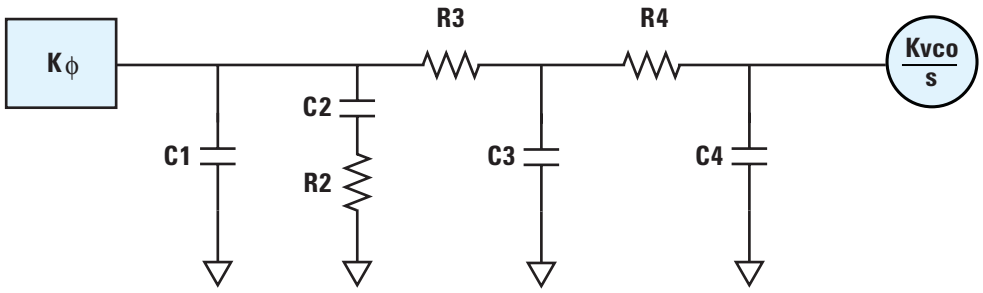


Figure 3.12 Fourth Order Loop Filter Topology

Table 3.6 Loop Filter Time Constants and Specified Parameters

Loop Filter Order	Number of Time Constants	Parameters Needed to be Specified for Passive Filter	Parameters Needed to Be Specified for Partially Integrated Filter
2	2 (T1, T2)	Loop bandwidth Phase margin Gamma	n/a
3	3 (T1, T2, T3)	Loop bandwidth Phase margin Gamma T3/T1 ratio T4/T3 ratio	n/a
4	4 (T1, T2, T3, T4)	Loop bandwidth Phase margin Gamma T3/T1 ratio T4/T3 ratio	Loop bandwidth Phase margin Gamma C3, C4, R3, R4

Setting the pole ratios T3/T1 and T4/T3 equal to one theoretically gives the maximum spurious attenuation, but one of the capacitors will approach zero and one of the resistances will approach infinity. So, this is just a starting approximation. For a third order filter, choosing T3/T1 equal to 0.67 will get one to within 1 dB of the maximum theoretical limit. For a more complete presentation on higher order filters, Reference [23] should be consulted.

In integrated VCO/PLL devices such as National's LMX2531 family of frequency synthesizers, there are partially integrated loop filters, where R3, R4, C3, and C4 are embedded within the device and may enabled or disabled through the device's programming interface. The motivation for partially integrating these components is that it reduces board space, saves components, and has some performance advantages. Specifically, when the VCO is integrated on silicon, the components integrated on silicon can filter noise that external components might not be able to, such as noise internal to the chip or due to crosstalk on the bondwires.

The equations involved in the design of these partially integrated loop filters are quite involved, but covered in Reference [23] and applied in National's free online simulation tool, EasyPLL [24].

The bandwidth of higher order filters is also limited by component values: for example, as bandwidth increases, capacitor C1 approaches zero and eventually equals zero for some finite bandwidth.

Determining Components for Higher Order Loop Filters
As shown for the second order loop filter, constraints can be applied to calculate the time constants. Once the time constants are known, they can be related to the component values. For higher order filters, the formulas are more complicated and will not be presented here (see Reference [23]). For example, in the third order passive filter, there are actually 5 components, but only 3 time constants and a loop bandwidth constraint. That leaves one degree of freedom. This can be fulfilled by imposing the requirement that the capacitor C3 is maximized. For the fourth order loop filter, there are actually two additional requirements that can be specified, giving a total of seven component values but only five constraint equations. One approach is to pick C1 and R3 based upon the design constraints for a 3rd order loop filter. While this balances the constraint equations and the number of components to be selected, a further reduction in order can be achieved by next trying to maximize capacitor C4 to overcome the parasitic capacitance of the VCO input. This also allows R4 to be minimized, which can offer benefits in thermal noise performance.

Active Loop Filters

Often, charge pump gain ($K\phi$) is inadequate to cover the full tuning range of the VCO. To overcome this problem, active filters are sometime used for loop filters to provide additional gain. For active filters, the filter functions will have the same basic form as for passive filters, leading to the same general solutions for the time constants. The calculation of the component values will be somewhat different because the latter combine differently in determining the poles and zeros of filter function. Hence, the appropriate equalities between T1, T2, T3 and T4 and components R1, C1,…,R4, C4 must be re-derived. However, once this is done, the remainder of the process is the same.

One caution about active loop filters: due to their active nature, they will contribute additional noise to the loop, either through internal device noise, or through interference entering on power supply rails. Hence, the designer should choose low noise devices when possible and pay specific attention to design of the power supply interface.

Conclusion

This chapter has introduced some of the fundamental aspects of PLL design and performance. Many of the results in this chapter come from Reference [23], which were used with special permission from the author. Design constraints for loop filters based on loop bandwidth, phase margin, and a gamma parameter were described, and exact solutions for a second order filter were presented.

Chapter 4
Data Converter Clocking

Introduction

In this chapter, we will develop a more applied view of jitter, specifically as it impacts the performance of Analog-to-Digital Converters (ADCs). First, we will develop an intuitive understanding of the impact of jitter on a sampled waveform, and then derive a well known expression for the Signal-to-Noise Ratio (SNR) of a sampled waveform that includes the impact of jitter. Finally, we examine at a qualitative level the impact of sample clock phase noise in a bandpass sampling application.

Figure 4.1 (a) shows an example ADC input waveform (V_{IN}) in the form of an asymmetric trapezoidal pulse. The black dots show the desired sampling points. These points form a distortion-free version of the original waveform. ***Figure 4.1 (b)*** shows shaded regions that represent a range of possible times at which the sample clock edge can occur, assuming that the sample clock has a jitter component. Errant sample locations due to the jitter component are shown as red dots. These points are within the range of possible clock edges but not in the center of the shaded area. ***Figure 4.1 (c)*** re-plots the samples captured with the jittered clock, except they have been repositioned at the correct sampling times, representing the apparent waveform as it would appear in the digital domain (red trace). Each corresponding value on the X-axis is the expected sampling point in time since the data acquisition system has no knowledge of clock noise or any way to compensate for it. As a result, the digital waveform is distorted.

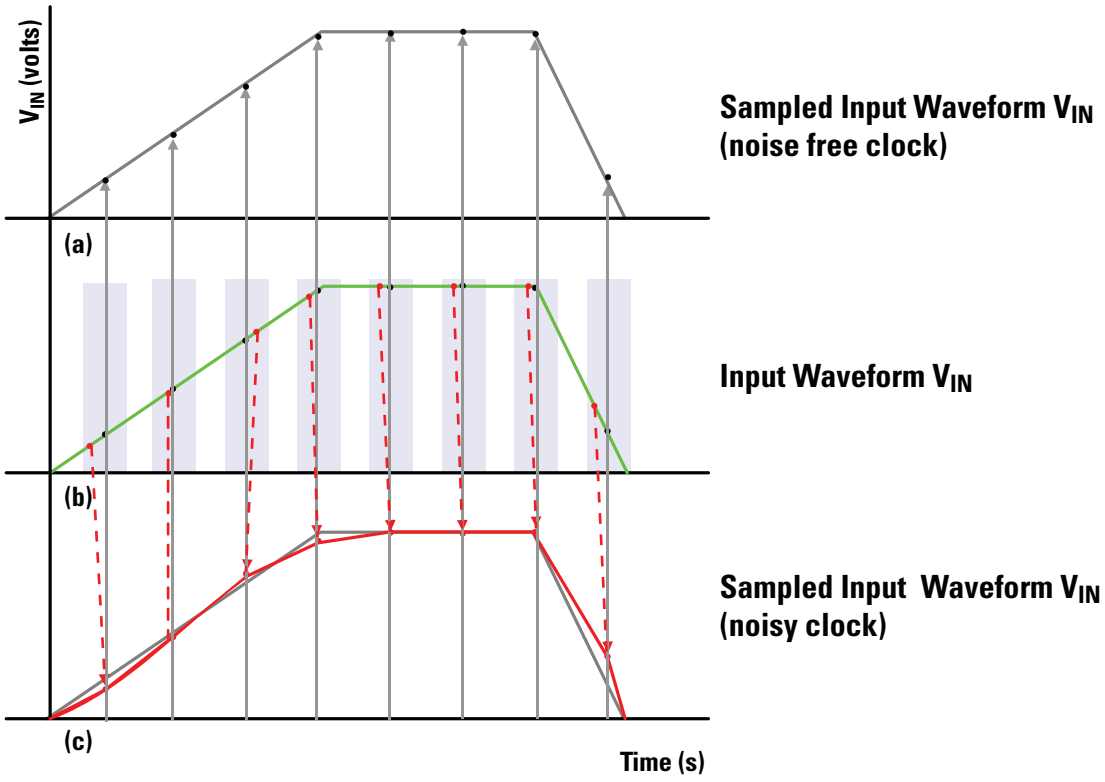


Figure 4.1 Distortion and Clock Jitter

Sampling A Signal – A Time Domain Perspective

The level of importance that the sample clock has on ADC/DAC performance is intuitive; however, it would be helpful to understand how these observations relative to data converter performance parameters. ***Figure 4.2*** shows a simple model of an ADC, along with a small segment of an input waveform and the ADC clock. The desired sample point is shown as the point at which the ADC input switches from track to hold (switch open). The range of likely instances at which the actual sampling point could take place is indicated by the region labeled as Δt. Within this region, the actual sampling instant is $t \pm \tau_j$. Specifically, τ_j represents the clock jitter and is a zero mean random variable with RMS value σ_j. The range of input signal levels that can be observed over the possible sampling interval is labeled ΔV.

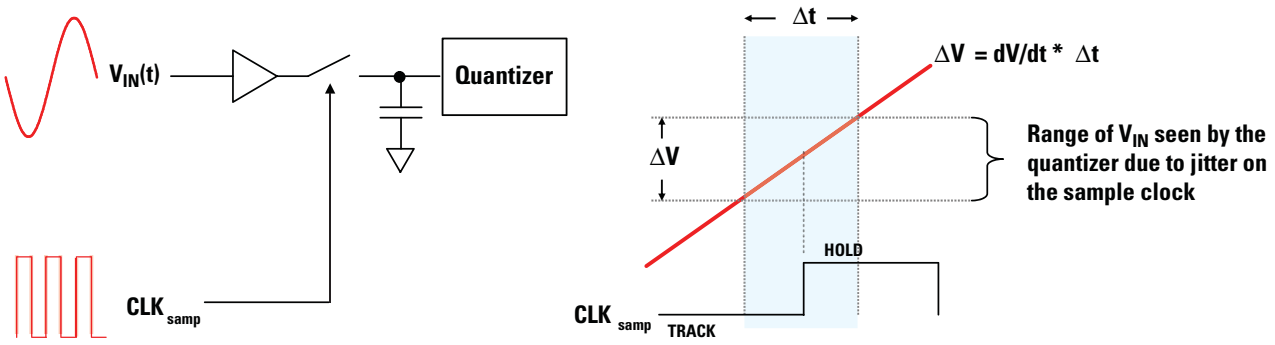


Figure 4.2 Data Converter Sampling Process

Assuming a sinusoidal input for v(t) we have,

$$v(t) = V_o \sin 2\pi f_{in} t \tag{4.1}$$

Because $\Delta t << \frac{1}{f_{in}}$, the derivative with respect to time can be represented by:

$$\frac{\Delta V}{\Delta t} = 2\pi f_{in} V_o \cos 2\pi f_{in} t \tag{4.2}$$

Taking the RMS value of both sides:

$$\frac{\Delta V_{rms}}{\sigma_j} = \frac{2\pi f_{in} V_o}{\sqrt{2}} \tag{4.3}$$

where σ_j = the RMS value of Δt.

The RMS error voltage due to jitter is

$$\Delta V_{rms} = \frac{2\pi f_{in} V_0 \sigma_j}{\sqrt{2}} \tag{4.4}$$

The Signal-to-Noise Ratio (SNR) in decibels is obtained by rearranging ***Equation (4.4)*** and taking the log:

$$SNR = 20\log_{10}\left[\frac{signal}{noise}\right] = 20\log_{10}\left[\frac{V_0/\sqrt{2}}{\Delta V_{rms}}\right] \quad (4.5)$$

Substituting (4.4) into (4.5) gives SNR due to jitter:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{in}\sigma_j}\right] \quad (4.6)$$

Equation (4.6) is an important and well known result. While it was derived for a sinusoidal input at the ADC, it still provides a reasonable estimate of SNR for a broadband signal if the sample rate is significantly higher than the signal bandwidth. Note that the SNR due to jitter is independent of ADC resolution and sample rate, and decreases as the signal frequency increases. The SNR is also independent of the input signal amplitude since the error voltage, as shown in ***Equation (4.4)***, directly scales to the amplitude of the input signal. Consequently, changing the gain in the signal path in front of the ADC has no impact on the SNR due to jitter.

Sampling – A Frequency Domain Perspective

We can supplement the insight developed in the previous section by reviewing the mathematics of the sampling operation. The multiplication of an arbitrary band-limited input signal, x(t), by a train of perfect impulses represents the ideal sampling operation. This process yields a stream of sample values, y(nT), as shown in the following equation:

$$y(nT) = x(t)\cdot\sum_{n=-\infty}^{\infty}\delta(t-nT_S) \Leftrightarrow Y(\omega) = \frac{2\pi}{T_S}\sum_{k=-\infty}^{\infty}X(\omega - k\omega_S) \quad (4.7)$$

Mathematically, multiplication in the time domain is the dual of convolution in the frequency domain. However, a train of ideal impulses in the time domain transforms to a train of ideal impulses in the frequency domain. Convolving this frequency impulse train with the signal spectrum simply results in the familiar periodic signal spectrum of digital signals.

In reality, the sampling waveform is neither a perfect impulse nor is it stable in time. Instead, it is more realistic to consider the final sample voltage as a weighted average of the input signal over some very small time window. However, because we are primarily concerned with the impact of clock jitter, we'll continue to use the impulse as the sampling waveform, but with a jitter term included. If the effect of clock jitter is included, then the delay term in the impulse function includes a random component, τ_j. As in the time domain analysis of the previous section, τ_j is modeled as a Gaussian random process with zero mean and standard deviation σ_j. The sampled signal is now:

$$\hat{y}(nT) = x(t)\cdot\sum_{n=-\infty}^{\infty}\delta(t-nT_S-\tau_j) \Leftrightarrow \hat{Y}(\omega) = \frac{2\pi}{T_S}\sum_{k=-\infty}^{\infty}X(\omega - k\omega_S)\cdot e^{-j(\omega-k\omega_S)\tau_j} \quad (4.8)$$

Comparing ***Equations (4.7)*** and ***(4.8)***, we see that the jitter has introduced a modulation term in the spectrum of the sampled signal. In essence, the term $e^{-j(\omega-k\omega_S)\tau_j}$ results in small, residual spectrum shifts that spread the signal band. ***Figure 4.3*** illustrates the frequency domain effect when the sampled signal is a single sinusoid. The perfect impulse of the input is sampled by an ADC clock with jitter, which causes the clock spectrum to be spread. Hence, the perfect input impulse is spread by the ADC clock during the sampling operation.

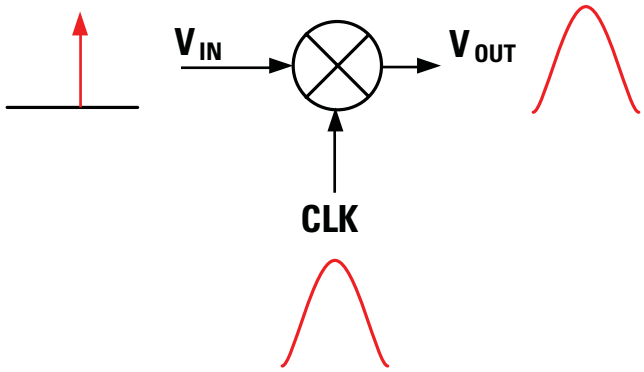


Figure 4.3 Sampling and Mixing

Figure 4.4 illustrates the spectrum of a noiseless sample clock. A sample clock with Gaussian phase noise is shown in *Figure 4.5.*

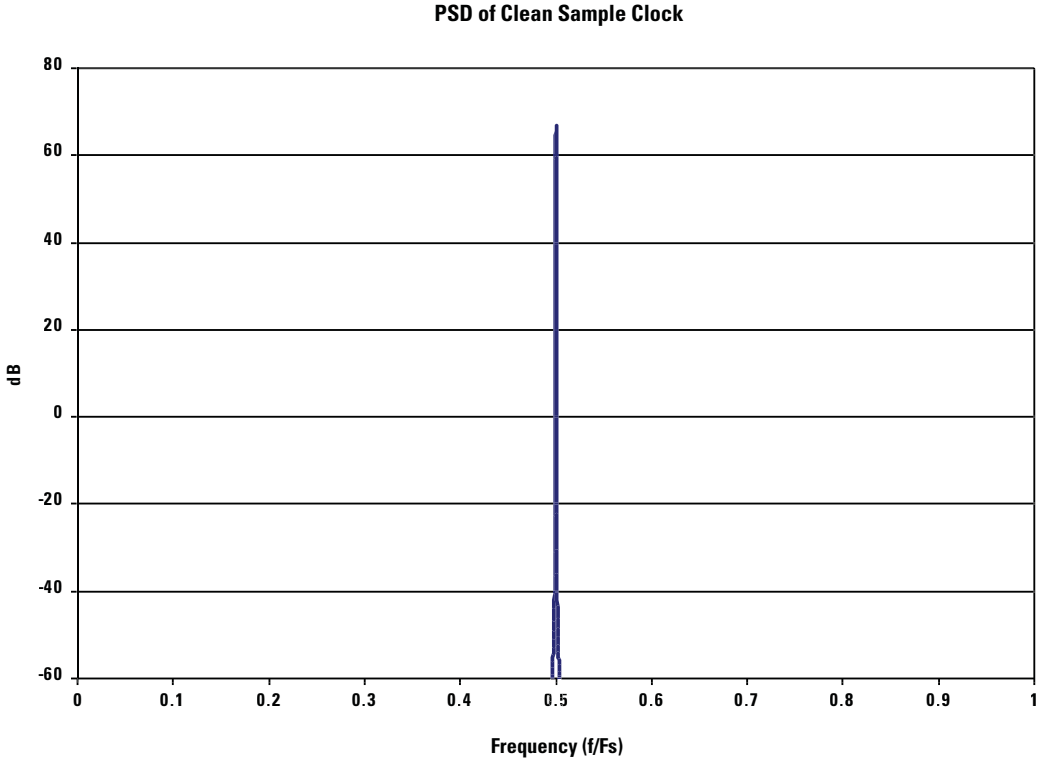


Figure 4.4 Sample Clock PSD without Noise

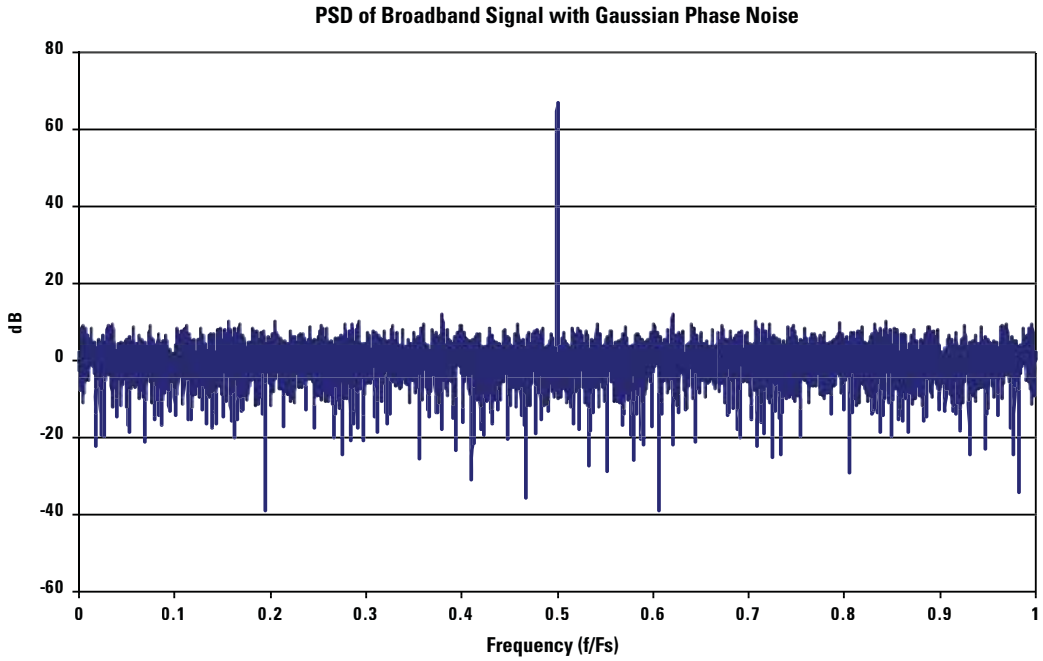


Figure 4.5 Sample Clock PSD with Gaussian Phase Noise

Any signal sampled with the clock shown in ***Figure 4.5*** will not have an SNR any better than that of the sample clock, in this case about 68 dB.

Three key observations can be made with respect to the preceding analysis:

- Even if the ADC is perfect, a noisy sample clock will add noise and undesired distortion. The process of sampling a signal with an ADC is much like the process of mixing in the RF world. Mixing the signal with a noisy clock has the net effect of 'spreading' the desired signals in the frequency domain as well as converting it ***(Figure 4.3).***
- The frequency of the input signal determines the degree of sensitivity to clock noise. Sampling the signal at locations that are changing slowly with respect to time results in smaller sampling error (top of the trapezoid, ***Figure 4.1***). The greater the input frequency, the greater the error generated by a perfect data converter if the sample clock is noisy.
- In essence, ADCs have resolution in two dimensions: the degree of granularity of quantization (determined by the characteristics of the ADC), and, the ability of the data conversion system to consistently sample the signal at precise intervals (determined by the characteristics of the sample clock generation system and to a limited extent intrinsic ADC characteristics).

Bandpass Sampling and the Impact of Clock Noise

At this point, we have quantified the impact of sample clock jitter in terms of SNR and demonstrated how this is embodied in the frequency domain. Mathematically, we saw that jitter has the effect of spreading the signal spectrum, directly adding noise to the signal band. However, because we are dealing with a signal in the digital domain, there is an additional impact that must be considered: the sampling rate with respect to the spectral occupancy of the input signal; and, the sampling rate with respect to the input bandwidth of the ADC. Both can exert further influence the final SNR of the sampled signal.

Nyquist sampling theory tells us that for a baseband signal, the sampling rate must be at least twice the highest frequency component in the signal. If not, aliasing results. However, for bandpass signals, the sampling rate must be at least twice the bandwidth occupied by the signal. Specifically, the sampling rate must satisfy the following inequality:

$$F_s \geq \frac{2 \cdot (B + f_L)}{M + 1}$$

and

$$M = \left\lfloor \frac{f_L}{B} \right\rfloor \qquad (4.9)$$

where B = signal bandwidth
f_L = lowest signal frequency

This is known as *bandpass sampling* or *sub-Nyquist sampling*. A bandpass signal is illustrated in ***Figure 4.6.***

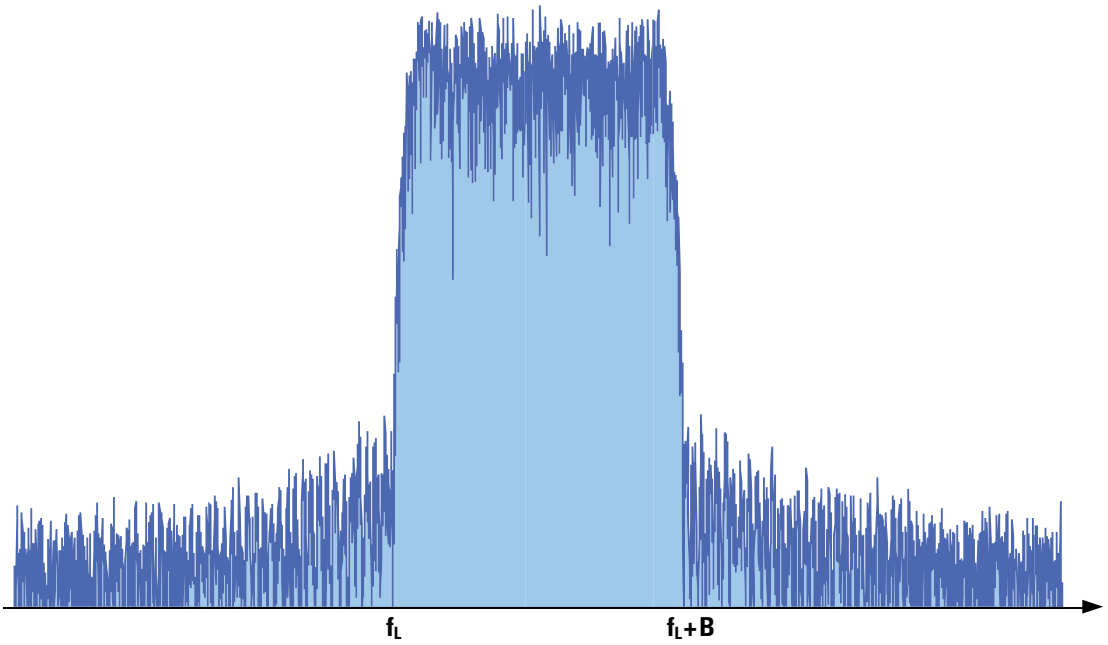


Figure 4.6 Spectrum of a Bandpass Signal

If the signal in ***Figure 4.6*** is sampled at some frequency that satisfies the relationship in ***Equation (4.9)***, then ***Equation (4.7)*** tells us that signal spectrum is periodic in the frequency domain with period F_S. ***Figure 4.7*** contains a plot of a bandpass signal with sampling clock jitter. ***Figure 4.8*** illustrates a bandpass-sampled signal with a noisy clock.

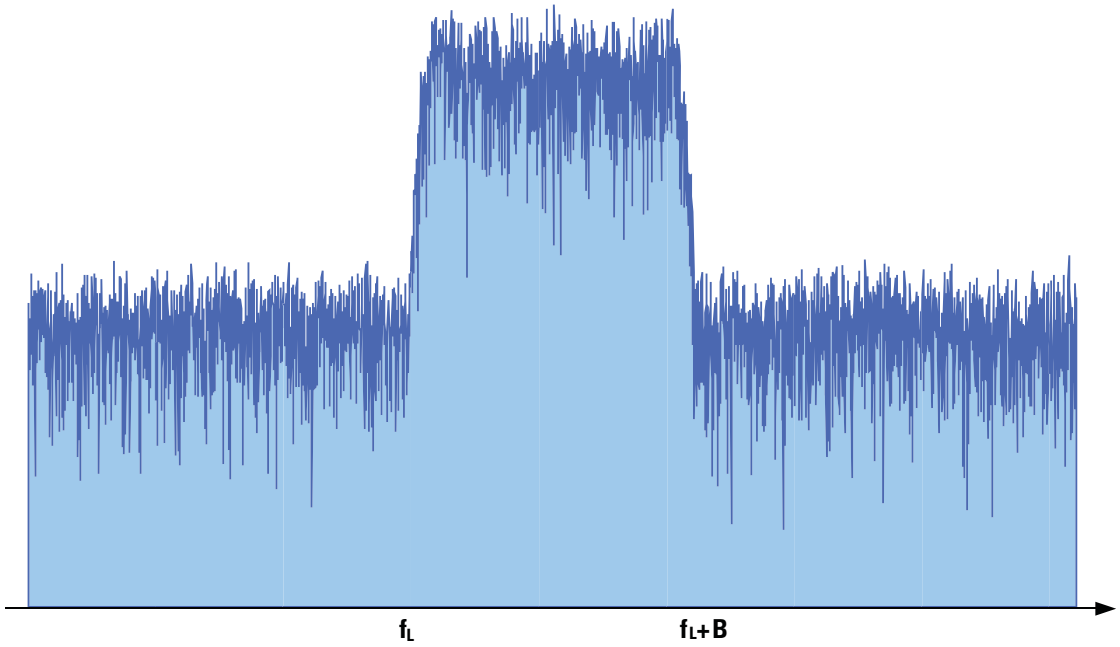


Figure 4.7 Bandpass Signal with Noisy Sample Clock

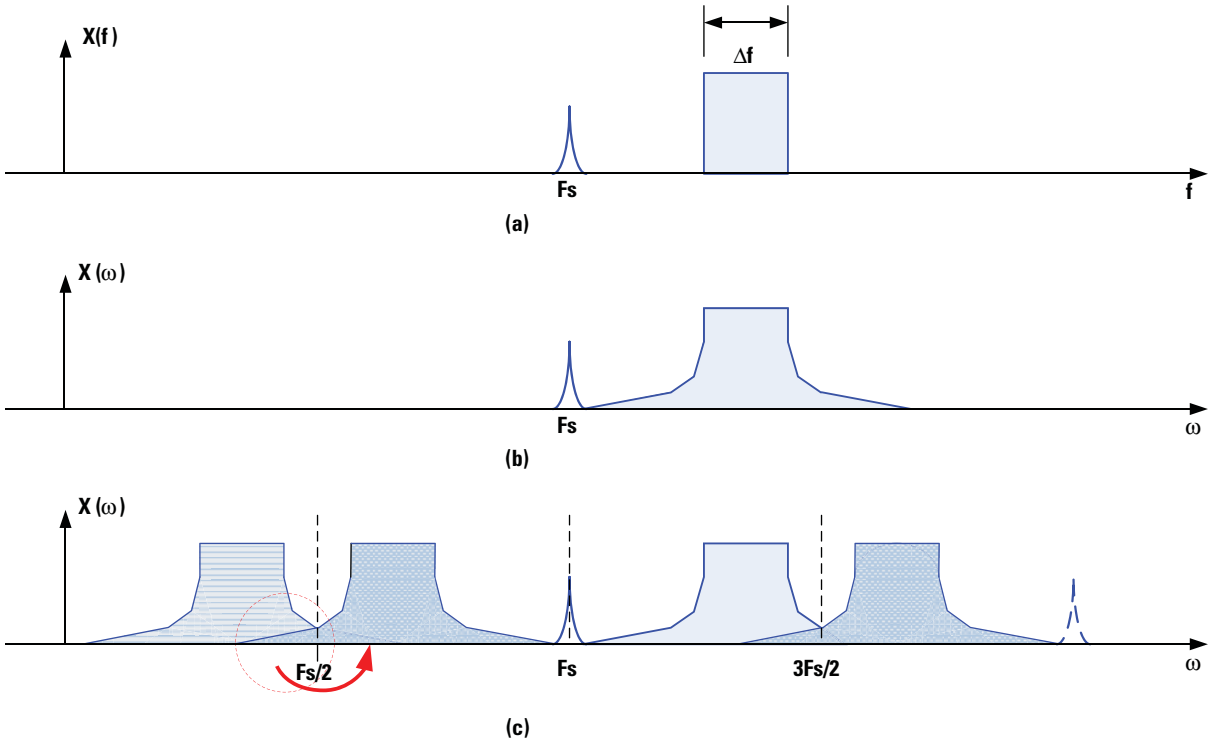


Figure 4.8 Bandpass Sampling

Figure 4.8 (a) through *(c)* illustrates the effect embodied in *Equation (4.8)*. The jitter term modulates the original signal spectrum shown in *Figure 4.8 (a)*, giving the spectrum shown in *(b)*. *Figure 4.8 (c)* shows the digital, jitter-modulated spectrum after bandpass sampling. Jitter has an impact on the signal band in two ways. First, residual spreading caused by the jitter (due to the close-in phase noise of the sample clock) directly degrades in-band SNR. Second, bandpass sampling causes out-of-band noise to be aliased into the signal band, further increasing the noise floor. In *Figure 4.8 (c)*, the out-of-band noise that "crosses" the frequency boundaries that are multiples of $F_s/2$ (marked by the vertical dotted lines) will fold back into the signal band. If this out-of-band noise is high enough, it will significantly raise the noise floor. These combined effects emphasize the importance of both close-in phase noise and phase noise at large offsets from the clock frequency. This effect can be somewhat mitigated by increasing the sampling rate, which would cause the images to be more widely separated in frequency, but the tradeoff is that the number of samples to be processed is increased. However, this may be an acceptable tradeoff in some applications. This example also reinforces the importance of analog filtering in the signal path to limit the out-of-channel noise at the ADC input.

The RMS jitter value σ_j in *Equation (4.6)* is total jitter and comprises two primary components: the intrinsic RMS jitter of the ADC itself and the RMS jitter of the sample clock. These are random and independent in nature, so the total RMS jitter σ_j is calculated by taking the root sum squared of the intrinsic ADC jitter and the jitter of the sample clock:

$$\sigma_j = \sqrt{\sigma_{ADC}^2 + \sigma_{Clk}^2} \qquad (4.10)$$

The "intrinsic" jitter specified in ADC datasheets is usually given in units of seconds, making it easy to calculate the total jitter once the sample clock RMS jitter is known.

Equation (4.6) is plotted in *Figure 4.9* for various fixed values of jitter. Clocks capable of delivering jitter performance well under 1 ps RMS (1 kHz – 30 MHz) are difficult to implement, but are nonetheless available.

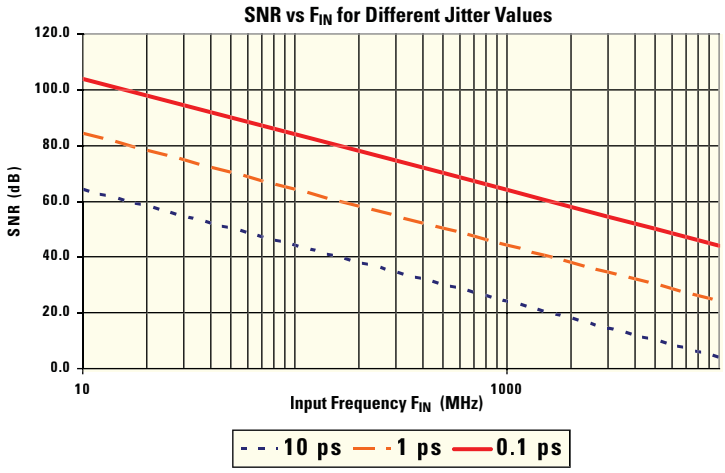


Figure 4.9 Data Converter SNR

Summary

In more and more contemporary applications, ADCs are being used to sample signals of 1 GHz or greater in frequency. In most cases, this is the result of a shift in implementation paradigm, in that operations that were formerly done in the analog domain, such as frequency translation, are now being done in the digital domain. However, this does not mean that SNR requirements have been relaxed. *Figure 4.9* shows that for constant lines of SNR, a 10x increase in the input frequency requires a 10x improvement in RMS jitter (and equivalently, phase noise). Consequently precision clock conditioners become more important in extremely high-frequency sampling applications.

Chapter 5
Data Clocking

Introduction

Backbone data networks have employed serial data links for years, mostly in the optical domain. With the improvement in semiconductor technology that has benefited both digital processing architectures and timing devices, parallel data link formats are quickly being replaced by high-speed serial data links (USB, IEEE 1394, SATA) in the wired domain. Consequently, it is important to examine the impact and relevance of clock conditioners in data-clocking applications. In this chapter, we will briefly examine data-clocking applications and the impact of clock jitter and skew. Understanding the causes of jitter is important because it has a direct impact on Bit Error Rate (BER) of the system.

This chapter is organized as follows: First, we will briefly review certain aspects of the data clocking architecture of data communication systems. Next, a brief discussion of the impact of phase noise/jitter on system performance is presented, followed by the causes and effects of timing skew, skew correction.

Data Communication Systems and Clock Conditioners

All data communication systems have common aspects that the designer must deal with. At the heart of the system is a clock (and its derivatives) that constitutes the means for reliably segregating each information bit at the transmitter and receiver. A data encoding format that aids recovery of the bit clock from the information bit stream is often employed when the receiver and transmitter do not have access to a global clock. ***Figure 5.1*** and ***Figure 5.2*** illustrate a generic architecture at the transmitter end showing how clock conditioners are integrated into the architecture. Though this architecture depicts several parallel and possibly independent data channels being combined, these could be easily replaced by a parallel data interface and a serializer/de-serializer (SerDes) device, as shown in ***Figure 5.3.*** In either case, multiple, parallel source streams running at bit rate FDATA are multiplexed into a single bit stream before injection into the transport channel. The channel may be a satellite link, fiber-optic link, coaxial cable, backplane, or copper trace. For generality, we have shown a band-limiting filter, amplifier and modulator block, although these may not be required in certain applications. Due to the multiplexing of N streams, the multiplexer (SerDes) output stream runs at $N \cdot F_{DATA}$. In order for the multiplexing operation to be error free, the parallel data clocks and multiplexer clock must maintain a fixed phase relationship. In ***Figure 5.3***, the parallel channel clocks and the multiplexer clock are derived from different devices, but are locked to the same reference.

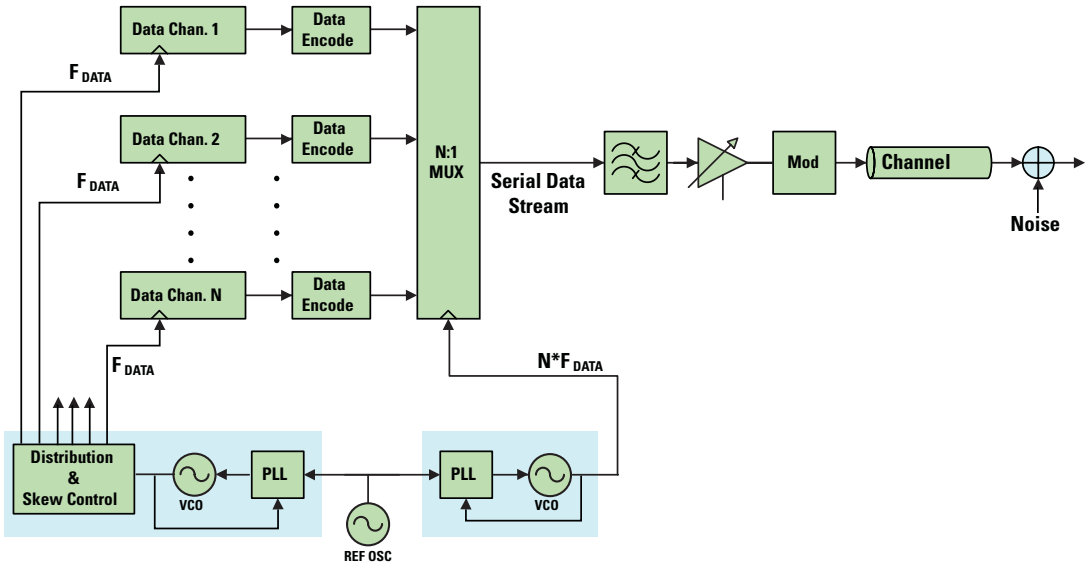


Figure 5.1 Conceptual Model of Transmitting End of a Data Communication System with Clock Conditioners

In *Figure 5.2* and *Figure 5.3*, a single clock conditioner is used to generate the parallel channel clock(s) and the multiplexer (SerDes) clock. The multiplexer clock runs at $N \cdot F_{DATA}$, and the parallel channel clocks are derived from the multiplexer clock via a bank of dividers. In both architectures, key performance specifications of the clock conditioner for the data channels are random jitter (phase noise) and skew (or delay). Jitter appearing on the clock at the transmitter is superimposed on the data.

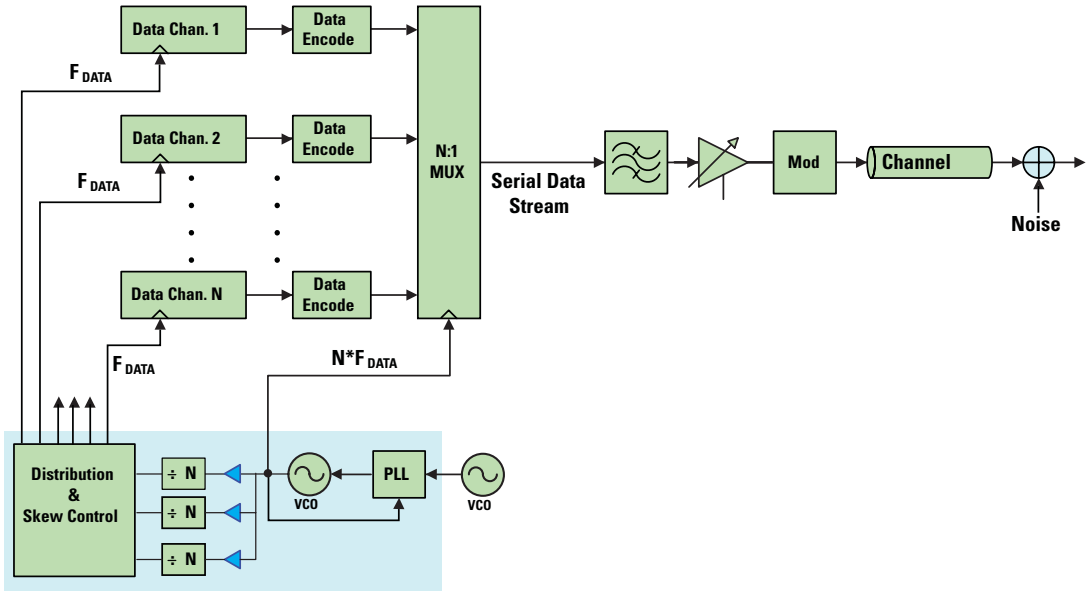


Figure 5.2 Data Communications Transmitter with Alternative Clock Architecture

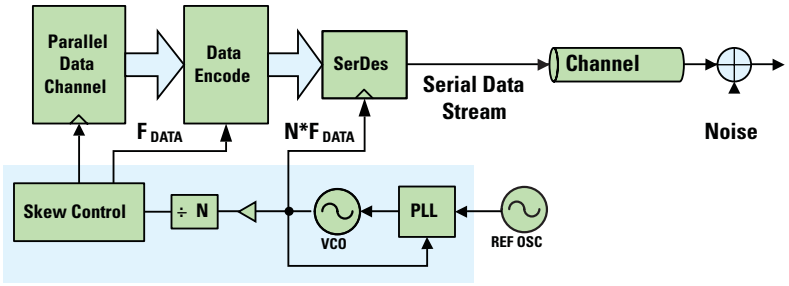


Figure 5.3 Parallel-Serial Data Communications Link

Though the serial data clock rate ($N \cdot F_{DATA}$) may be known at the receiver, the clock phase is not. Most receiver architectures are based on sampling the input signal to regenerate a clean version of the serial stream. Recovery of the bit clock is required in order to reliably detect the true bit values. *Figure 5.4* presents an example of the ideal relationship between a recovered clock and a NRZ bit stream at the receiver. Rationally, the best time to sample the bit value is the mid-way point between the bit transitions to allow margin for skew and jitter. One edge of the recovered clock is aligned with the apparent bit transition edges. The alternate clock edge is used to sample the signal at mid-bit, forming a decision on the bit value. Hence, the frequency of the recovered clock is equal to the implicit bit rate. The sampling action can be implemented in multiple ways (ADC, D flip-flop). The shading on the NRZ waveform represents the jitter and skew that affects the data and thus reduces the margin for the sample clock. Because the

receiver recovers the clock from the data, jitter introduced by the transmitter clock not only appears in the data but also in the recovered clock. At first, this might appear to be advantageous because the data jitter and clock jitter could be correlated. However, the clock recovery architecture may induce a delay between the clock recovered at bit time T_n and the bit time in which it is actually used to sample the data. The random jitter appearing at bit times T_n and T_{n+1} will add and could result in either a larger (or smaller) jitter value. Combining this random jitter with other jitter sources could cause a bit error. National Semiconductor application note AN-1059 provides a detailed discussion of receiver data sampling, skew and jitter components, and margin.

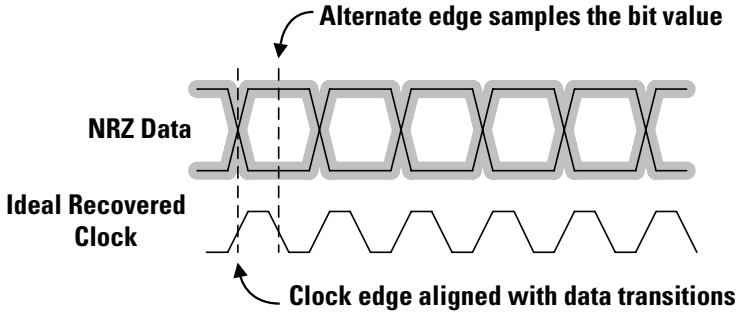


Figure 5.4 Example of Recovered Clock and Data Timing Relationship

Figure 5.5 shows the general structure of a receiver in which the input signal is used by a clock recovery block to generate a clock that is used to sample the input signal at the optimal time. However, there are several aspects of the end-to-end system that make this a challenging problem. The transmitter and receiver are separated by a channel whose frequency response will create distortion of the signal. This channel-induced distortion may be caused by attenuation of certain frequency components in the signal, group delay, and additive noise. Any clock jitter introduced at the transmitter is exacerbated by channel distortion. Components in the transmitter and receiver signal paths, such as amplifiers, modulators and filters can add to the jitter through random noise and non-linear behavior. These impairments act to corrupt the bit stream and the embedded clock. At the receiver, a clock recovery block will usually include a VCO and possibly a reference clock, and these devices will contribute some amount of jitter.

The three critical performance areas for the clock recovery block are:

1. It must have a certain phase relationship to the data in order to sample the incoming signal at the optimal times
2. It will have a frequency equal to the data rate
3. It must have low jitter

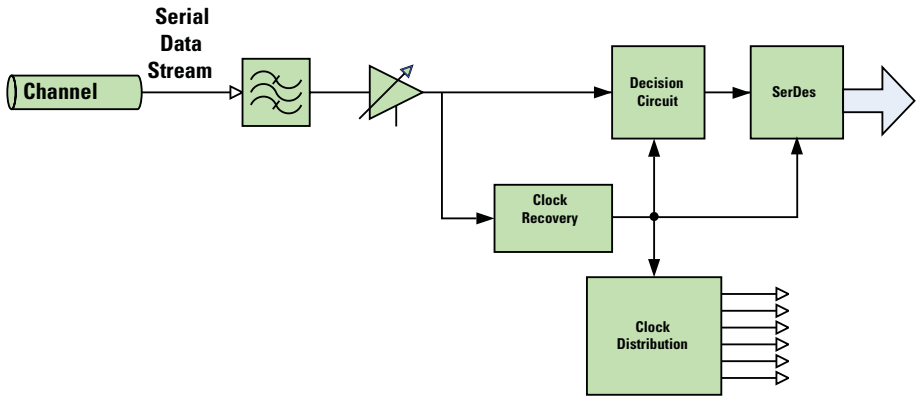


Figure 5.5 Block Diagram of a Serial Data Stream Receiver Architecture

The clock recovery block can be implemented in several ways. Some architectures use both a reference source and a VCO, while others use only a VCO. However, all of the possible architectures depend upon a low-jitter local frequency source that runs at the nominal data rate. The following section provides a brief introduction to both architectures, prefaced by a short discussion of phase detectors for random data.

Clock and Data Recovery Architectures

In this section we will briefly review some CDR architectures. The CDR's basic building blocks are a Phase Detector (PD), a VCO, a loop filter, and a decision circuit. Beyond these fundamental elements, the CDR may also include a reference source and a frequency detector (FD). The following section is a short review of two classes of phase detectors, linear and non-linear. Their basic operation is reviewed and some of their limitations are discussed.

CDR Phase Detectors

In a CDR, the phase detector must be able operate with random data as one of its inputs, the other input being the VCO. The two important functions of the PD are detection of data transitions and detection of the phase difference between the data and the VCO. For this reason, the structure of PDs in data communications is different than is commonly found in frequency synthesizers or LO circuits. Data communication PDs are typically based on an arrangement of D flip-flops and a few additional logic gates. Some well known phase detectors in this class are the Hogge PD [25] and the Alexander PD [26], also known as a Bang-Bang PD [27]. They are classified as linear (Hogge) or non-linear (Alexander). Linear phase detectors produce an error output whose voltage level or pulse width is proportional to the phase error between the data and VCO. ***Figure 5.6*** is an example of a linear detector. The error voltage is integrated to produce the control voltage for the VCO.

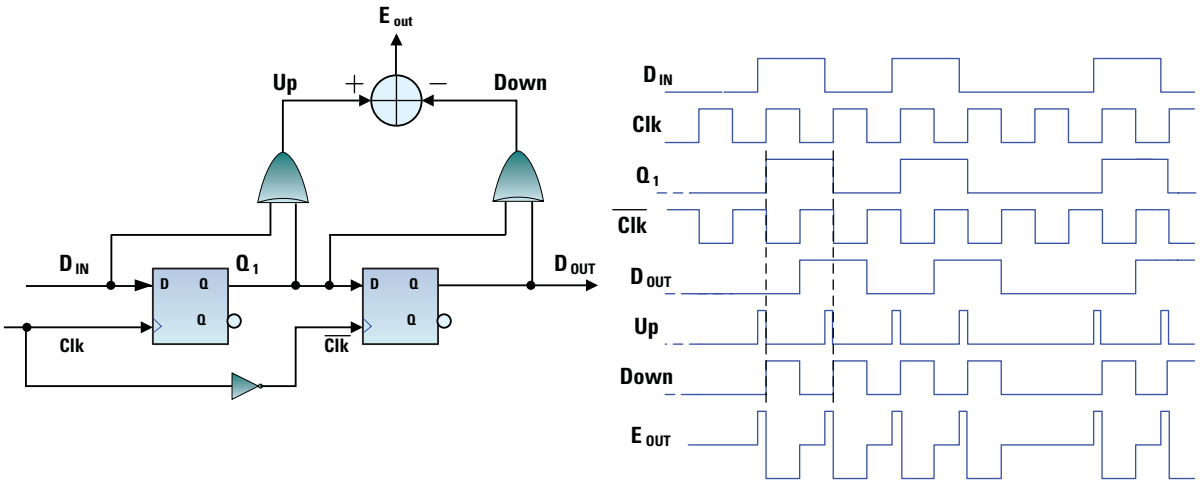


Figure 5.6 Example of Simple Linear PD

25 C. R. Hogge, "A Self-Correcting Clock Recovery Circuit," *IEEE Journal of Lightwave Technology*, Vol. 3, December 1985, pp. 1312-1314.
26 J. D. H. Alexander, "Clock Recovery from Random Binary Data," *Electronics Letters*, Vol. 11, October 1975, pp. 541-542.
27 S. I. Ahmed and T.A. Kwasniewski, "Overview of Oversampling Clock and Data Recovery Circuits," IEEE, *Canadian Conference on Electrical and Computer Engineering*, May 2005, pp 1876-1881.

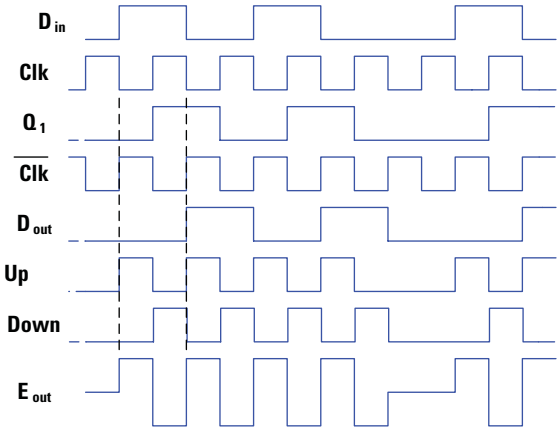


Figure 5.7 Linear PD Example in Phase Alignment

The output from non-linear PDs are typically binary-quantized, that is, either "0" or "1". Specifically, the Bang-Bang (BB) phase detector samples the signal at the nominal mid-bit time and data transition time, examining three consecutive sample values to produce a "decision" signal [28]. ***Figure 5.8*** and ***Table 5.1*** illustrate the principle of operation. ***Table 5.1*** lists the full truth table for the BB PD operation. ***Figure 5.8*** illustrates the case of an early clock phase.

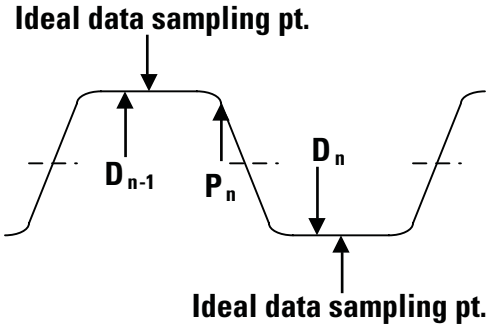


Figure 5.8 Bang-Bang PD Sampling

Table 5.1 Bang-Bang PD Truth Table

D_{n-1}	P_n	D_n	Decision
0	0	0	Hold
0	0	1	Early
0	1	0	Hold
0	1	1	Late
1	0	0	Late
1	0	1	Hold
1	1	0	Early
1	1	1	Hold

28 J. Sonntag and J. Stonick, "A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid State Circuits,* Vol. 41, No. 8, August 2006.

Though BB type PDs are more prevalent as data rates increase (due to their simplicity and accuracy), one of the problems with BB type PDs is that they exhibit limit cycle behavior in steady state operation [29]. Despite this problem, the implementation of the BB type PD has been well studied and there are several sources for detailed discussion of implementation. The list of references at the end of this guide contains a section on Bang-Bang phase detectors. If a more general introduction to PDs is preferred prior to diving into the specifics of implementation, [30] provides a good introduction to the operation of several basic phase detectors for random data. The references at the end of this manual list several good sources that cover CDRs and phase detectors. The survey of CDR architectures in this section will look at those with and without external references and the strategies used to overcome some of the limitations of each approach. Most of the discussion is drawn from [31].

Architectures Without an External Reference

CDRs that operate without an external reference can work well in scenarios where a narrow tuning range is acceptable, or a high-Q VCO can be used.

PLL-Based CDR - ***Figure 5.9*** presents a PLL-based CDR block in which the NRZ data is input to a Phase Detector (PD) (possibly after some pre-processing) and compared to the phase of a VCO. The VCO clocks a sampling device which produces a "clean" version of the bit stream. This architecture is most viable for lower data rates. The narrow bandwidth of the loop filter (required due to the noisy output of the PD generated by random data edges) means that the VCO phase noise will dominate the overall phase noise of the loop. Hence, the performance specifications of the VCO will be more important than in other architectures. The input signal depicted in ***Figure 5.9*** contains distortion due to device non-linearities and channel response, as well as random jitter. By optimally sampling the signal, these effects are removed and a clean version of the signal is produced.

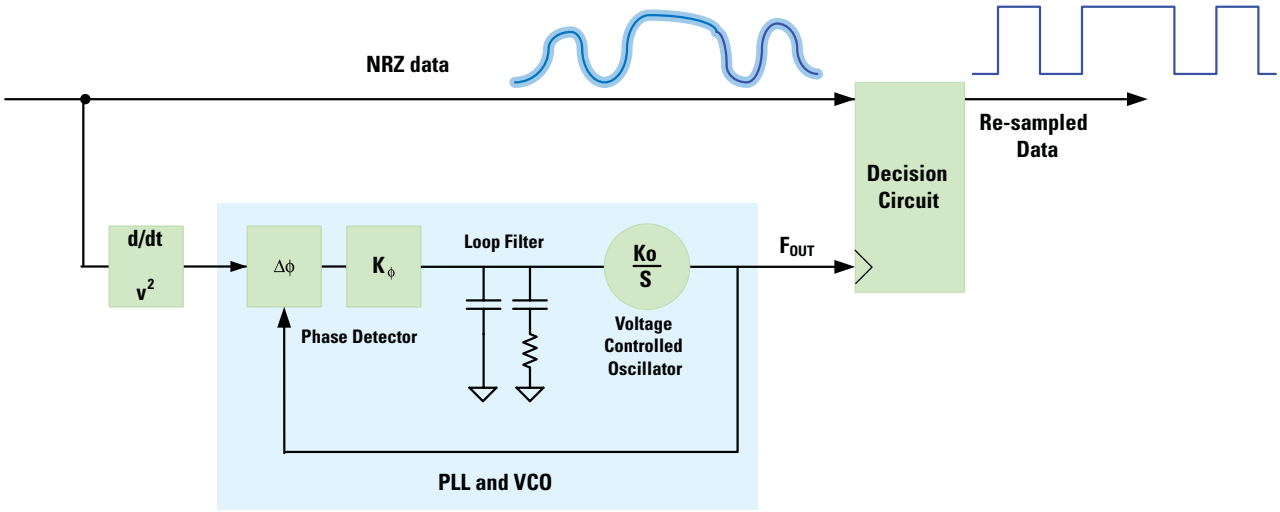


Figure 5.9 Generalized PLL-Based CDR Architecture

29 J. Sonntag and J. Stonick, "A Digital Cock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid States Circuits,* Vol. 41. No. 8, August 2006.
30 M Perrott, Massachusetts Institute of Technology, lecture notes on High Speed Communication Circuits and Systems: MSK Modulation and Clock and Data Recovery Circuits, 2003
31 B. Razavi, "Challenges in the Design of High-Speed Clock and Data Recovery Circuits," *IEEE Communications Magazine,* August 2002, pp. 94-101.

Aided Acquisition – If the frequency of the VCO is outside the capture range of the PD (at startup or due to any other event that causes loss of lock), then lock may never be achieved (or re-established). The addition of a Frequency Lock Loop (FLL) with a frequency detector (FD) can be used to aid in frequency acquisition, after which the phase detector loop takes over. ***Figure 5.10*** illustrates this structure. One problem with this architecture is that the two loops may enter a state in which they work against one another and the system may never achieve lock. Any spurious components appearing in the signal may also act to confuse the FD. Consequently, the bandwidth of the frequency loop may need to be lower than the phase loop. Modifications to this architecture that addresses these issues include separation of the loop inputs to the VCO so that that frequency control loop acts as a coarse control, and the PLL acts as a fine control. Another modification is a lock detect state machine that switches control from one loop to another when it detects frequency lock has been achieved [32].

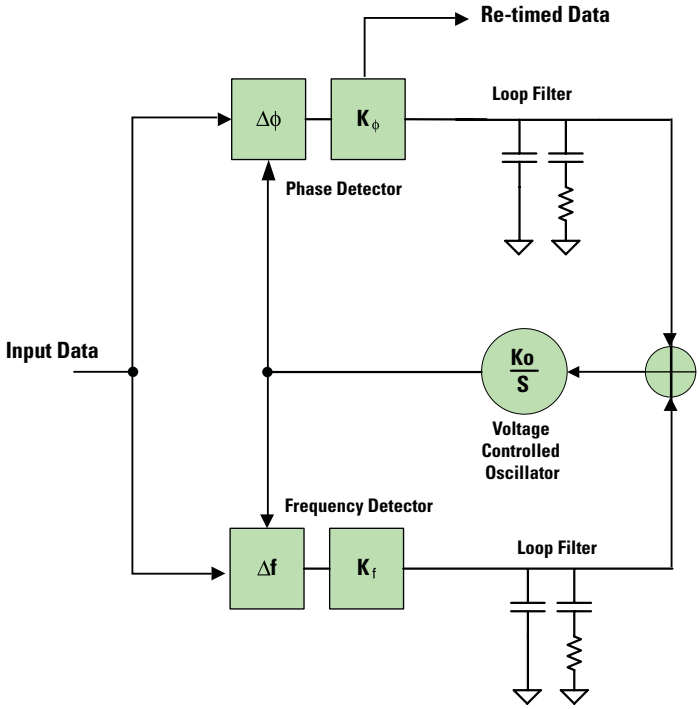


Figure 5.10 Aided Acquisition CDR Architecture

Architectures With an External Reference

Adding an external reference to the architecture can improve immunity to process variation in the VCO. The PLL/FLL act to correct for variations in the VCO. ***Figure 5.11*** illustrates a referenced-based architecture using an external reference and aided acquisition. The state machine controller monitors the state of both the PLL and the FLL and switches the control voltage between the two loops as appropriate. The advantage of this architecture is that the jitter performance of the circuit can be improved because the combination of the reference and PLL can be designed to provide very good close-in phase noise, while a VCO with good phase noise at larger offsets but whose close-in performance is nominal (i.e., lower Q) can be used if it provides some advantage in cost. However, this architecture can have problems if the local reference has a frequency offset relative to the reference at the transmitter. If all of the local references in the system meet minimum accuracy and stability requirements, or are themselves locked to some master reference, then this architecture works well.

32 R. Walker, "Clock and Data Recovery for Serial Digital Communication," *IEEE International Solid State Circuits Conference Short Course,* February 2002.

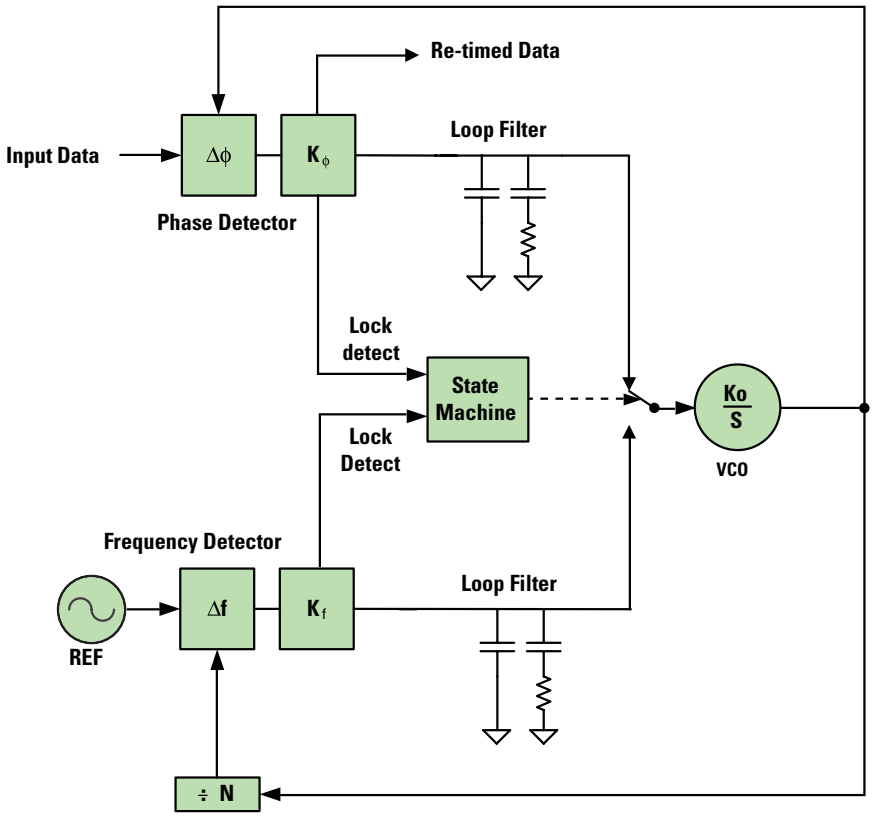


Figure 5.11 CDR Architecture with External Reference

Jitter Sources

In the data communications world, engineers usually try to resolve jitter into its random and deterministic components. *Jitter tolerance* (JT) is defined as the ability of the clock recovery circuit to maintain lock under specified peak-to-peak jitter. The JT of the clock and data recovery architecture always depends upon the levels of both deterministic and random jitter. The cause of each of these components is usually attributable to different sources, so that separately measuring and characterizing them begins to sort the probable causes into subsets. Furthermore, by measuring the relative impact of random jitter and deterministic jitter, it is possible to assess where the most improvement can be achieved for reasonable cost. In this section, we will discuss some common causes and sources of jitter, and then review the mathematical model that is most often employed in high-speed communication standards.

Deterministic Jitter Causes

In Chapter 2, we covered some of the causes of random jitter. Some examples were thermal noise, flicker noise, and shot noise. In this section, we will briefly introduce some causes of deterministic jitter and their manifestations.

Data Dependent Jitter – Data Dependent Jitter (DDJ), sometimes referred to as pattern dependent jitter, is due to particular data bit sequences interacting with the system impulse response. Stated another way, insufficient channel or system bandwidth distorts the bit pulses, usually slowing down the edge rates, resulting in a deviation from the expected threshold crossing time. In rapidly changing data sequences (strings of alternating 0s and 1s) the pulses my not reach a steady state level, resulting in jitter on

isolated pulses. Inter-Symbol Interference (ISI) is another term that is used to describe this jitter. [33] provides a basic derivation illustrating the dependency of threshold crossing times on data bit sequences. Though the latter uses a simplified model based upon a Taylor-series approximation, it provides some insight to the influences on DDJ, as seen in ***Equation (5.1)*** for the threshold crossing time, t_C:

$$t_C = t_0 + \frac{v_{TH} - \sum_k a_k \left[u(t_0 - kT) - u(t_0 - (k+1)T)\right]}{\sum_k a_k \left[u'(t_0 - kT) - u'(t_0 - (k+1)T)\right]} \quad (5.1)$$

where: $u(t)$ = step response of the system,
$u'(t)$ = the first derivative of the step response, and
$u(t) - u(t\text{-}T)$ = system pulse response.
t_0 = expected threshold

If we define jitter as t_C-t_0 = Δt_D, then the expression to the right of the "+" sign in ***Equation (5.1)*** represents Δt_D. ***Equation (5.1)*** says the DDJ depends on the previous bit sequence $\{a_k\}$ and on the system pulse response. Assuming for the moment, a linear system and therefore that the slopes of the rising and falling edges are symmetrical, the derivative in the denominator gives us the intuitive observation that waveforms with slower edges will tend to have higher DDJ. [34] provides fundamental derivation and description of ISI. From the designer's perspective, the use of an equalizer in the receiver front end can help reduce the impact of DDJ (ISI), but DDJ usually cannot be completely eliminated. Hence, the clock recovery architecture must be designed with some JT with regard to DDJ.

Baseline Wander (BLW) – Caused by a low-frequency cutoff somewhere in the signal path. The effect is a slowly changing bias in the signal, causing the threshold crossing points on the waveform to wander.

Amplifier offsets – May cause pulse-width (or duty cycle) distortion, as the signal mean will be offset relative to the decision threshold, causing the durations of the positive and negative logic portions of the signal to be unbalanced.

Non-linear Amplifier effects – Unpredictable, but often can be seen in asymmetric slopes of rising and falling clock edges.

Power Supply Noise and Crosstalk – Noise from switching power supplies will have a periodic component, which, if coupled to the data signal, will introduce a deterministic component into the jitter. Systems that have multiple serial data streams and significant capacitive coupling may exhibit crosstalk between the streams, called bounded uncorrelated jitter (BUJ). [33] derives an expression for BUJ for the case of microstrip on a PCB and equiprobable NRZ data:

$$\Delta t_{BUJ} = -\frac{Z_0 C_C}{2} \frac{\sum_k (b_k - b_{k-1}) u'(t_0 - kT)}{\sum_k (a_k - a_{k-1}) u'(t_0 - kT)} \quad (5.2)$$

where $\{b_k\}$ is the bit sequence of the interferer signal,
Z_0 = the characteristic impedance of the transmission line, and
C_C = the coupling capacitance of the PCB.

Equation (5.2) says that BUJ depends on the history of both the victim and aggressor signals and is also a function of characteristic impedance and capacitive coupling of the PCB.

33 J. Buckwalter, B. Analui, A. Hajimiri, "Data-Dependent Jitter and Crosstalk-Induced Bounded Uncorrelated Jitter in Copper Interconnects," *IEEE MTT-S Digest*, 2004.
34 John G. Proakis, *Digital Communications*, 4th Edition, McGraw Hill, New York, 2001.

Clock Skew

In many communication systems, it is often required to clock several devices from the same reference clock or a derivative of the reference clock. Some examples are cellular basestations and data network nodes where data is being aggregated and disaggregated. In ***Figure 5.5***, the recovered clock in a receiver is injected into a distribution device that provides multiple copies of the recovered clock to other devices in the system. Phase alignment of these clocks is usually required. However, either the distribution device or the down stream signal path may introduce skew. If the distributed clocks are being used to clock data coming from the link, there will be setup and hold time requirements in the post-detection processing that must be met. In ***Figure 5.1*** through ***Figure 5.3*** parallel data is being multiplexed into a serial stream. There are two elements of skew (differential delay) that must be controlled for proper operation of the multiplexing operation. The first is the channel-to-channel skew, and the second is the channel-clock-to-mux-clock skew. For example, unmatched gate delays in digital devices can introduce skew. Unequal signal path lengths can also introduce skew. Hence, programmable skew control is an important feature of any clock conditioner used in this architecture. Consider a clock signal propagating on a transmission line on FR-4 printed circuit substrate:

$$V = \frac{c}{\sqrt{\varepsilon_r}} = \text{the velocity of propagation,} \qquad (5.3)$$

where the speed of light is c = 0.2998 mm/ps and the relative dielectric constant for the transmission medium is ε_r (ε_r = 4.2 for FR-4). Since we are interested in the time skew introduced by a difference in path length it may be more convenient to consider the reciprocal of ***Equation (5.3)*** which gives us the time required to propagate the signal 1 mm, 6.84 ps. Thus a difference in path length of 1 mm can cause about 7 ps of clock skew.

Jitter Characterization and Measurement

As stated previously, the data communications world separates jitter into its deterministic and random components. Deterministic jitter is usually characterized by its peak-to-peak value and random jitter by its RMS value (or standard deviation). In this section, we will briefly review the nomenclature employed and how total jitter is defined from random jitter and deterministic jitter.

Characterization and Modeling – Random jitter comes from random processes such as thermal noise. Though we saw in Chapter 2 that not all of these random sources have a Gaussian probability density function (PDF), almost all jitter models employed in the data communications world treat this random jitter as Gaussian, with zero mean and variance σ^2_J. The familiar PDF is:

$$p_J(\Delta t_J) = \frac{1}{\sigma_J \sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{\Delta t_J}{\sigma_J}\right)^2} \qquad (5.4)$$

where Δt_J is the jitter random variable. Random jitter is normally inherent to VCOs, PLLs, DLLs, and reference sources.

Though there are many causes of deterministic jitter, DDJ is the most common in data communications. If we are able to apply ***Equation (5.1)*** and also assume that for values of k that are more than 2 bit times removed from the current bit the contribution is negligible, then a finite number of terms can be found for DDJ. Because they are finite and deterministic, the PDF of DDJ is usually modeled as the summation of a series of Dirac-delta functions at the offsets computed from ***Equation (5.1)***, having the form:

$$p_D(\Delta t_D) = \sum_{m=1}^{2^N} \beta_m \delta\left(t - \Delta t_{D,m}\right) \qquad (5.5)$$

Because uncorrelated jitter components combine through convolution, ***Equation (5.5)*** may result from the convolution of multiple pairs of DDJ. The coefficients $\{\beta_m\}$ are the product of the convolution operation and are proportional to $(1/2)^k$.

In a system that has both random and deterministic jitter, the total PDF is found by convolving $p_J(\Delta t_J)$ and $p_D(\Delta t_D)$, graphically illustrated in ***Figure 5.12.***

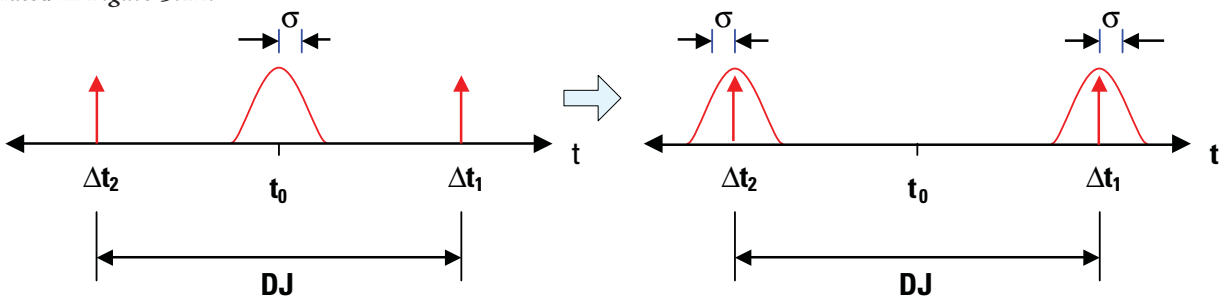


Figure 5.12 Total Jitter Distribution from Convolution of Individual Jitter PDFs.

Figure 5.12 illustrates a model often used in test and measurement of digital transmission systems called the *dual-Dirac delta model* [35] [36]. This model was developed for the purpose of providing a quick and reliable method of estimating total jitter at a given BER based on reasonable short term measurements. While we have arrived at this model by combining random jitter with peak-to-peak DDJ, in practice, the dual-Dirac model is not intended to approximate the true DDJ distribution. The implied DDJ distribution in the model is meant to result in the best fit between the measured jitter distribution and the model with Gaussian tails at the extremes. In the next section, the utility of this model and its implications for measurement will be more fully explained.

Measurement - In Chapter 2, we saw that the frequency domain was the preferred approach for measuring random jitter. In the data communications world, observation of the jitter in the time domain is the preferred measurement method. The most common way to observe jitter in the time domain is using an oscilloscope to capture multiple clock cycles overlaid on one another, resulting in the classic "eye" diagram, as shown in ***Figure 5.13***. Most high-speed modern oscilloscopes have a feature that captures waveform data over an extended period of time and not only builds an eye diagram, but accumulates the values of the threshold crossings and builds a histogram of the crossing distribution, as shown in ***Figure 5.14***.

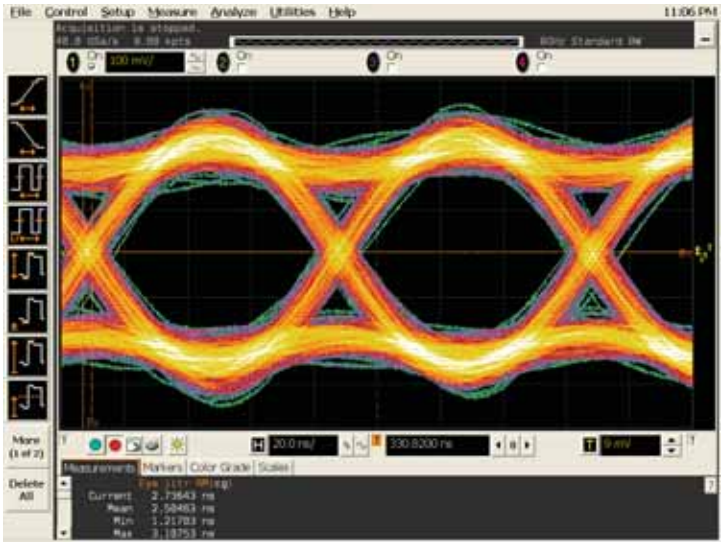


Figure 5.13 Eye Diagram

35 R. Stephens, "Jitter Analysis: The dual-Dirac Model, RJ/DJ, and Q-scale," *Agilent Technologies White Paper,* 2005.
36 C. Pease and D. Babic,"Practical Measurement of Timing Jitter Contributed by a Clock-and-Data Recovery Circuit," *IEEE Transactions on Circuits and Systems –I: Regular Papers,* Vol. 52, No.1, January 2005.

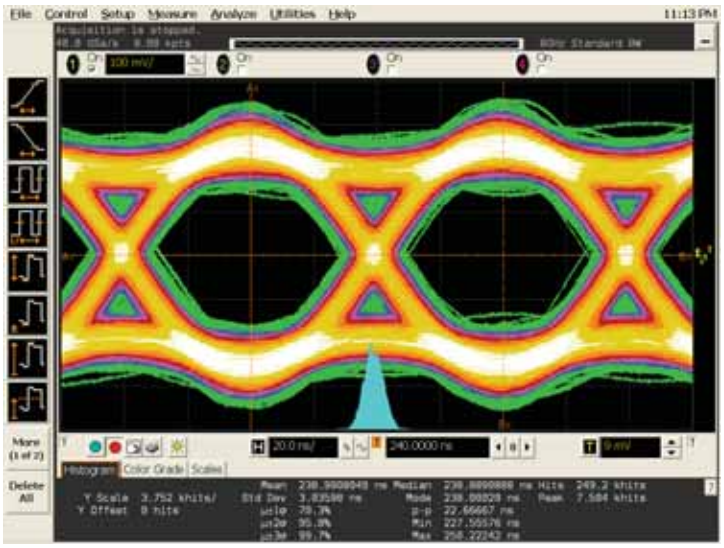


Figure 5.14 Eye Diagram with Histogram of Random Jitter

Some of the key aspects of eye diagrams are:

- The primary value of the eye-diagram is that is allows us to visually observe the margin of error for sampling the waveform. Comparing ***Figure 5.13*** and ***Figure 5.14***, we see that as the jitter has increased, the "eye' closes, in affect, decreasing the margin of error for the data sampling point. Crossover points are the level at which the accumulated rising and falling edges intersect, representing the transition threshold for each bit waveform. This threshold should be more or less mid-range between the maximum amplitude and minimum amplitude of the bit waveforms, and should be equivalent at both the left and right sides of the diagram. If there are other crossover intersections, then this indicates duty-cycle distortion and possibly DDJ.

- If multiple rising edges or multiple falling edges are observed, as shown in ***Figure 5.15***, the presence of deterministic jitter (DJ) is indicated.

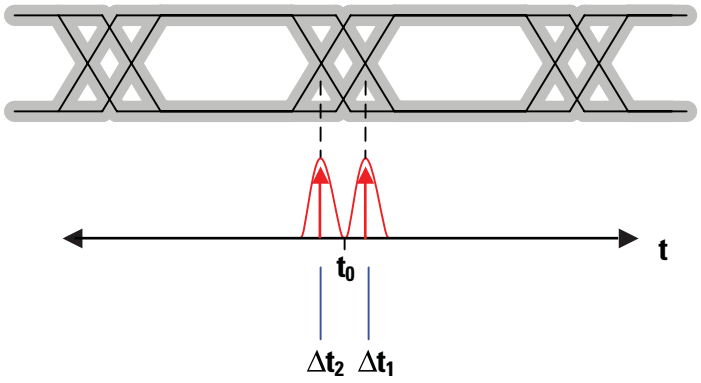


Figure 5.15 Eye Diagram of a Signal with Deterministic Jitter

Given a distribution as shown in ***Figure 5.15***, one measurement task is to estimate the standard deviation (σ) of the random jitter and the DJ value that best fits the model shown in ***Figure 5.12.*** [35] provides a thorough explanation of the use of the dual-Dirac model to estimate total jitter. Additional jitter measurements include jitter tolerance, jitter transfer, and jitter generation. These measurements are generally made at the component level to ensure compliance with a standard or specification. For most high-speed applications (several hundred Mbps to several Gbps), specialized jitter measurement equipment is required (high-speed sampling oscilloscopes and jitter analyzers) to accurately measure jitter performance. ***Figure 5.16*** illustrates a generic measurement setup for jitter. It consists of a highly accurate, very low jitter frequency reference. Clock source A produces a low jitter version of the data clock which is used as a trigger for the measuring instrument. Clock source B also produces a version of the data clock, but with a calibrated amount of jitter injected from a controlled source; clock B is used to clock a pattern generator with dual outputs. One set of outputs is used to drive the device under test (DUT), while the complementary set is injected into the measurement instrument as a reference for measuring jitter transfer. The clock output from the pattern generator to the DUT is shown as a dotted line because this may not be necessary or even possible to use with the DUT.

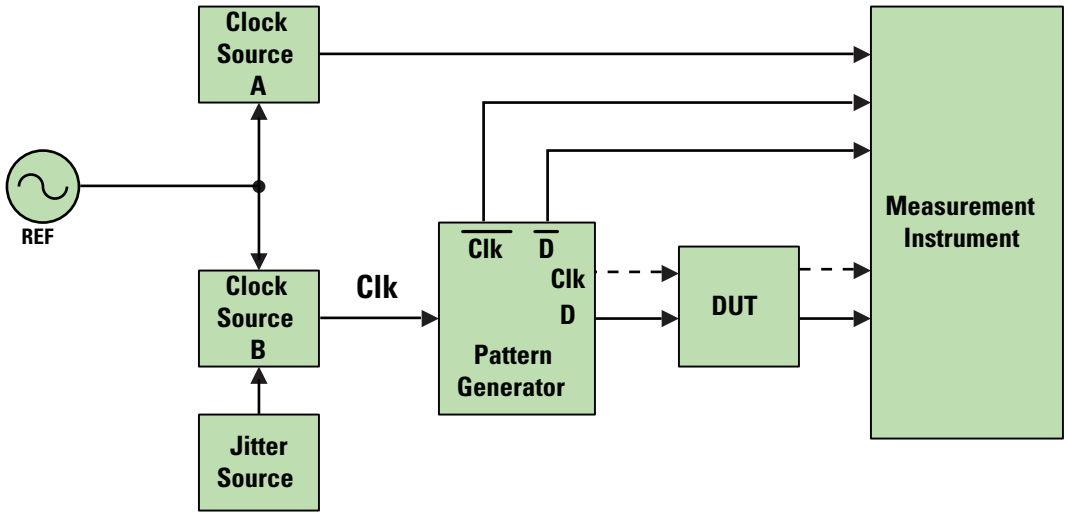


Figure 5.16 Example of a Generic Jitter Measurement Setup

Online Resources

National Semiconductor's LVDS website can be found at:
lvds.national.com

This website provides access to several valuable resources for the engineer working in the area of high speed data communications. Some specific references that can be accessed through this website are listed below. These references offer fundamental technical introductions to specific technologies that are related to high speed serial data communications and in particular, critical aspects of the clocking function.

App Notes

National Semiconductor, "High Speed Transmission with LVDS Link Devices," *Application Note 1059* (AN-1059), June 1998.

Design Guides

LVDS Owner's Manual, National Semiconductor, 3rd Edition, Spring 2004.
DS92LV16 Design Guide, National Semiconductor, October 2002.
18-bit SerDes Design Guide, National Semiconductor, June 2005.
Channel Link Design Guide, National Semiconductor, June 2006.

Papers

Dave Lewis, National Semiconductor Corporation, "SerDes Architectures and Applications," DesignCon 2004,
www.national.com/appinfo/lvds/files/designcon2004_serdes.pdf.

Chapter 6
Design Guidelines

Introduction

This chapter will discuss hardware design issues that are particularly relevant to clock conditioners. In general, this chapter is not meant to be a complete guide to hardware design or PCB design, but it offers some insight into certain design aspects that are particularly important when designing clock conditioner circuits used to clock data converters or in clock distribution applications. Generally accepted, good design practices are assumed, and where these would be contrary to best practice for clock conditioners, an explanation will be provided.

Much of the material in this chapter is drawn from other National Semiconductor design guides and seminar material, particularly in the areas of Low Voltage Differential Signaling (LVDS) and data converters. [37] The latter technologies have much in common with clock conditioners, either in the:

- Application domain - Clock conditioners are used to clock data converters
- Implementation - Clock conditioner interfaces can employ the LVDS format
- Functional characteristics - Operational frequencies and mixture of analog and digital technology

Engineers familiar with LVDS and high-speed data converter design practices will find familiar material in this chapter. However, this material will be presented with a slant toward clock conditioners, and so will offer some unique insights.

The major objectives when designing circuits that involve clock conditioners are to:

- Minimize electromagnetic interference (EMI)
- Minimize distortion due to signal path characteristics (or alternately, maintain signal integrity)
- Minimize any internally generated noise

This chapter is organized as follows:

1. Fundamental aspects of signal behavior in printed circuit boards (PCBs), for both single ended and differential signals.
2. Transmission line theory
3. Aspects of Radio Frequency Interference (RFI) and EMI.
4. Issues related to signal integrity (distortion)
5. Design tips and rules
6. Summary

Transmission Lines

Clock and oscillator frequencies from several megahertz up to multiple gigahertz are routinely used in today's systems. Even the clocks used in lower speed applications utilize sharper edges than in the past. At these frequencies, a PCB can no longer be treated as a lumped system, a simple collection of electrical interconnects. Traces carrying these high-speed signals need to be treated like transmission lines. These transmission lines should be designed with appropriate impedance and need to be correctly terminated.

37 LVDS Owner's Manual, Low-Voltage Differential Signaling, 3rd edition, National Semiconductor, http://www.national.com/appinfo/lvds/0,1798,100,00.html

The equivalent circuit model for a transmission line with losses is shown in ***Figure 6.1*** .

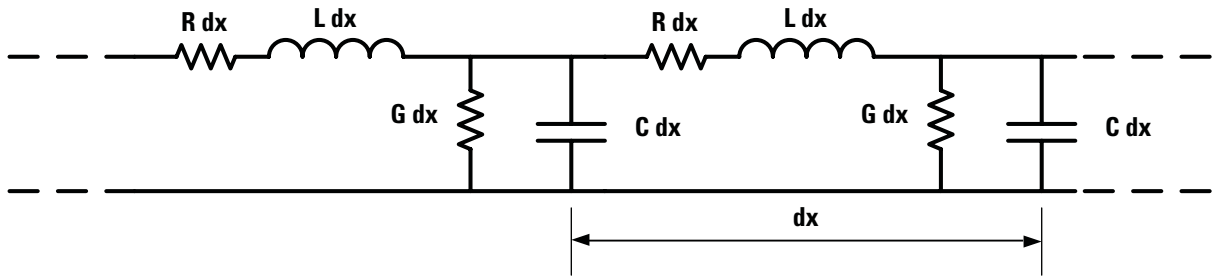


Figure 6.1 Transmission Line Model with Return R and L Folded into the Signal Line [38].

R = series resistance of the conductor, per unit length
L = inductance per unit length
C = capacitance per unit length
G = admittance per unit length

The characteristic impedance (Z_0) of the general transmission line is the ratio of voltage to current at any point along the line and at any instant. In terms of the circuit parameters from ***Figure 6.1***, Z_0 is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad \frac{ohms}{unit\ length} \tag{6.1}$$

At high frequencies, the imaginary terms greatly dominate R and G, so that $Z_0 \approx \sqrt{\frac{L}{C}}$. The importance of Z_0 comes from the fact that discontinuities in Z_0 create signal reflections which in turn degrade signal integrity, as these reflections combine with the desired signal and result in a distorted waveform. Depending on the type of transmission line, L and C are functions of the geometry of the conductors and material properties. *Permittivity* (ε), also referred to as the dielectric constant, and μ, the *permeability* are material characteristics that help determine the capacitance and inductance of transmission lines. Permittivity relates to the material's ability to transmit (or permit) an electric field. Permeability is the degree of magnetization of a material that responds linearly to an applied magnetic field.

When must we treat a trace like a transmission line? When dealing with digital signals, one rule of thumb is shown in ***Equation (6.2)***:

$$L_{MAX} \geq \frac{t_R}{6 \cdot t_{PR}} \tag{6.2}$$

L_{MAX} = maximum line length beyond which the line must be treated as a transmission line.
t_R = the 10% to 90% rise time
t_{PR} = signal propagation rate. For FR-4 board, 150 ps/in. < t_{PR} < 175 ps/in.

For analog signals, rise time from 10% to 90% can be approximated by ***Equation (6.3)***:

$$t_R = \frac{\cos^{-1}(-0.8) - \cos^{-1}(0.8)}{2\pi \cdot f_{max}} \approx \frac{2}{7 f_{max}} \tag{6.3}$$

38 Stephen C. Thierauf, *High-Speed Circuit Board Signal Integrity*, Artech House, Boston, 2004.

From ***Equation (6.3), Table 6.1*** can be constructed which lists the effective frequency for various rise times. When designing the PCB board with signals having specified rise and fall times, the design approach should be similar to those taken when dealing with RF signal frequencies equal to the effective frequency. The effective frequency also gives insight into the problem of selecting oscilloscopes and probes of the correct bandwidth to measure defined rise time signals. To measure a 100 ps rise time, a scope and probe capable of measuring a 3 GHz signal is required.

Table 6.1 Rise Time Viewed as Effective Frequency

Rise Time	10% to 90% rise time Effective Frequency	20% to 80% rise time Effective Frequency
1 µs	295 kHz	205 kHz
100 ns	2.95 MHz	2.05 MHz
10 ns	29.5 MHz	20.5 MHz
1 ns	295 MHz	205 MHz
100 ps	2.95 GHz	2.05 GHz
10 ps	29.5 GHz	20.5 GHz
1 ps	295 GHz	205 GHz

Currents in Conductors

This section reviews some basic concepts of currents and fields in conductors that will motivate the discussion in subsequent sections dealing with design techniques that minimize EMI and preserve signal integrity.

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance. For high-speed signals, the return current path will be the path of least inductance. The Proximity Effect on two conductors carrying opposite high frequency currents causes the AC current flow in those nearby conductors to be primarily on the side of the conductors nearest each other. In the case of a single trace over a copper ground plane acting as the return, the return current density in the ground plane is a function of the height (h) of the signal trace above the ground plane (or separation between the trace and ground plane) and the distance (D) from the edge of the signal trace, as shown in ***Figure 6.2.***

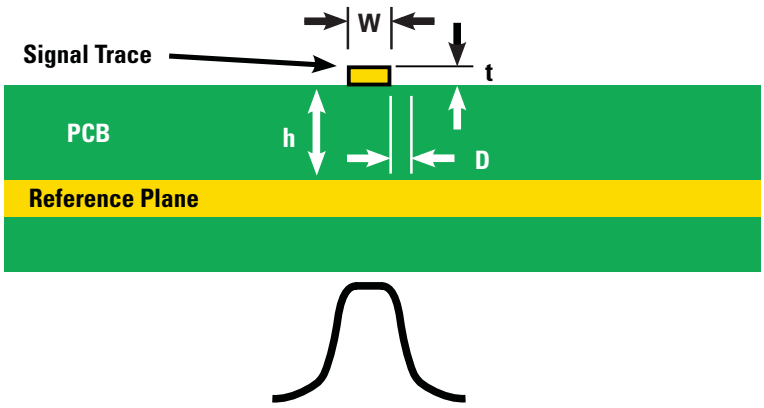


Figure 6.2 Current Density Profile for a Signal Trace over Ground Plane

$$I_{RP} = \frac{i}{h \cdot \pi \cdot \left(1 + \left(\frac{D}{h}\right)^2\right)} \frac{amps}{unit\ length} \quad (6.4)$$

I_{RP} = Reference plane current density at horizontal distance "D" from the outgoing signal trace
i = signal current
h = Height of the signal trace above the reference plane
D = Horizontal distance from the closest edge of the trace. D = 0 under the trace.
The dimensions can be any unit (mm or mils), as long as all dimensions are in the same unit.

The current density formula in ***Equation (6.4)*** gives us the current density at any point in the plane relative to the edge of the outgoing trace, or dimension "D". Note that this formula gives us current density, not current. The current density is highest directly beneath the signal trace and begins falling off proportionally to D^2 when observed beyond the trace edges. When D/h ≈ 5, the current density is around 4% of the maximum that occurs directly beneath the trace, and is 1% at D/h = 10. The result is a current density in the ground plane that is fairly well confined to the area below that current's corresponding outgoing current path. If adjacent traces are too close to each other, return currents can combine and produce crosstalk.

For differential signaling formats (LVDS, LVPECL, etc.) the return path is provided by a second signal trace. The signal current that flows in one trace of the pair will flow back through the other trace, completing the current-loop. This is ideal, because the current return antenna loop area can be minimized since the traces of a differential pair can be closely spaced. Real signals, however, will have some common-mode noise current, which must return also. This common-mode current will be capacitively coupled to ground and return to the differential driver through the path of least inductance. Therefore, a short ground current return path is still needed between the driver and receiver in differential systems. On PCBs, the best current return path is a uniform, unbroken ground plane beneath the differential signals as is the case with single ended signals. The ground plane allows the common-mode (even mode) current to return directly under the differential signals. This closely coupled path is the path of least inductance and means that the common-mode current loop area is minimized.

Electric Fields

The electric fields around a conductor are proportional to voltage or current. In single-ended lines like CMOS/TTL lines shown in ***Figure 6.3 (b)***, almost all the electric field lines are free to radiate away from the conductor. Certain structures can intercept these fields. But some of these fields can travel as Transverse Electromagnetic (TEM) waves which may escape the system and cause EMI problems.

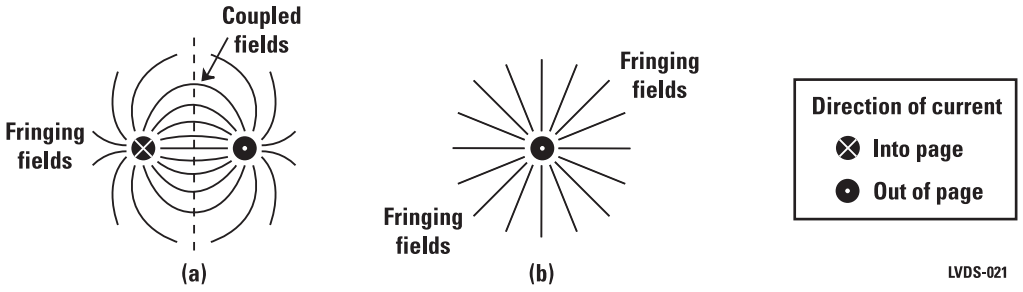


Figure 6.3 Electromagnetic Field Cancellation in Differential Signals Through Coupling (a) vs. a Single-Ended Signal (b)

Electric fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to the designer's advantage and such is the case with tightly coupled differential lines when the two traces carrying the signals are in close proximity with one another.

Balanced differential lines have equal but opposite ("odd" mode) signals. This means that the concentric magnetic field lines tend to cancel and the electric fields couple as shown in ***Figure 6.3 (a)***. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals, much less field energy is available to propagate as TEM waves vs. single-ended lines. The closer the two conductors, the better the coupling and the less EMI radiated.

Electro-magnetic Radiation

Today's increasing data rates and tough Electromagnetic Compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through TEM waves, which can escape through shielding and cause a system to fail EMC tests.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For differential signaling, the DC currents should never flow in the same direction as in ***Figure 6.4 a***, but various factors can cause an imbalance in currents (c) vs. the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

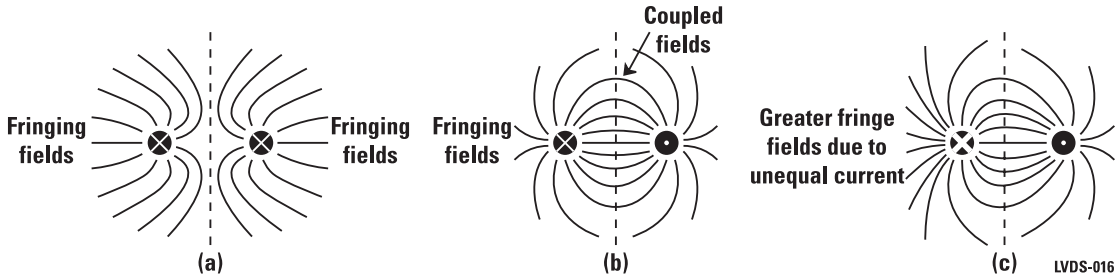


Figure 6.4 Even or Common Mode Signals (a), Ideal Equal and Opposite Odd Mode Signals (b), and Unbalanced Signals on Differential Lines (c)

Fields resulting from imbalances cannot easily be measured unless an elaborate EMI lab is readily available. However, fields are proportional to voltage and current amplitude so measuring waveforms, which is relatively easy, provides a strong indication of the far field. Any factors affecting the time (i.e., delay, velocity) and/or amplitude (i.e., attenuation) properties of the signals can increase EMI and can be seen on a scope. ***Figure 6.5*** illustrates how waveforms – easily seen on a scope – can help predict far field EMI. First, the beneficial field canceling effects of ideal differential signals (b) vs. single-ended signals (a) are compared. A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common-mode noise, and unbalanced attenuation. These affect the relative amplitudes of the fields at any given moment, reducing the canceling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

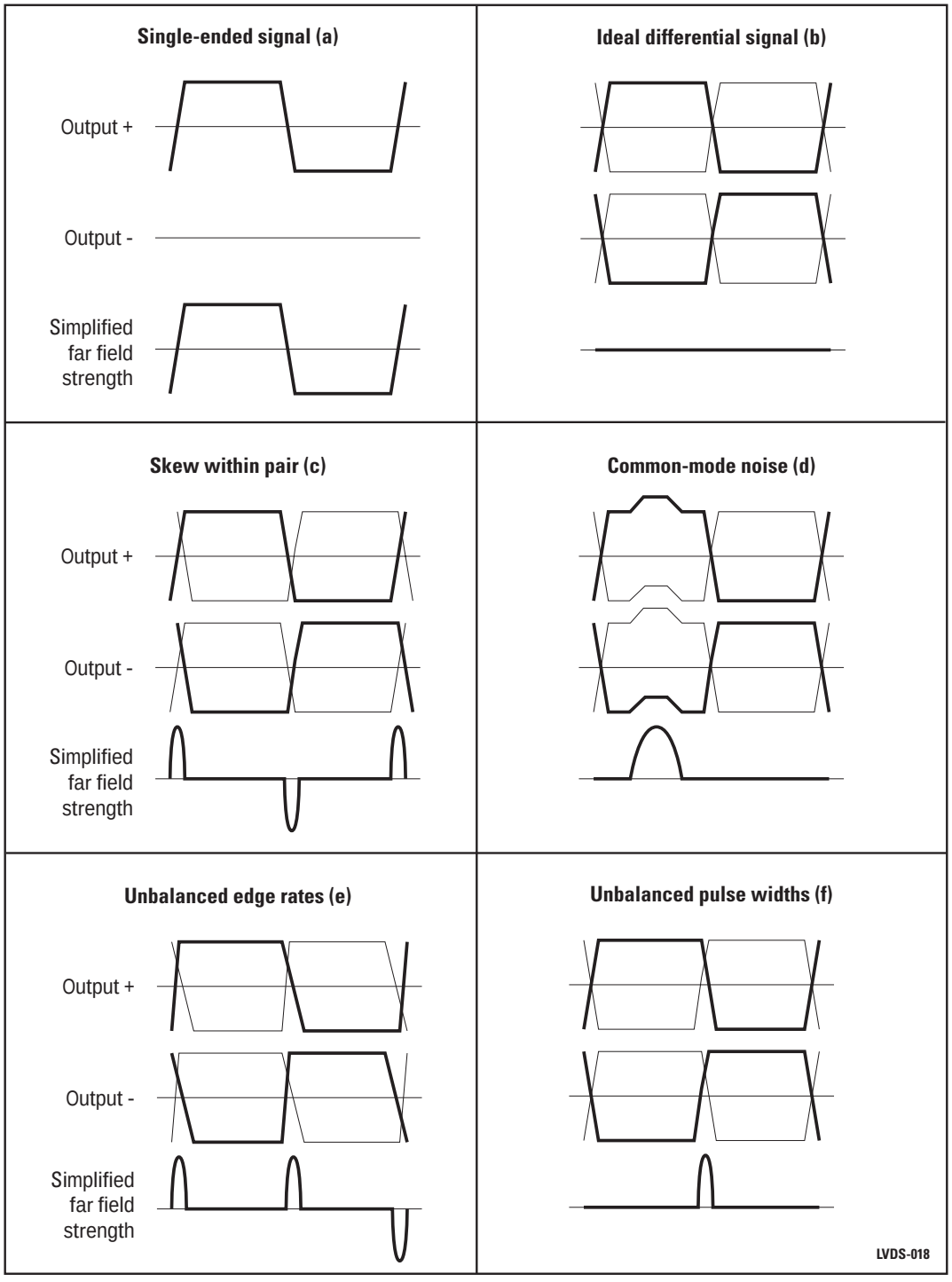


Figure 6.5 Simplified Far Field Radiation Under Various Conditions

Designing Transmission Lines

So far the traces discussed have been theoretical. Now we will discuss the different possible designs for traces. ***Figure 6.2*** represents a single-ended signal trace and is also a form of microstrip transmission line. ***Figure 6.6*** illustrates examples of three types of differential microstrip and stripline transmission lines constructions. The differential microstrip ***(Figure 6.6 a)*** and differential stripline ***(Figure 6.6 b)*** examples use edge coupling. The broadside differential stripline configuration ***(Figure 6.6 c)*** couples the width of the trace. ***Table 6.2*** introduces the closed form equations necessary to calculate trace dimensions for use in each design.

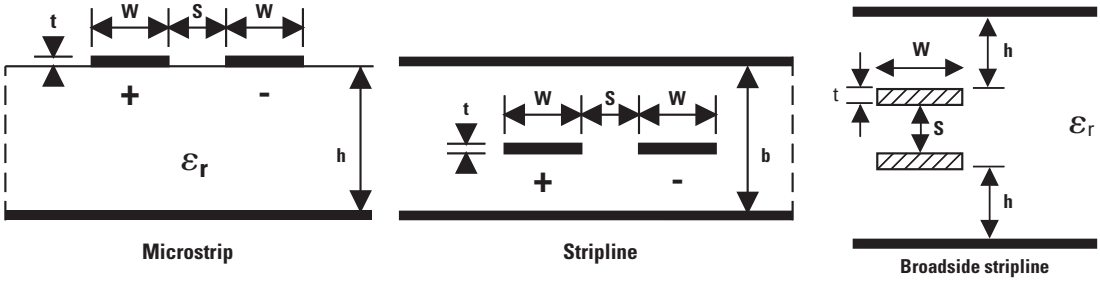


Figure 6.6 Microstrip and Stripline Transmission Lines

Table 6.2 Characteristic Impedance (Z0) for Common Transmission Line Types

Transmission Line Type	Z_0
Single-ended Microstrip *Figure 6.2*	$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left(\frac{5.98h}{0.8W + t}\right)\Omega$
Differential Microstrip, edge-coupled *Figure 6.6 a*	$Z_0 = \frac{60}{\sqrt{0.457\varepsilon_r + 0.67}} \cdot \ln\left(\frac{4h}{0.67(0.8W + t)}\right)\Omega$
Differential Stripline, edge-coupled *Figure 6.6 b*	$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\pi(0.8W + t)}\right)\Omega$
Differential Stripline, broadside-coupled	There is no closed-form equation for calculating the impedance of broadside-coupled stripline. Instead, a field solver should be used.

Traditionally 50 ohms is the characteristic impedance designed for in single ended RF circuits and used on test and measurement equipment. LVDS and LVPECL signals are designed with a differential impedance of 100 ohms. If uncoupled transmission lines were to be used with an LVDS or LVPECL signal, each trace would be designed to have a single-ended impedance of 50 ohms. Always use consistent dimensions (e.g., all dimensions in mils, cm, or mm) for S, h, W, and t when making calculations.

The ideal cases for microstrip and stripline traces are represented by ***Figure 6.7 (a)*** and ***(b)***. Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100 Ω Z_0 (Z_{DIFF}).

Depending on the environment of the PCB, effects similar to ***Figure 6.5*** can be seen in microstrip and stripline PCB traces. In an ideal world, the few remaining unterminated field lines of a differential microstrip or stripline (shown in ***Figure 6.7 a, b***) can be safely disregarded. However, in some circumstances the use of shield traces with critical differential microstrip may be required. As shown in ***Figure 6.7 d***, shielding traces will benignly terminate stray fields and do so without significantly impacting propagation velocity. Shield traces (preferably ground) should be added on both sides of the differential pair. Adding a single shield trace – or any trace – on one side of a differential pair ***(Figure 6.7 c)*** creates an imbalance that can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2S from the pair.

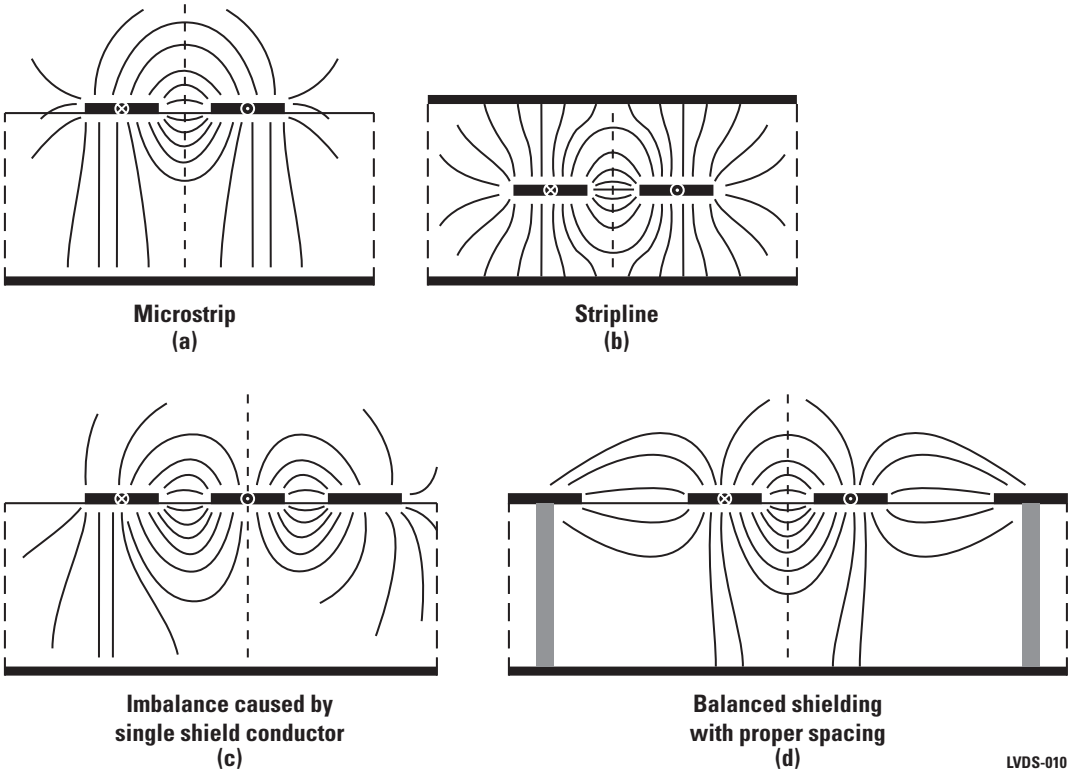


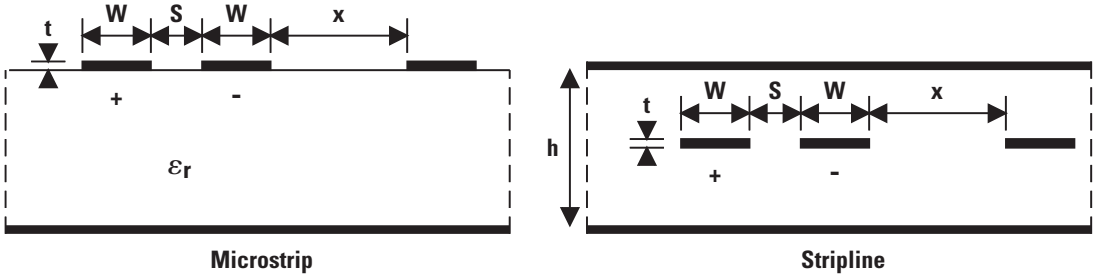
Figure 6.7 Ideal Differential Signals on Microstrip (a), Stripline (b), Negative Effects of Unbalanced Shielding (c), and Positive Effects of Balanced Shielding (d)

Design practices for low EMI

As discussed in the preceding sections, the two most important factors to consider when designing differential signals for low EMI are 1) close coupling between the conductors of each pair and 2) minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first. In order for sufficient coupling of EM fields to occur, the space between the conductors of a pair should be kept to a minimum as shown in ***Figure 6.8.*** (Note that matched transmission impedance must also be maintained). Close coupling also increases the immunity of the circuit to received electromagnetic noise. Noise coupled onto the conductors will do so as common-mode noise, which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also minimizes the antenna loop area.

When using differential stripline, power and ground planes or traces should not be closer than the distance between the differential conductors. This practice will lead to closer coupling between the differential conductors, as compared with the coupling between each conductor and the power/ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W.

The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.



For good coupling, make S < W, S < h, and x ≥ 2W and 2S

Figure 6.8 Coupling of Differential Traces

Reflections and Impedance Mismatches

Transmission line theory tells us that a discontinuity is created when a transmission line of characteristic impedance Z_0 forms a junction with another structure, such as a resistive load or another transmission line with different characteristic impedance. The discontinuity causes some portion of the incident wave, or voltage, to be reflected back toward the source. The reflection coefficient gives us the ratio of the reflected voltage to the incident voltage, and is defined as:

$$\rho \equiv \frac{R_L - Z_0}{R_L + Z_0} \qquad (6.5)$$

R_L is replaced by Z_{0L} when a different characteristic impedance creates the junction. In either case, it is clear that in order to prevent reflections (i.e., ρ=0), $R_L(Z_{0L}) = Z_0$ must be true. Thus, the line must be properly terminated at the characteristic impedance in order to avoid reflections.

It is also important to minimize impedance imbalances in order to reduce EMI. Complex interaction between objects of a system generate fields and that are difficult to predict (especially in the dynamic case), but certain generalizations can be made. The impedance of your signal traces should be well controlled. If the impedances of two traces within a pair are different, it will lead to an imbalance. The voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is any unavoidable impedance discontinuity introduced in proximity to differential lines should be introduced equally, to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, and PCB traces. Remember the key word is balance. ***Figure 6.9*** contains many examples of improper design practices which will cause impedances mismatches, discontinuities, etc.

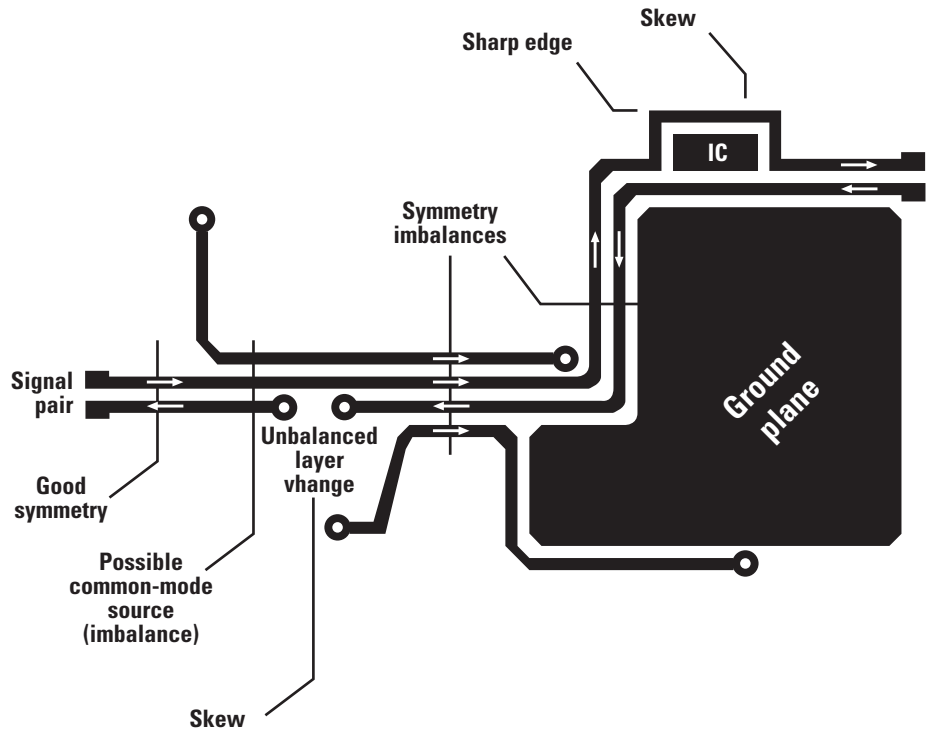


Figure 6.9 This PCB Layout Contains Many Sources of Differential Signal Imbalance That Will Tend to Increase Electromagnetic Radiation

General Design Guidelines

The remainder of this chapter provides design guidelines that supplement the design guidelines for minimizing EMI.

Avoiding Crosstalk: Trace Spacing

In the case of single-ended signals, ***Figure 6.2*** shows us that we need to maintain proper spacing between signal traces in order to avoid cross talk between nearby signals. If adjacent traces are too close, the return currents will combine and create crosstalk. Reiterating, the current density in ***Figure 6.2*** drops to about 4% when D/H = 5, and 1% when D/H = 10. This suggests that the minimum spacing between adjacent single-ended traces should be 5 times the inter-plane thickness and greater if possible.

For differential signal trace pairs, the spacing S between the traces in a pair is used to define spacing relative to other differential pairs.

- The distance between two pairs should be >2S.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.

Split Ground Planes

When the return current path remains close to the primary signal path, EM field fringing is minimized and characteristic impedance is well controlled. A common practice is to split ground planes for the analog and digital sections of a PCB. This is illustrated in ***Figure 6.10.*** The signal trace crosses the boundary between ground planes, while the return current must detour around the boundary. This increases the size of the loop area defined by the signal trace and return, creating a more effective antenna that can aggravate EMI and RFI. This also creates a discontinuity in the characteristic impedance of the pair, causing signal distortion. If it is possible to maintain good spacing between analog and digital signals, then there is no need to split ground planes. The proximity effect guarantees that the analog and digital return currents will not interfere with one another. While using split ground planes isn't necessary, it is good design practice to segregate analog and digital sections of the board.

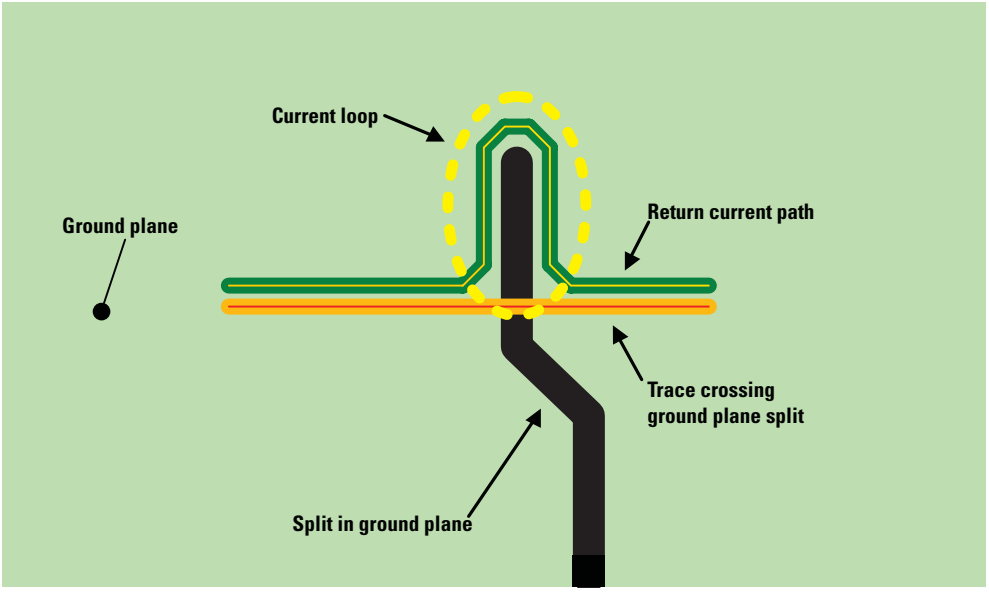


Figure 6.10 Return Current Path in a Split Ground Plane.

Minimizing Skew

If microstrip or stripline differential signaling is employed, as shown in ***Figure 6.6,*** then the return path and primary signal path are clearly paired. It is important to minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pair that appears and radiates as common-mode noise. Therefore, differential pair traces should be routed as close together as possible and as soon as they leave any IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. Signals that are 1 mm apart radiate far less noise than traces 3 mm apart, as magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver. Match electrical

lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! The following result is repeated from Chapter 5:

$$V = \frac{C}{\sqrt{\varepsilon_r}} = \text{the velocity of propagation,} \qquad (6.6)$$

where the speed of light is C = 0.2998 mm/ps and the relative dielectric constant for the transmission medium is ε_r = 4.2 for FR-4. Because we are interested in the time skew introduced by a difference in path length, it may be more convenient to consider the reciprocal of equation. The reciprocal gives us the time required to propagate the signal 1 mm, 6.84 ps. A general rule is to match lengths of the pair to within 1/20 of the signal rise time.

The fast edge rate of high speed clock signals (high effective frequencies, see ***Table 6.1***) means that impedance matching is very important – even for short runs. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI. Controlled differential impedance traces should be used as soon as possible after the signal leaves any IC. Stubs and uncontrolled impedance runs should be kept to < 1/20 of the signal rise time or not used at all. Also, avoid 90° turns since this causes impedance discontinuities by adding capacitance because the conductor width increases at the turn. Use 45° turns, radius or bevel PCB traces.

Termination

Termination to maintain signal integrity can be done in several ways, depending on the nature of the clock circuit. Parallel termination schemes place the terminating resistor(s) at the load, while series termination is used at the source (driver). For clock circuits, series termination at the source is generally not recommended, as it increases the RC time constant and slows down the clock edge, making it more susceptible to noise. ***Figure 6.11*** illustrates several possible configurations. Use a termination resistor that best matches the impedance of the transmission line, whether single-ended or differential. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. Differential signaling formats such as LVDS are not intended to work without a termination resistor.

1. Typically, a single, passive resistor across the pair at the receiver end suffices.
2. Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized.
3. Resistor tolerance of 1% or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match, the better. Match to the nominal differential impedance of the interconnect. For multi-drop/multipoint applications, match the differential impedance to the fully loaded case.
4. Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.

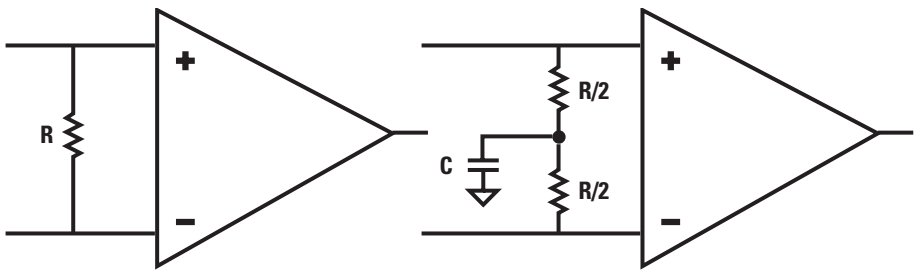


Figure 6.11 Common Differential Termination Schemes. R = 100 Ohms for LVDS/LVPECL. C = 50 pF

PCB design

1. Use at least 4 PCB board layers (top to bottom): differential signals, ground, power, single-ended signals. Dedicating planes for VCC and ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground will also create an excellent high frequency bypass capacitance.
2. Isolate fast edge rate single-ended signals from differential signals; otherwise the noisy single-ended signals may couple crosstalk onto the differential lines. It is best to put single-ended and differential signals on a different layer(s), which should be isolated by the power and ground planes.
3. When clocking a Data Converter, the clock produced by the clock conditioner should be completely isolated from all other lines, both digital and analog.
4. In layout, achieve the shortest possible length between the clock conditioner and the Data Converter clock input, and employ a straight path, if possible.

Power Supplies

Ideally, power supply and ground traces should present a low impedance to return currents. Because the impedance of an inductor is proportional to frequency, connections between the clock conditioner and the power supply that have significant inductance will not appear as low impedance to high speed clock signals. Decoupling (bypass) capacitors between the power supply and ground work by lowering the distributed impedance of the system which in turn lowers the system noise and lowers EMI. They are placed as close as possible to the clock conditioner IC in order to minimize the trace inductance. Because the impedance of a capacitor is inversely proportional to frequency, it combines with the inductance associated with power supply traces and vias to form a resonant network. Series resonance corresponds to the lowest impedance (good), while parallel resonance corresponds to high impedance (bad). Consequently, for high-speed clock conditioner designs, the values of bypass capacitors should be chosen to provide the lowest impedance at the critical clock frequencies. Unfortunately, it is not always possible to determine the appropriate values through analysis. Hence, multiple capacitors of different values are often the best choice for bypassing because up to a point, they can broaden the low impedance frequency range. After the circuit is prototyped, the actual performance of the bypassing can be measured and the capacitor values adjusted.

1. To create low impedance paths for power and ground, use power and ground planes. If you must use traces, use wide traces because inductance is inversely proportional to trace width. Use multiple vias in parallel to reduce inductance. Maintaining characteristic impedance for power supply traces is not necessary.
2. Provide a return path that creates the smallest loop for the image currents to return. For example, ground pins should be individually connected to the ground plane, rather than daisy chained (this increases loop size, increasing inductance). Use multiple, regularly spaced vias to minimize inductance to the power planes.
3. Use bypass capacitors at each IC in the circuit. For best results, the capacitors should be placed as close as possible to the VCC pins to minimize parasitic effects that defeat the frequency response of the capacitance. Two or Multi-Layer Ceramic (MLC) surface mount capacitors (0.1 μF and 0.01 μF) in parallel should be used between each V_{CC} pin and ground if possible.
4. Use two vias to connect to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

Clock Traces

1. Use coupled differential traces whenever possible. Single-ended traces should be spaced no closer than 5h (h = dielectric layer height), and farther if possible. Minimize parallel runs between the clock trace and any other signals. Use shield traces (or copper fill) on both sides of the clock trace. However, the trace routing must maintain balanced spacing along the entire path. Vias from the shield trace (copper fill) should be spaced less than 1/4 λ apart.
2. For clock traces, straight is best. If a change of direction is unavoidable, use 45º bends rather than 90º to minimize reflection. Try to use an even number of right and left bends to minimize differential to common mode conversion from skew due to differences in trace length.
3. Do not route clock traces through different layers, as vias create an impedance discontinuity and hence, reflections. If an inner layer is used to route clock signals, sandwich it between reference planes if at all possible.
4. Proper termination is absolutely required. Termination at the receiver end is preferable.
5. Use point-to-point routing for clock traces if possible. Techniques such as daisy-chain routing are not recommended.
6. Traces for differential clock signals should be closely coupled to maintain common-mode rejection at the receiving end and designed for the appropriate impedance, typically 50 ohms (single-ended) or 100 ohms for differential impedance. The spacing between the trace pair should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.
7. Edge-coupled microstrip lines offer the advantage that a higher differential Z_0 is possible (100Ω to 150Ω). Also, it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.
8. Stripline may be either edge-coupled or broad-side coupled lines (see ***Figure 6.6***). Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect to them. Broadside coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector pin field. Remember, there is no closed-form equation for calculating the impedance of broadside-coupled stripline. Instead, a field solver should be used.
9. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.
10. When designing for a specific differential Z_0 (Z_{DIFF}) for either microstrip or stripline edge-coupled lines, it is best to adjust trace width "W" to alter Z_{DIFF}. It is not recommended to adjust "S" (spacing) which should be the minimum spacing specified by the PCB vendor for line-to-line spacing. Keeping "S" to a minimum enhances the coupling between the traces reducing EMI.
11. PCB Trace width and spacing design can be done using computer software. Various PCB manufacturers will have software available to calculate recommended trace dimensions for microstrip and stripline traces. Better yet, software such as 2D field solvers can be used to calculate trace impedances which can account for variables such as the solder mask layer over the copper trace and the trapezoidal shape of the actual copper trace (a result of the etching process as seen in ***Figure 6.12***). Accounting for the solder mask lowers the impedance of the traces as it increases the effective permittivity. Accounting for the trapezoidal shape of the traces increases the impedance of the traces.

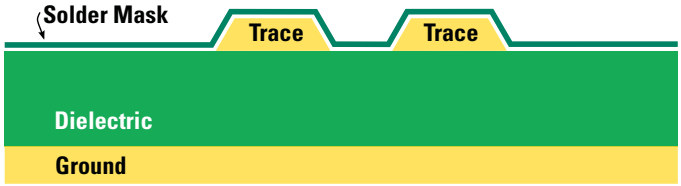


Figure 6.12 Detailed View of Differential Traces

Common values of dielectric constant (ε_r) for various printed circuit board (PCB) materials are given in ***Table 6.3.*** Consult the PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most high-speed applications, the widely used FR-4 PCB material is acceptable. GETEK is about 3 to 4 times as expensive as FR-4 and ROGERS4003 can be 3 times as expensive as GETEK, but can be considered for 1000+ MHz effective frequency designs. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew.

Table 6.3 Dielectric Constants and Loss Tangents for Several PCB Materials

PCB Material	Dielectric Constant (ε_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1 to 2.5	0.0002 to 0.002
BT resin	2.9 to 3.9	0.003 to 0.012
Polyimide	2.8 to 3.5	0.004 to 0.02
Silica (quartz)	3.8 to 4.2	0.0006 to 0.005
Polyimide/glass	3.8 to 4.5	0.003 to 0.01
Epoxy/glass (FR-4)	4.1 to 5.3	0.002 to 0.02
GETEK	3.8 to 3.9	0.010 to 0.015 at 1 MHz
ROGERS4350 core	3.48 ± 0.05	0.004 at 10 GHz, 23ºC
ROGERS4403 prepreg	3.17 ± 0.05	0.005 at 10 GHz, 23ºC
ROGERS4003 core	3.38 ± 0.05	0.0027 at 10 GHz, 23ºC
PSR-4000BN Silkscreen	4.5	0.0290 at 1 MHz
PSR-4000MP Silkscreen	4.7	0.0220 at 1 MHz

Conversion from Single-Ended to Differential Signaling

Clock conditioners often include or interface to oscillators, which are usually handled as single-ended devices. The clock conditioner output itself may be single-ended. However, the clock conditioner output often drives a differential input, such as an ADC clock input or a clock distribution IC. Therefore, conversion from single-ended to differential is required. One way to do this is to use a RF transformer also known as a balun.

Center-Tap Baluns

Mini-circuits ADT2-1T and ADT2-1T-1P are examples 50:100 ohm impedance baluns which work well for translating from an unbalanced 50 ohm impedance to a balanced 100 ohm impedance or vice-versa. These baluns provide DC isolation and typically operate at lower frequencies. An example schematic is shown in ***Figure 6.13.***

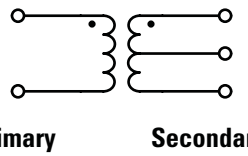


Figure 6.13 Schematic of a Center-Tapped Balun

Guanella Baluns

Mini-circuits ADTL2-18 is an example of a 50:100 ohm impedance Guanella balun. Many Guanella baluns have 1:1 or 4:1 impedance matching for which extra care will be needed in designing the trace impedances and terminations. These baluns do not provide DC isolation and typically operate at high frequencies and have wide bandwidths of operation. An example schematic is shown in ***Figure 6.14***.

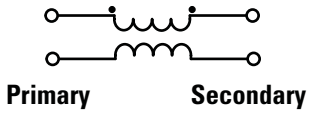


Figure 6.14 Schematic of a Guanella-Type Balun.

AC-Coupling

Why would you want to AC-couple a signal?

- To change the DC bias voltage when interfacing logic families with different input thresholds (such as optical systems where LVDS and PECL are used), or
- To protect drivers from possibly getting shorted when used in a removable interface (such as on cards used in network switches and routers), or
- To prevent DC currents flowing between systems with different ground potentials.

If your application meets one of these requirements and you are using encoded data, use AC-coupling. AC-coupling works best with encoded data that provides an equal number of ones and zeros (a DC-balanced signal). Some examples of DC-balanced signals are 50% duty-cycle clocks, 8b/10b coding, and Manchester-coded data. For signals with good DC-balancing, the useful spectral content of the data usually has a low frequency cutoff, and it is possible to pass the information with minimal degradation in content. However, for any signal passed through an AC-coupling circuit, you should expect a small portion of the signal to be filtered out. When AC-coupling is used, the DC common-mode bias voltage used in LVDS and many other logic families is lost. Although many devices have a wide common-mode operating voltage range, this should be verified in the device's datasheet. For devices limited in common-mode operating range, a simple bias circuit can be used to properly bias the signal. The most common method of AC-coupling is to use a DC-blocking capacitor. For high-speed designs, the smallest available package should be used. This will help minimize degradation of the signal due to package parasitics.

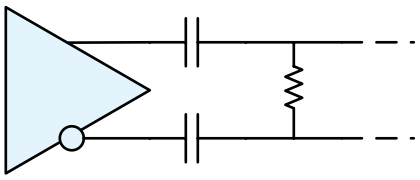


Figure 6.15 AC-Coupling

To find the appropriate capacitor value to use, you can use the following equation as a rough approximation:

$$C = \frac{T_b \cdot N \cdot 10^{\left(-\frac{droop}{20}\right)}}{2\pi R\left[1-10^{\left(-\frac{droop}{20}\right)}\right]} \approx \frac{34 \cdot T_b N}{2\pi R} \quad (6.7)$$

C = DC block capacitor value
T_b = bit period
R = impedance
N = the maximum number of consecutive identical bits
droop = max droop in dB allowed

Every AC-coupled signal will have some droop in amplitude when passed through a capacitor. The equation listed above takes into account a 0.25 dB droop. The most commonly used capacitor values found in high-speed applications are 0.1 µF (low as 500 kHz at 50 ohms, 250 kHz at 100 ohms) and 0.01 µF (low as 5 MHz at 50 ohms, 2.5 MHz at 100 ohms) capacitors. These capacitors are easy to find and have sufficient bandwidth to support most high-speed data rates. For applications where edge rates are very fast, placing the AC-coupling capacitors closer to the receiver inputs may provide better results since edge rates will be slower. In general, for logic interconnects within the same PCB, a simple DC-coupled interface is best. If AC-coupling must be used, then make sure that DC-balanced data is used.

Summary

Fundamentally, managing and controlling EMI means managing: (1) the coupling between the primary signal path and return path, and (2) the balance between primary signal path and return path. The balance between the paths encompasses length and impedance discontinuities. Practices that minimize radiated interference also help to minimize susceptibility to interference. Distortion results when the impedance of signal traces is not controlled and when signal paths are incorrectly terminated.

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Notes

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