WHITE PAPER

David A. Rice,
Technical Director
Critical Link, LLC

Joseph Coombs,
Applications Engineer
TMS320C6000™ Digital Signal Processors
Texas Instruments

TEXAS INSTRUMENTS

MityDSP®-L138F Software Defined Radio Using uPP Data Transfer

The problem

Critical Link was approached by a customer who needed to develop a spread-spectrum radio transceiver for several applications. The customer had already developed the algorithms they intended to use to modulate and demodulate the signals but lacked the resources and expertise to put together the complete system. The customer wanted to take advantage of the extreme flexibility offered by software defined radio (SDR) systems.

The platform

Critical Link chose to use its MityDSP-L138F **system-on-module** as the basis for the SDR, since it was a good fit from a processing-horsepower point of view, and it would save the customer a significant amount of up-front design cost. The MityDSP-L138F module features a Texas Instruments Incorporated (TI) OMAP-L138 **DSP**+ARM® processor, which integrated a 456-MHz ARM9™ processing core and a 456-MHz TMS320C674x DSP core. The module also includes a Xilinx Spartan®-6 LX16 **FPGA**, along with NAND and NOR flash, and DDR2 memory.

For prototype purposes, TI's evaluation kits for the high-speed ADC and DAC for the radio were used. Data converters capable of converting at 60-MHz sample frequency were required.

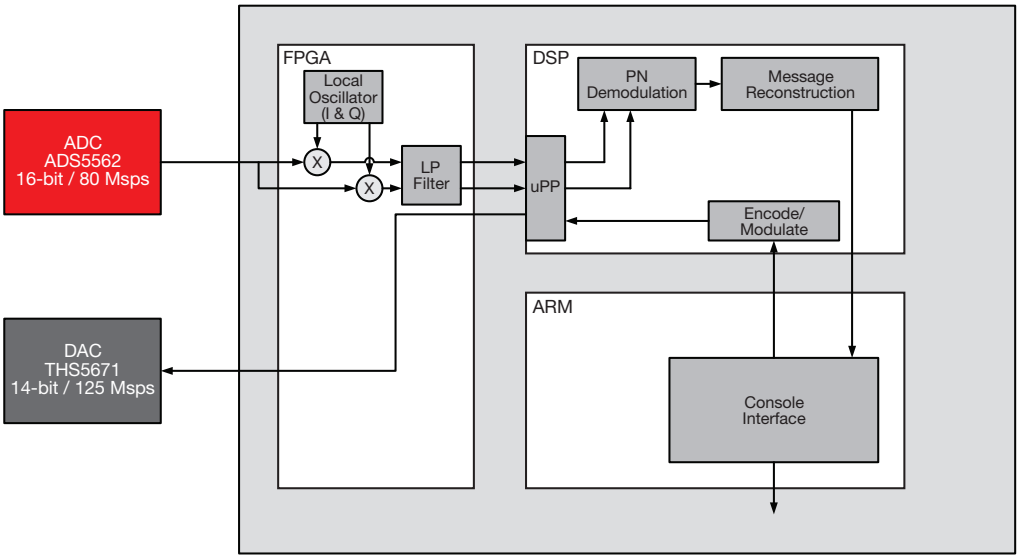
For the A/D converter, TI's ADS5562 was selected, which will convert at 80 Msps with 16 bits of precision. Since spread-spectrum radios need to pull signals out of the background noise, high dynamic-range is very important for such a radio.

For the DAC, TI's THS5671 was selected, a 14-bit, 125-Msps differential current output DAC. The customer for this project provided the front end design for the system, as shown on the following page.

The data movement problem

Many DSP-based applications require high-speed data transfers to allow the system to acquire and process data or to transmit data to an external device. Typically, digital signal processors include an asynchronous address/data bus to allow the processor to read and write to external devices. These interfaces are often adequate to move data at low rates, but can become a bottle neck at high speeds.

The OMAP-L138 DSP+ARM processor has an address/data bus called the External Memory Interface A (EMIFA). The EMIFA allows addressing external memory or devices



Customer provided front-end design

asynchronously and includes several control pins to allow for varying wait-states, transfer widths, etc. Because this interface is very general purpose, each transaction can take multiple clock cycles to complete. The minimum read cycle, for example, would require three cycles per 16 bits. Running the EMIFA at 100 MHz, you can expect a data transfer rate of no more than 66 MBytes/s, assuming nothing else is going on that bus. Interleaving reads and writes on the bus significantly reduces this, since additional turnaround cycles must be added.

The OMAP-L138 processor also includes a more dedicated interface, known as the Universal Parallel Port (uPP). This interface is specifically designed to move large amounts of data continuously into or out of the processor's memory. The uPP can clock one data word (8 or 16 bits) per clock cycle (or two per clock for double-data-rate, but the clock speed must be half as fast). The uPP clock rate can be up to half of the processor clock rate. For an OMAP-L138 processor running at 300 MHz, the uPP clock can be up to 75 MHz. This allows a throughput of up to 150 MBytes/s.

The OMAP-L138 processor actually includes two uPP interfaces, each of which can be configured independently. For our application, this allowed us to set up one port for transmit and one for receive, thus removing contention that would be present on a single bus.

From a hardware point of view, the uPP interface is a fairly simple synchronous data interface. It includes a clock pin, data pins and several control pins that indicate valid data and start/wait conditions. In fact, the interface can be used gluelessly with some parallel ADCs and DACs.

The architecture

Since our SDR requires high-speed data movement to and from the DSP, we chose to implement the FPGA interface using the uPP ports. We use one port for the transmit side of the interface and one for the receive side. The processing system is actually able to transmit and receive simultaneously, although that was not a system requirement. A nice benefit of this capability was that it allowed us to do quite a bit of testing and debug by looping back the transmitter to the receiver.

For a 10 MHz carrier, the nature of the processing required for this type of modulation make doing all of the processing in the DSP too much for the OMAP-L138 processor. For slower applications, the DSP alone could handle the data rate, but since this customer needed to be able to send data at the higher rate, we needed to enlist the help of the FPGA for some of the processing tasks.

The FPGA is particularly good at repetitive tasks at very high frequencies, so we chose to do the initial demodulation and base-banding process in the FPGA, which then allows us to decimate the data and reduce the data rate to the DSP. On the transmit side, the DSP can pre-compute the final RF signal, so that encoding the payload data takes an inconsequential time. For this reason, the FPGA merely passes the transmit waveform data from the uPP port to the DAC.

The FPGA includes a sine/cosine lookup table in dual-ported RAM, which is used to synthesize the local oscillator signals for the receiver. Multiplier/accumulators in the FPGA are used to demodulate the signals, as required.

Transmit processing chain

The transmit process is started when the software on the ARM microprocessor sends a message packet to the DSP for transmission. The DSP encodes this data into a spread-spectrum modulation sequence and indexes into a pre-computed, modulated, sine-wave look-up table. The DSP then sets up a DMA transfer, using the uPP's built-in DMA engine, to transfer the data from the DSP memory into the DAC. The FPGA acts as the intermediary, providing a programmable clock to the DAC and uPP to set the transmit sample rate.

Receive processing chain

The receive process runs continuously. ADC samples are clocked into the FPGA, where the data is base-banded by multiplying the input samples by quadrature sine and cosine waveforms and integrating to provide in-phase and quadrature samples at a reduced data rate to the DSP. These samples are DMAed into the DSP memory by the uPP DMA engine, where the DSP performs the remaining processing steps for the spread-spectrum demodulation. Once the signal is demodulated, the resulting data packet is then transferred back to the ARM® processor using TI's DSPLink interprocessor communications library. The ARM software receives the decoded data and presents it to the user via the command interface.

Using the FPGA to perform the initial base-banding for the receiver relieves the DSP of enough processing to allow all of the remaining demodulation and decoding to be done with ease. If the sample rate of the input

signal was significantly lower than the 60 MHz in this system, the DSP could be counted on to do the base-banding without help from the FPGA.

Initial work on this system used a carrier frequency in the LF band (tens or hundreds of kHz). The FPGA in this initial implementation was merely passing data through to the DSP, and the DSP performed all of the demodulation functions. This worked quite well, but was insufficient for applications where higher sample rates were required. By doing the base-banding in the FPGA, we can base-band and filter digitally at the full sample rate, thereby improving the noise performance of the system in a way which isn't possible by merely under-sampling.

Conclusion

The end result of this project was a prototype system that has been used as a proof-of-concept for several applications. The performance of the system has been quite good, when compared to the theoretical performance of an ideal spread-spectrum radio. The combination of TI's OMAP-L138 DSP+ARM® processor and the FPGA allows for a cost-effective solution with outstanding performance. Off-loading processing from the DSP to the FPGA allows the system to be built using a low-cost, low-power processor, rather than requiring a GHz-class DSP to do the entire job. The uPP interface allows simple FPGA interfacing and boasts significant performance advantages over using other available interfaces on the DSP. Relieving the DSP of data movement by using the DMA in the uPP also helps keep DSP cycles available for more important work.

The addition of the ARM processor in the OMAP-L1x platform allows the use of embedded Linux® to provide the communications infrastructure to manage the user interface and all housekeeping functions in the system. Furthermore, the system software (ARM, DSP and FPGA) can be field-upgraded using an SD card, a USB drive or an Ethernet connection. Thus the flexibility of the SDR system can be fully leveraged as processing algorithms evolve.

Additional information

http://www.mitydsp.com/upp

Related products

MityDSP: **http://www.mitydsp.com**

MityDSP-L138F: **http://www.mitydsp.com/mitydsp-l138f**

OMAP-L138 processor: **http://www.ti.com/omapl138**

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265