Application Report
SPNA087A–September 2011

3.3 V I/O Considerations for Hercules™ Safety MCUs in Automotive and Industrial Environments

ABSTRACT

As new generations of microcontrollers lower their supply voltages from 5 V to 3.3 V and beyond, issues with interfacing and noise are increasing. This application report presents cost-effective interfacing techniques for inputs and outputs of 3.3 V microprocessors in an automotive environment. In addition, concerns about 3.3 V analog-to-digital converters (ADC) are discussed.

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1 Introduction

To stay competitive, new generations of devices must shrink their geometries. Part of this shrinking process requires the transistor's gate oxide to be thinned to maintain speed and drive strength. To restrict voltage stress on the transistor's oxide, the supply voltages must be lowered proportionately. This gives rise to the 3.3 V microprocessor.

While it is possible to place level shifters inside the microprocessor, this adds considerable complexity to the device's processing; thus, increasing cost. It is generally more cost-effective to provide level-shifting logic externally.

In an automotive environment, many pins already have passive signal conditioning circuitry. In this case, it is a simple matter of adjusting the ratios of the components already present. In some cases, inputs and outputs will be compatible with no alterations. Typically, only a few pins will require additional components in order to provide compatibility with surrounding circuitry.

2 Supplying Power

The device requires 3.3 V for power, so in systems with older technology 5 V parts, the power supply will have to support dual rail 3.3 V and 5 V supplies.

As always with digital circuitry, minimize noise by close-coupling a small ceramic capacitor between each pair of V_{CC}/Gnd pins. Make the area encompassed by the routing as small as possible, and run power and ground lines as closely spaced to each other as practical to minimize loop areas. The larger the loop area, the larger the antenna that can radiate noise (EMI).

3 Inputs

There are numerous types of input signals that need to be interfaced to a microprocessor's input pins. Some originate from within the user's module and need little protection from extreme conditions, while others originate outside and may be subjected to high voltage stress. Several different types of interface situations are covered here.

NOTE: On automotive microcontrollers, input pins usually have internal pull up or pull down circuits. These circuits approach ideal current sources given a fixed V_{CC}. As such, they will not affect impedance calculations (RC time constants); however, they can substantially affect DC bias calculations. Be sure to check the device-specific data sheet for which pins have pull ups and pull downs and for their rated current specifications before making bias calculations. The following examples do not take into account these current sources in order to simplify discussions.

3.1 5 V TTL to 3.3 V CMOS

The V_{OH} level of TTL outputs is typically 3.4 V at rated current, and 4.05 V at no-load and VCC5_max of 5.25 V. Similarly, the tolerable V_{IH} on a 3.3 V I/O Hercules Safety MCU device is (VCC3 + 0.3 V). Since the worst-case differential voltage between the devices is assumed, VCC3 = 3.0 V is set, therefore, the maximum differential voltage is 0.75 V.

For instance, if you wanted to limit the current to 75 uA, then placing a 10K Ω resistor between the TTL output and 3.3 V CMOS input will suffice. This will create a small RC delay of about 10K*5pF = 50 nS. This delay should be negligible in most cases except perhaps for network transceiver interfaces (CAN, Flexray, etc.), which are subject to a maximum round-trip time.

This same technique will work exactly the same for an open emitter pull-up, except that the falling time constant will be longer considering that there is now a transistor emitter capacitance to deal with during fall time.

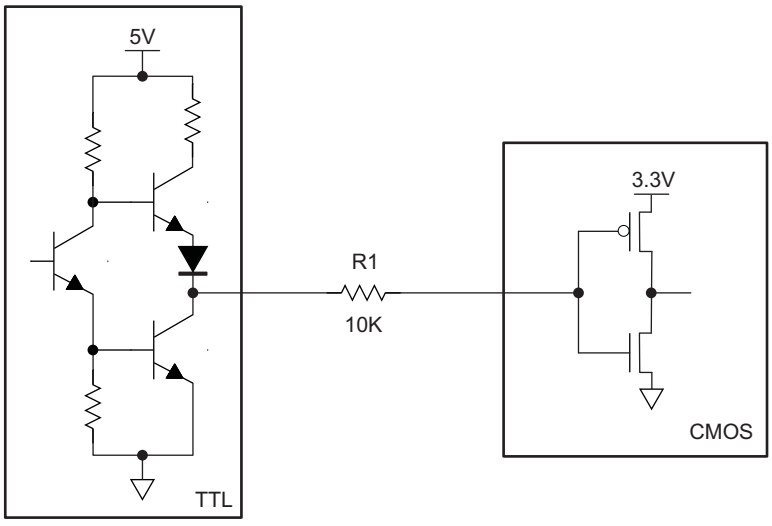

Figure 1. 5V TTL to 3.3V CMOS

3.2 5 V CMOS to 3.3 V CMOS

Using the same analysis as above, the V_{OH} level of 5 V CMOS outputs is typically 5.25 V at no-load and with a VCC5_max of 5.25 V. Therefore, the maximum differential voltage is 1.95 V, which presents a slightly more difficult problem. In this case, a resistor divider network needs to be added such that an input of 5.25 V will give out 3.0 V. Since the divider is referenced to ground, 0 V in will yield 0 V out.

Using the same argument from above that 10K input impedance yields an acceptable time constant, the two resistors can be calculated: R1 = 18K and R2 = 22K. Using these values, a 5.25 V output will yield 2.9 V to the CMOS input. The L_{OH} current will be limited to 130 µA and the impedance seen by the CMOS input will be 9900 Ω.

This same technique will work exactly the same for an open-drain pull-up, except that the falling time constant will be longer considering that there is now a transistor drain capacitance to deal with during fall time.

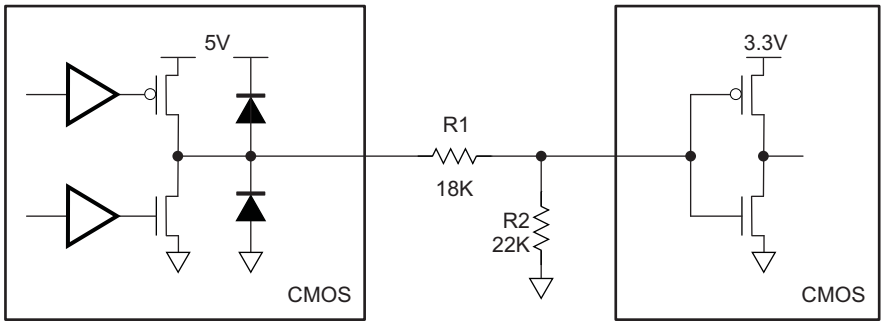

Figure 2. 5V CMOS to 3.3V CMOS

3.3 Open Drain / Open Collector Pull-Down to 3.3 V CMOS

This type of input requires a pull-up resistor sourced by the 3.3 V power rail. Considering the significant increase in capacitance due to the drain/collector junction ($C_{junction}$), the rise time is slowed unless the pull-up resistor is reduced from the usual 10K Ω.

Tr = Rpu * (5pF + Cjunction)

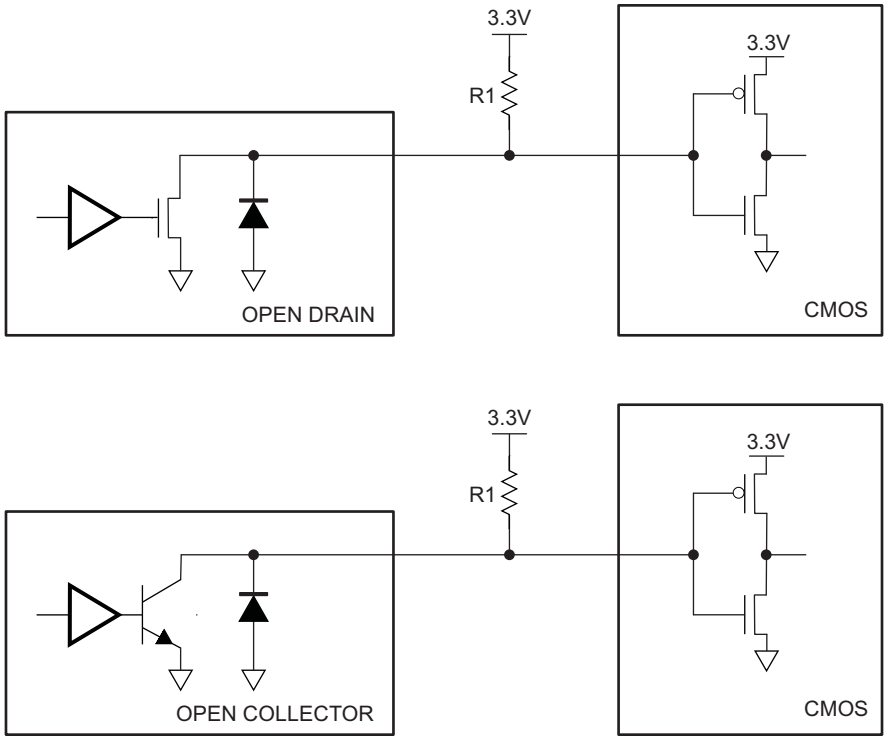

Figure 3. Open Drain / Open Collector Pull-Down to 3.3 V CMOS

3.4 High Voltage to 3.3 V CMOS

Higher voltages (12 V to 18 V) typically come from outside the module. Any type of signals coming from outside the module must have signal conditioning circuitry to limit noise spikes that can damage the device from over current or over voltage.

Usually these circuits take the form of a voltage divider similar to the 5 V CMOS to 3.3 V CMOS case above except that a capacitor must also be included from the device pin to ground to limit voltage transients. Typically, test methods for automotive circuits require the inputs to survive 200 V spikes of prescribed waveshapes.

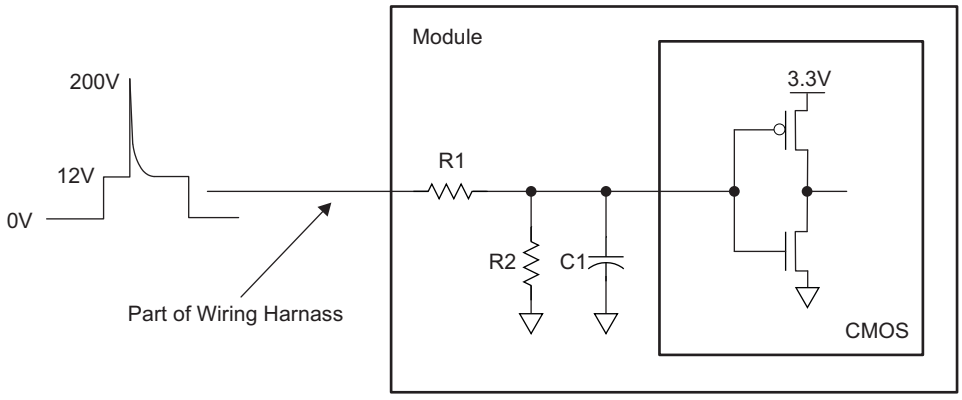

Figure 4. High Voltage to 3.3V CMOS

The divider network R1/R2 is set to translate 18 V down to 3.3 V. 18 V is the maximum dc voltage that the module expects to see from the charging system, even though 12 V is typical when the engine is off, and cranking volts can be as low as 4 V. R1 must be set large enough to avoid exceeding the device pin's maximum input clamp current in the event that some rocket scientist uses double battery (24 V) to crank the vehicle in the winter. The time constant of the parallel resistance (R1||R2) in combination with C1 is set to absorb the 200 V spike without overstressing the input as well. It can quickly be observed that there are more constraints than there are variables (if 4 V is a marginal "one" then 18 V will certainly forward bias the input clamp circuit.)

4 Outputs

Like the inputs, outputs may need translation to other technologies or voltage levels. Examples of various output interfaces are shown in the following sections.

4.1 3.3 V CMOS to 5 V TTL

There is nothing to do here. The V_{IH} and V_{IL} for TTL are 2.0 V and 0.8 V, respectively. This gives plenty of margin to the loaded 2.8 V to 0.4 V swings of the 3.3 V CMOS output buffer.

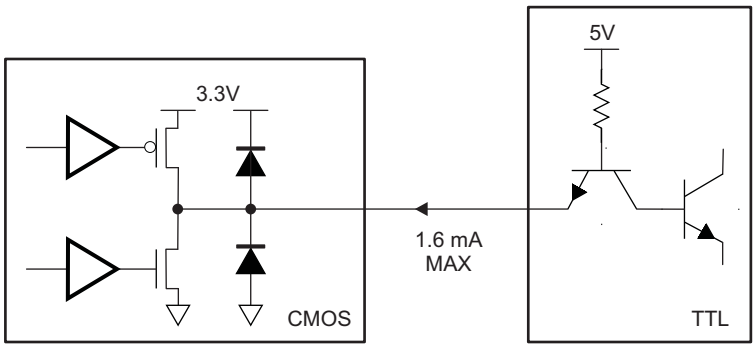

Figure 5. 3.3V CMOS to 5V TTL

4.2 3.3 V CMOS to 5 V CMOS

Going from 3.3 V CMOS to 5 V CMOS requires level shifting. In Figure 6, R1 and D1 provide a 0.6 V upward shift of the CMOS output's voltage. With R1 around 10K, the CMOS output buffer swings from about 0.2 V to 3.3 V. At the diode's anode, it swings from about 0.8 V to 3.9 V. The 5 V CMOS input thresholds are 1.0 V and 3.5 V, which gives a margin of 0.2 V and 0.4 V, respectively. Here, there will be a small rise-time delay due to the RC time constant of R1 and the node capacitance, Cn.

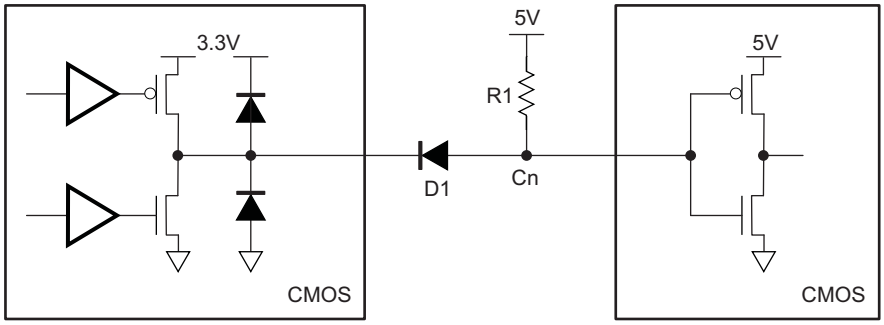

Figure 6. 3.3V CMOS to 5V CMOS

4.3 3.3 V CMOS to Bipolar

The circuit in Figure 7 is the same whether the output driver is 3.3 V or 5 V; however, the resistors need to be resized to match the lower V_{OH} to the required base-drive current.

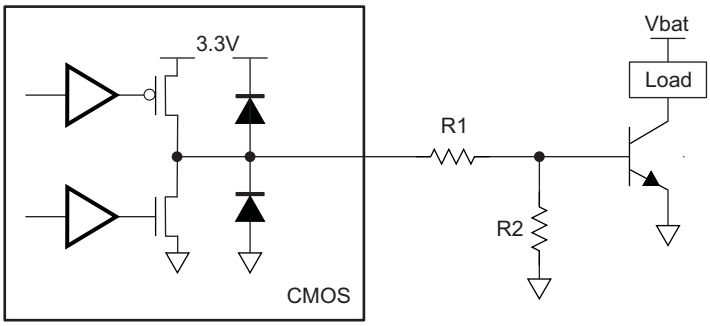

Figure 7. 3.3V CMOS to Bipolar

4.4 3.3 V CMOS to MOSFET

This is the most troublesome of the conversions. Many MOSFETs available require more than 3.3 V on their gate to saturate at the required load current. Newer MOSFETs are becoming available but at a premium.

One low-cost technique is to use a standard 5 V CMOS buffer such as the 74AHCT04 HEX inverter or the 74AHCT241 Octal Buffer to translate the 3.3 V CMOS output up to a 5 V CMOS level. These devices are available in automotive temperatures for around $0.10 each and one device will translate 6 or 8 outputs.

In this implementation, R1 is a gate pull-down for safety purposes.

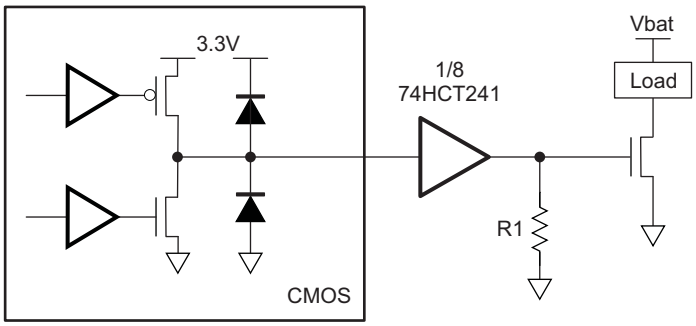

Figure 8. 3.3 V CMOS to MOSFET

5 Analog to Digital Converter Inputs

There are two primary issues with using a 3.3V ADC compared to a 5 V ADC: the effect upon signal-to-noise ratio and changes to the interface circuitry.

5.1 Signal-to-Noise Ratio

First, there is the noise that rides the signal at the input to the module. It can easily be seen that noise from outside the module is scaled at the same rate as the signal; therefore, when scaling the signal down from 5 V to 3.3 V, the signal-to-noise ratio remains constant.

Second, there is the switching noise generated by the microprocessor and coupled into the ADC via the substrate or near-field EMI. Given that the noise is constant, moving to a 3.3 V ADC would make the signal-to-noise ratio worse; however, in actuality moving the microprocessor from 5 V to 3.3 V has the effect of reducing generated noise. While it is not easy to deduce if the reduction in noise offsets the increase in the 3.3 V ADC's sensitivity to it, it is the designers' goal to hold this source of signal-to-noise constant, if not to reduce it.

Therefore, it can reasonably be stated that the effect of migrating to 3.3 V is not an issue with respect to signal-to-noise ratio.

5.2 Interfacing to a 3.3 V ADC

Just as in the case of high voltage to 3.3 V CMOS, it is a simple matter of adjusting the resistor ratio to accommodate the lower Vrefhi conversion value. Figure 9 shows an example of a typical interface.

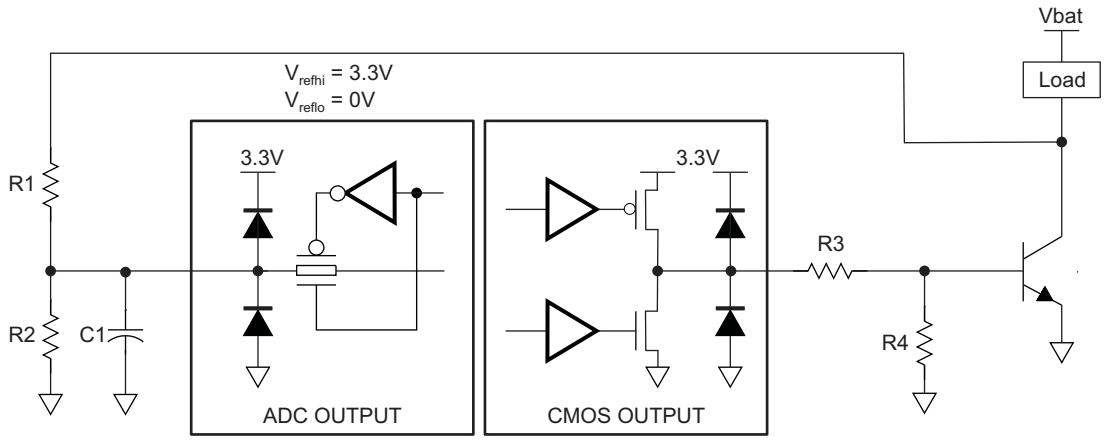

Figure 9. 3.3 V ADC Example - MOSFET Monitor Circuit

The MOSFET saturation voltage is fed back to one ADC input channel as a monitor. The ADC can then make the determination if the system load develops an overload condition or an open circuit. C1 is sized to suppress load transients as described previously.

6 References

High Speed Digital Design, A Handbook of Black Magic Howard Johnston, Martin Graham, 1993 Prentice-Hall, ISBN 0-13-395724-1.

Advanced CMOS Logic Data Book (SCAD001)

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