Using IBIS Models for Timing Analysis

C6000 Hardware Applications

ABSTRACT

Today's high-speed interfaces require strict timings and accurate system design. To achieve the necessary timings for a given system, input/output buffer information specification (IBIS) models must be used. These models accurately represent the device drivers under various process conditions. Board characteristics, such as impedance, loading, length, number of nodes, etc., affect how the device driver behaves. This application report discusses how to properly use IBIS models to attain accurate timing analysis for a given system. This report focuses on the use of SDRAM with a TMS320C6000™ DSP, but is applicable to all interfaces that have setup and hold parameters.

Contents

List of Figures

List of Tables

1 Introduction

Digital signal processors (DSPs) and memories are tested to specifications given by their respective data sheets. These tests are performed under specific operating conditions given by the data sheets. Any variation from these specific operating conditions will cause a change in behavior from which the device was tested. These operating conditions include temperature, voltage, frequency, capacitive loading, impedance, etc.

Input/output buffer information specification (IBIS) is a fast and accurate way of modeling a buffer's behavior over all process conditions. IBIS models are generated based on V/I curves derived from full-circuit simulations and/or bench-top testing. In order to use IBIS models, a simulation package, from companies such as Hyperlynx or Mentor Graphics, must be purchased. These simulation packages give accurate information on signal integrity issues that may occur based on system, board, and component-level characteristics.

For example, a DSP tester has a given test load. If a board has more or less loading than that of the tester, the timings will be skewed from what was originally intended. This can hurt or help the system, depending on which way the timing is skewed, and what parameter is of concern.

Important to this application report is that of impedance and loading. It is assumed that frequency remains constant, the voltage remains well within the data sheet specification range, and the temperature remains at or near room condition (well within the specification limits, normally 0°C and 90°C).

Systems that use multiple sychronous dynamic random-access memory (SDRAM) chips to fill the bus width will have to do IBIS simulations on each component. This must be done since there is no longer a point-to-point connection between the DSP and the SDRAM. The variations in trace lengths create differences in timings between the multiple components. Users must perform IBIS simulations to ensure signal integrity.

This application report discusses the various reference points for timings that are important to both the DSP and the SDRAM. In section 3, an overview of the tester used to test the DSP and/or the SDRAM is given along with an explanation of the timing variation between the tester and a typical board. Reference voltages and noise margins impact the timings presented by both the tester and a typical board. An understanding of why this occurs is briefly discussed in sections 4 and 5. Section 6 of this application report encompasses the formulas used to establish setup and hold times for both the DSP and the SDRAM, based on IBIS Simulations. Section 7 summarizes the AC timing analysis procedures.

2 Establishing a Reference Point

Data sheet timings are measured from the pins of the device connected to the test board with a given tester load. On a real system board, these timings change as loading increases or decreases from the loading on the tester board. Before going into further details (in section 3) on how timings differ on a real system board versus the test board, this section discusses how to establish a reference point. A reference point must be established when modeling a board that varies from the original test board model. As a matter of convenience, the reference point is taken from just inside the master device, the DSP. The reference point represents the time in which the DSP output buffer is enabled.

Figure 1 gives a high-level drawing of how a DSP write to SDRAM can be represented in a real system board. The point, denoted by t_0, is the point in which all timings will be referenced. The points A, B, D, and E are measured at the pins of the DSP and SDRAM, respectively. Point F describes the point at which the output buffer turns on relative to time t_0. X_n is an internal timing delay that is represented by a constant value, fixed by the design of the DSP. Assume that the design of the DSP sets X_n to –3.1 ns. Also assume that the output buffer at A had an internal delay of 0.2 ns, and the output buffer at D had an internal delay of 0.3 ns. Calculations would show that the time at point A is (t_0 + 0.2) ns, or simply 0.2 ns relative to t_0, Similarly, calculations would show that the time at point D is (t_0 + X_n + 0.3) ns = (t_0 – 3.1 + 0.3) ns, or simply –2.8 ns relative to t_0. The output setup time for the DSP is calculated from when the data transitions at point D, to when the clock transitions at point A. In this case, the output setup time is [0.2 – (–2.8)] ns = 3 ns.

X_n will be different for hold times, since this uses different internal logic to gate the buffers.

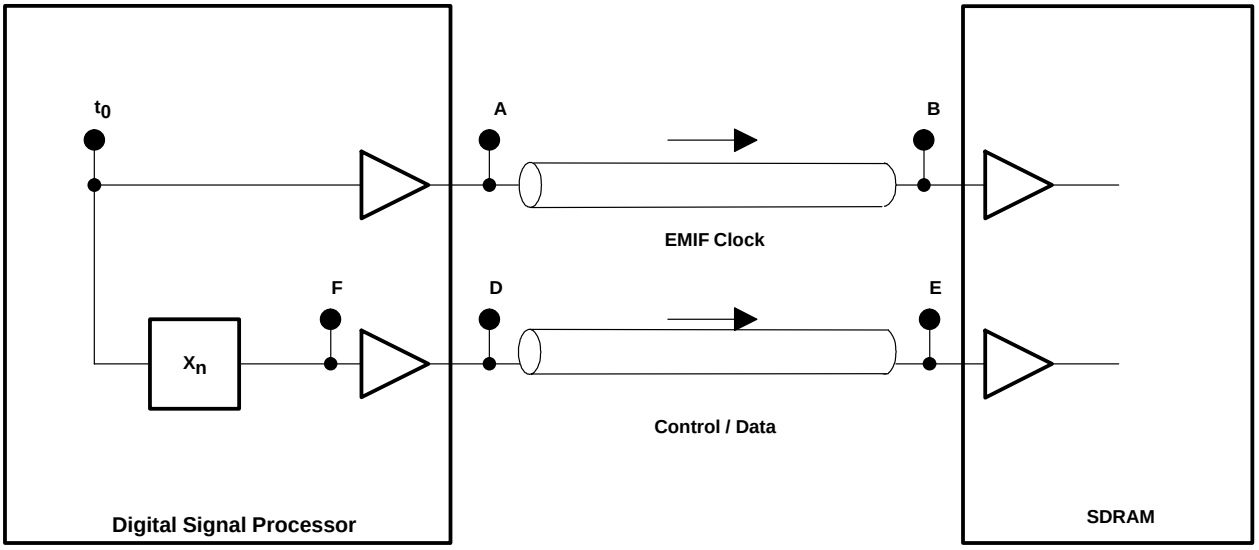


Figure 1. DSP Writes (Control Signals and/or Data Signals)

In the case of DSP reads, the DSP outputs the clock, control, and address signals as shown in Figure 1. Upon receiving the read command, the SDRAM outputs the data signals. Figure 2 gives a high-level drawing of how the SDRAM outputs data relative to the clock from the DSP. Y_n represents the internal timing delay generated by the SDRAM. The SDRAM measures input and output timings with respect to the clock signal at the pin of the device. For example, the output hold time of the SDRAM starts as soon as the clock signal at point B passes a given reference voltage, V_{ref}. The hold time ends at point D as soon as the signal crosses V_{ref}. Assume that the output hold design of the SDRAM sets Y_n to 1.8 ns. Also assume that the input buffer at B has a delay of 0.3 ns, and the output buffer at D has a delay of 0.4 ns. Calculations would show that, in Figure 2, the time at point D relative to point B is [0.3 + Y_n + 0.4] ns = [0.3 + 1.8 + 0.4] = 2.5 ns, giving an SDRAM output hold time of 2.5 ns in this example.

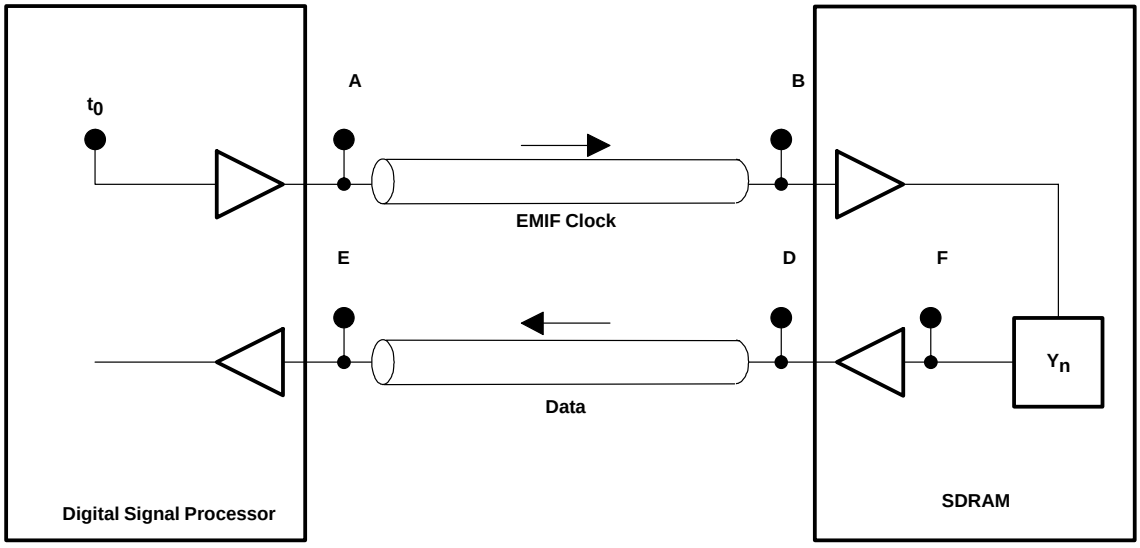


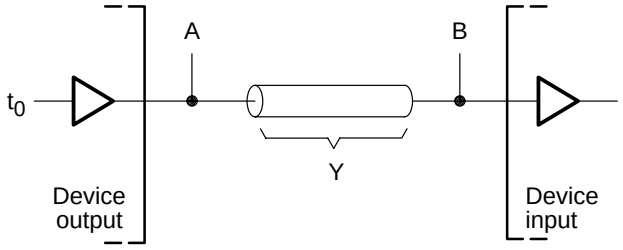
Figure 2. DSP Reads (Data Signals Only)

Both the DSP and the SDRAM measure input and output timings with respect to the clock signal at the pin of the device. Output times are measured when V_{ref} is crossed at the data/control signal relative to when V_{ref} is crossed at the clock. Input times are measured when the data/control signal goes valid (setup times) or invalid (hold times) relative to when V_{ref} is crossed at the clock.

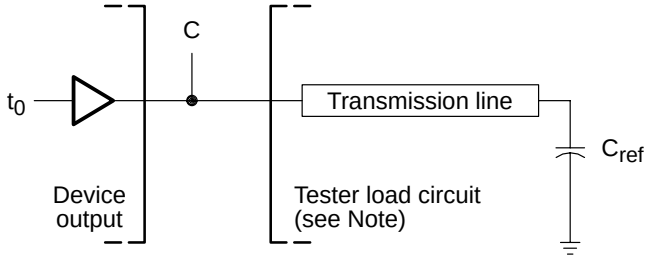
3 Understanding the Tester

3.1 Tester Load Adjustment

As mentioned in previous sections, the tester loading must be accounted for when performing timing analysis on a real system board. The tester loading must be subtracted out of the board routes in order to accurately reflect the change in loading. Figure 3 gives a simplistic view of how the board route varies from the tester loading.



Typical point-to-point board route



Typical tester route

NOTE: Tester load circuit differs on the various devices. Refer to the device data sheet for the exact tester load circuit.

Figure 3. Board Route/Loading vs Tester Route/Loading

In Figure 3, the top figure shows a typical point-to-point board route. The output from the DSP (point A) drives a load consisting of the transmission line and the load at point B. The line delay, Y, is a function of the board routing and characteristics. The bottom figure shows a typical tester circuit. Refer to the device data sheet for the exact tester circuit. Typical testers will subtract off line delays and provide data sheet output timings at the pins of the device (point C) given the capacitive loading of the tester. Data sheet timings are obtained when a signal crosses the reference voltage V_{ref} at point C. You cannot take the data sheet timing measured at point C and assume it applies to the timing at point A or point B on your board. This is because, in most cases, the board has a different capacitive loading than the tester circuit. A system board with loadings smaller than the tester loading will cause faster timings to point B, compared to the data sheet timing measured at point C. A system board with larger loadings will cause slower timings to point B, compared to the data sheet timing measured at point C.

By providing the proper board route characteristics (Y) and IBIS models for the DSP and the SDRAM, IBIS simulations can be used to measure the actual timings at point B and C, respectively. IBIS simulators have the ability to give absolute timings or reference timings. Absolute timings are measured from when the buffer is turned on at t_0. Reference timings are measured from when the output pin under test reaches the reference voltage. For example, absolute timing at point B is measured from t_0, while reference timing at point B is measured from when the output at A reaches the reference voltage. For AC timing analysis, use absolute timings in IBIS simulations to establish a common reference point for both the system board circuit and the tester circuit. Absolute timings are represented by a subscript 0. Performing IBIS simulations with the proper IBIS models and board route characteristics, you can obtain B_0, the absolute delay measured from t_0 to B. Similarly, you can perform IBIS simulations to obtain C_0, the absolute delay from t_0 to C. The following equation gives the difference between the actual timing seen at the pin of the SDRAM (B_0) and the data sheet timing (C_0):

$$\textit{Difference between timing at SDRAM and data sheet} = B_0 - C_0 \quad (1)$$

As shown in Figure 3, the board delay Y is represented by this equation:

$$Y = B_0 - A_0 \quad (2)$$

This shows that, if board loading is equivalent to the tester loading ($C_0 = A_0$), the difference between the timing at SDRAM and data sheet = $B_0 - C_0 = B_0 - A_0$. In other words, the delay caused by the tester is equivalent to the delay caused by the board loading. If board loading is smaller than the tester load ($C_0 > A_0$), then B_0 is smaller, making the difference between the timing at SDRAM and data sheet smaller. The opposite is true as well. Larger board loading ($C_0 < A_0$) will cause B_0 to be larger; thus, the difference between the timing at SDRAM and the data sheet will also be larger. Figure 4 and Figure 5 show how the loading affects a given line with respect to the rising clock signal. Parameters C_0 and Y are constant in Figure 4 and Figure 5. Parameter A_0 is different in Figure 4 and Figure 5, assuming different loading at point B.

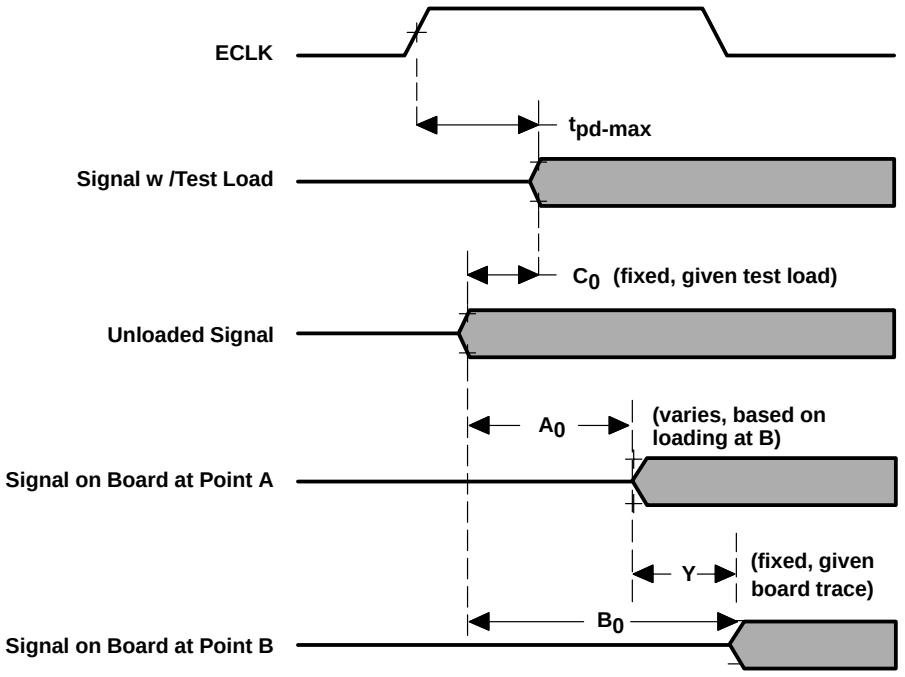


Figure 4. Signal Delay With Heavier Load Than Tester Load ($C_0 < A_0$)

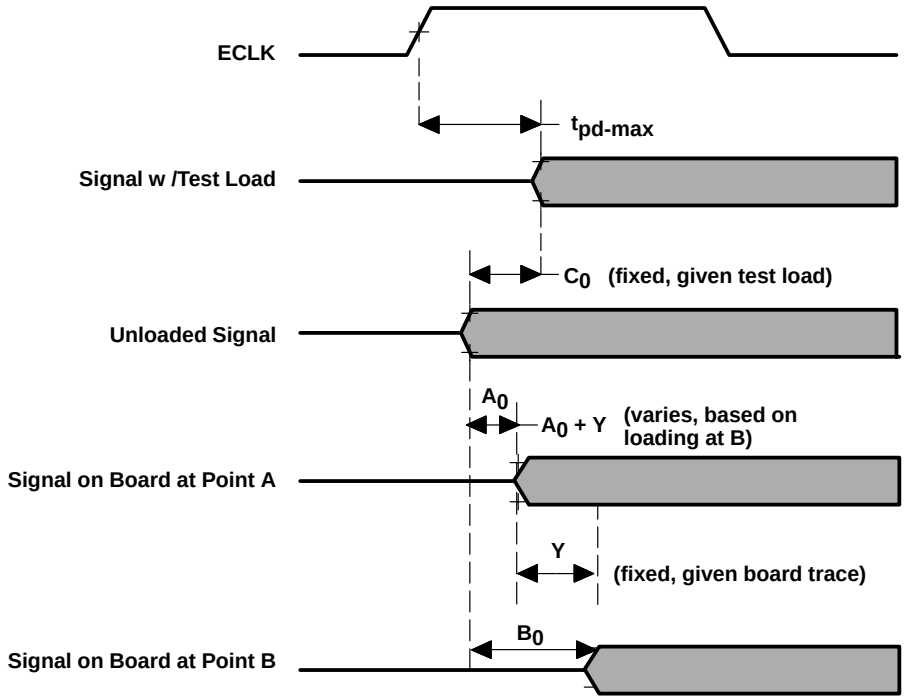


Figure 5. Signal Delay With Lighter Load Than Tester Load ($C_0 > A_0$)

Note that B_0 and C_0 are calculated from absolute timing in IBIS simulation. The difference ($B_0 - C_0$) is a constant for a given board trace and input/output buffer. ($B_0 - C_0$) is referred to here as the tester load adjustment.

$$\textit{Tester load adjustment} = B_0 - C_0 \quad (3)$$

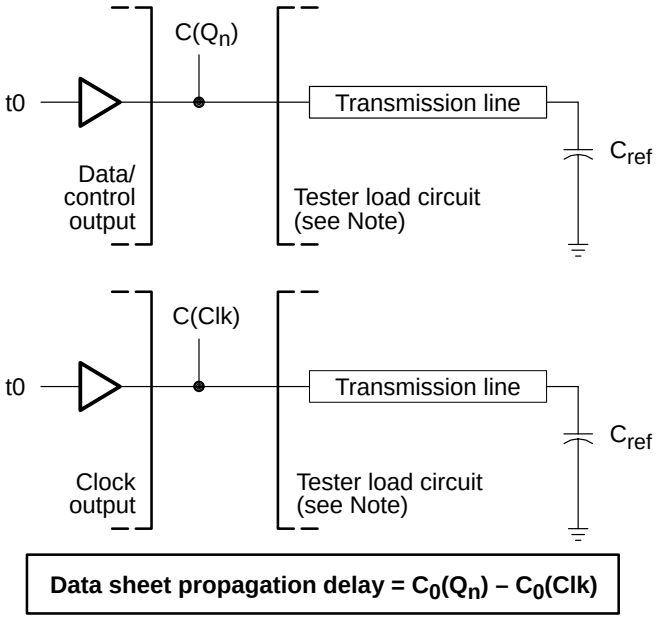
This shows that for a given pin, if you know the time t_1 when the signal transitions at point C, you can easily find out time t_2 when the signal transitions at point B by simply adding the tester load adjustment, which is a constant for a given pin and board trace:

$$t_2 = t_1 + (B_0 - C_0) \quad (4)$$

The next section explains how to make use of the tester load adjustment in AC timing analysis.

3.2 Using Data Sheet Timing on a Real System Board

The data sheet does not provide the internal reference t_0 and the absolute time, C_0, at which a signal switches (see Figure 3). Instead, the data sheet provides data/control signal timing, with respect to the clock signal at the pin of the device, given a tester load. Figure 6 shows how the data sheet timing is obtained, using propagation delay as an example.



NOTE: Tester load circuit differs on the various devices. Refer to the device data sheet for the exact tester load circuit.

Figure 6. Data Sheet Timing

For the remainder of this application report, the term "t_{pd}" is used to represent the propagation delay from the clock signal to the data/control signal. t_{pd} is measured from when the data/control switches relative to when the clock transitions. To understand AC timing in the DSP-to-SDRAM write example, you must translate the data sheet timing (t_{pd} at the DSP pin with tester loading) to t_{pd} at the input pin of the SDRAM, to decide whether the SDRAM input timing requirements can be met in a real system board. Section 3.1 provides a tester load adjustment ($B_0 – C_0$) that shows the difference in timing between when a signal switches at point B vs. C (Figure 3). You need to use this tester load adjustment to translate data sheet timing to t_{pd} at the SDRAM pin.

As shown in Figure 6, the t_{pd} in the data sheet is calculated from:

$$t_{pd}(datasheet) = C_0(Q_n) – C_0(Clk) \quad (5)$$

On the real system board, the t_{pd} at the SDRAM input pin is:

$$t_{pd}(at\ SDRAM) = B_0(Q_n) – B_0(Clk) \quad (6)$$

In the above equations, the only unknown is t_{pd}(at SDRAM). Parameter t_{pd}(datasheet) is provided in the data sheet, and parameters $C_0(Q_n)$, C_0(Clk), $B_0(Q_n)$, and B_0(Clk) are obtained from IBIS simulations with the proper board trace and IBIS models. You know that given C_0—the time when a signal switches at C—you can calculate the time when a signal switches at the SDRAM pin by adding the tester load adjustment, as seen in equation 4 in section 3.1. Therefore, you obtain:

$$B_0(Q_n) = C_0(Q_n) + [B_0(Q_n) – C_0(Q_n)] \quad ; Add\ tester\ load\ adjustment \quad (7)$$

$$B_0(Clk) = C_0(Clk) + [B_0(Clk) – C_0(Clk)] \quad ; Add\ tester\ load\ adjustment \quad (8)$$

This means t_{pd}(at SDRAM) can be calculated as follows:

$t_{pd}(at\ SDRAM)$
$= B_0(Q_n) - B_0(Clk)$; *Equation 6*
$= \{C_0(Q_n) + [B_0(Q_n) - C_0(Q_n)]\} - \{C_0(Clk) + [B_0(Clk) - C_0(Clk)]\}$; *Substitute equations 7 and 8.*
$= C_0(Q_n) - C_0(Clk) + [B_0(Q_n) - C_0(Q_n)] - [B_0(Clk) - C_0(Clk)]$; *Rearrange.*
$= t_{pd}(datasheet) + [B_0(Q_n) - C_0(Q_n)] - [B_0(Clk) - C_0(Clk)]$; *Substitute equation 5.*

Figure 7 presents this calculation graphically to show how the tester load adjustment is added to the data sheet timing to derive timing at the SDRAM pin.

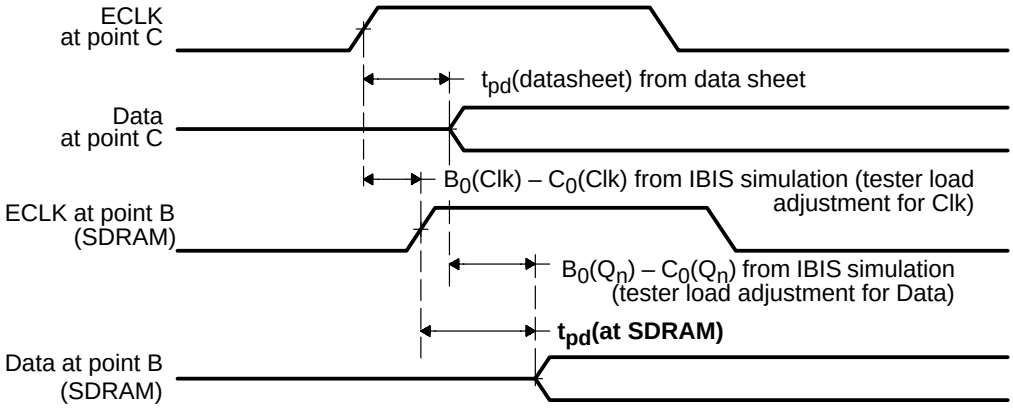


Figure 7. Adding Tester Load Adjustment to Obtain Timing at SDRAM

3.3 Variations Between Device Pins

For any given pin, Q_n, the value of C_0 will be constant. $C_0(Q_n)$ may vary between the different pins due to variations within the component packages. This variation between pins is generally small, but must be taken into account when calculating the timings. For simplicity, the average value for C_0 for all Q_n can be used, and a factor of margin can be added to compensate for this simplification. If more exact timings are desired, $C_0(Q_n)$ should be calculated for each signal trace.

For each pin, C_0 is calculated by placing the specific pin on the tester load given in the data sheet. You can obtain the value C_0 for a given pin by performing IBIS simulation using this simple setup. For each pin, the IBIS file provides its input/output characteristic at three conditions—weak, strong, and typical. You should perform at least two independent IBIS simulation runs—one using weak conditions, and one using strong conditions. The independent weak and strong runs will give you the worst-case scenarios. The delay from t_0 to point C_0 (Figure 3) is measured with respect to the reference voltage given by the data sheets. The reference voltage is discussed in the next section.

4 The Reference Voltage

A point that needs discussion is that of the reference voltage, V_{ref}. Control and data signals are latched at the rising edge of the clock signal. The question of where exactly between V_{IL} and V_{IH} does the SDRAM or the DSP latch the data must be examined. There is no exact answer. Process variations cause inconsistencies between similar devices. In order to keep device characteristics consistent, a reference voltage is given by the data sheet to show how signals are measured on the tester. This reference voltage is used as a starting point for calculating device characteristics, such as setup and hold. For example, the data sheet may provide t_{pd}(Clk-Data) = 3 ns. This means that the delay between the clock crossing V_{ref} at point C (Figure 3) and the data crossing V_{ref} at point C is 3 ns. Some IBIS packages will only calculate when devices achieve valid logic levels (V_{IL} and V_{IH}) from the time in which the buffer is enabled (t_0). Using these times, in conjunction with the V_{ref} stated in the data sheet, the time it takes to get to V_{ref} can be interpolated. Figure 8 shows how this is done.

Figure 8 shows an example IBIS simulation of a particular device pin. The first IBIS simulation run produces the left waveform (buffer in strong condition), and the second simulation run produces the right waveform (buffer in weak condition). V_{ref}, V_{IL}, and V_{IH} are parameters from the data sheet. Timing parameters t_{ref}, t_{il}, and t_{ih} are obtained from IBIS simulations at point V_{ref}, V_{IL}, and V_{IH}, respectively. As shown in Figure 8, the interpolation formula applies because the given waveforms are clean and the slope from (t_{il}, V_{IL}) to (t_{ref}, V_{ref}) can be assumed to be the same as the slope from (t_{ref}, V_{ref}) to (t_{ih}, V_{IH}). This assumption applies to the individual strong and weak waveforms.

As stated in the data sheets, AC timings are calculated based off of V_{ref}. Therefore, V_{ref} should be used when estimating the timings generated by the DSP or SDRAM on a given board. The use of strong and weak buffers should not be mixed when interpolating V_{ref}.

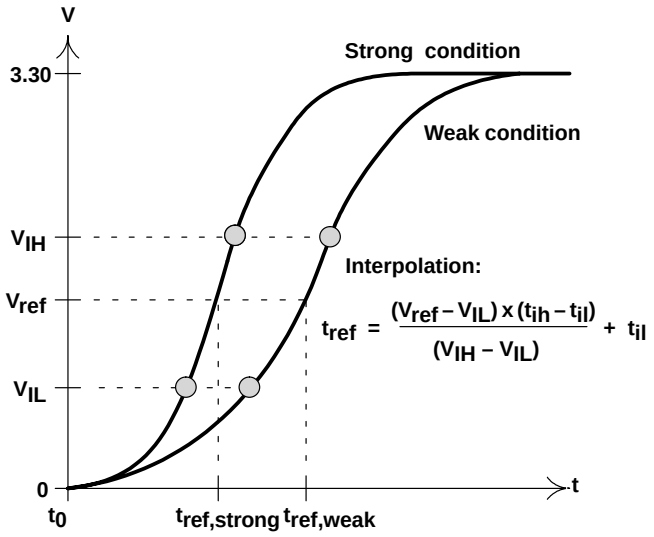


Figure 8. Interpolation Using V_{ref}

4.1 Understanding V_{ref} Measured on Tester vs. Real Board

The data sheet defines a reference voltage, V_{ref} , at point C in Figure 3, from which all AC timings are calculated. The corresponding timing reference, t_{ref} , can be calculated using IBIS simulations. This is possible because, on the tester, the signals have point-to-point connections (device under test connected to the tester), resulting in clean waveforms similar to the ones shown in Figure 8, where the transition between V_{IL} and V_{IH} is smooth and monotonic. Therefore, a single t_{ref} that corresponds to V_{ref} can easily be located. A real system board, however, may not provide clean, point-to-point connections. As a result, it may be very difficult to define a t_{ref} that corresponds to V_{ref} at point B (Figure 3). Figure 9 shows this problem where the signal between V_{IL} and V_{IH} is not monotonic.

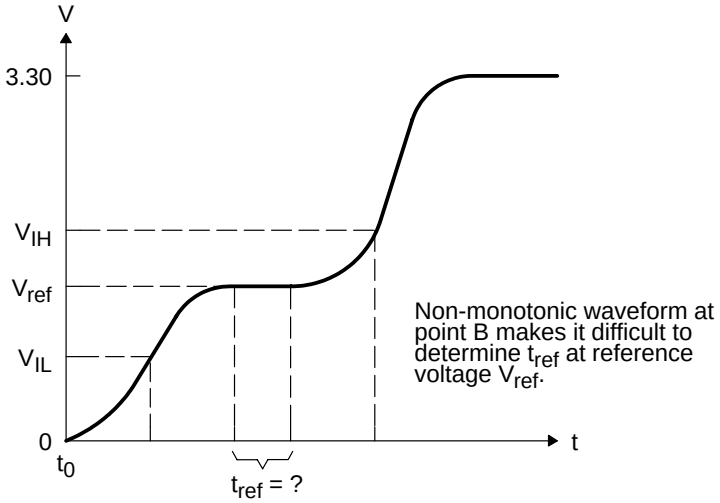


Figure 9. Difficulty in Defining Single (t_{ref}, V_{ref}) on Boards Without Clean Waveforms

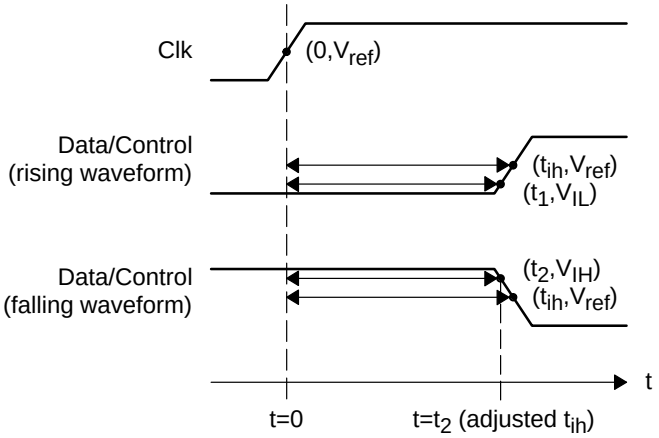
For proper operation, you must perform IBIS simulations to ensure that the clock signal at point B (input to SDRAM) is monotonic between V_{IL} and V_{IH} in a real system board, similar to the signal in Figure 8. Because clock signals are required to be monotonic, the reference voltage, V_{ref}, can easily be identified, as shown in Figure 8. Data and control signals, however, are not required to be monotonic. The only requirement for data/control signals is that they must meet the input setup and hold time requirement of the end device. Figure 9 may therefore apply to the data/control signals. You need to use voltages other than V_{ref} as a reference voltage at point B in a real system board. This is discussed in the next section.

4.2 Translating Data Sheet Reference Voltage From V_{ref} to V_{IL}/V_{IH}

As shown in section 4.1, data/control signals at point B (input of the end device) may not be clean. You must adjust the data sheet input requirement from using V_{ref} to using V_{IL}/V_{IH} as a reference voltage. For a rising data/control signal, V_{IL} should be used as the new reference voltage because the rising signal is no longer considered a logic-low the moment it goes above V_{IL}. Similarly, for a falling data/control signal, V_{IH} should be used as the new reference voltage because the falling signal is no longer considered a logic-high the moment it goes below V_{IH}.

Figure 10 gives an example of how to translate the data input hold requirement for a different reference voltage. Input hold requirement (t_{ih}) is measured from the clock switching at V_{ref} to the data switching at V_{ref}, measured at the input pin of the device. This is shown at point (t_{ih}, V_{ref}) in Figure 10. For a rising data signal, you need to translate t_{ih} to the new reference voltage t_1, shown as point (t_1, V_{IL}). For a falling data signal, you need to translate t_{ih} to the new reference voltage t_2, shown as point (t_2, V_{IH}). The tester provides input signals to the device under test at a specified input slew rate, measured in the unit volt per nanosecond (V/ns) and shown as slope m in Figure 10. The algebraic equations in this figure show the calculation of t_1 and t_2 based on the tester input slew rate m, V_{ref}, V_{IL}, V_{IH}, and the data sheet t_{ih}.

Because data signals can be either falling and rising, you need to define the new input hold requirement as the worst of t_1 or t_2. Larger input hold requirements are more stringent, therefore you should pick the larger of t_1 or t_2 as your new input hold requirement referenced at the new reference voltage V_{IL} or V_{IH}, respectively. In the typical case where V_{ref} = 1.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V, t_2 becomes the new input hold requirement because it is larger (and more stringent) than t_1. As mentioned in section 4.1, clock signals are monotonic; therefore, they can use the V_{ref} reference. Only data/control signals need to be translated to use the V_{IL}/V_{IH} voltage reference.



Calculating the adjusted t_{ih} (which equals t_1 or t_2)

t_{ih} = input hold requirement from data sheet

$t_1 = t_{ih} – (1/m) * (V_{ref} – V_{IL})$ where m is a positive value

$t_2 = t_{ih} – (1/m) * (V_{ref} – V_{IH})$ where m is a negative value

New input hold requirement is the greater of t_1 or t_2.

NOTE: All slopes (input slew rate or transition time) are m V/ns, as specified in the data sheet.
All signals are measured at the input of the device under test.
All points in this figure are labeled as (time, voltage).

Figure 10. Translating Input Requirement to V_{IL}/V_{IH} Reference Volage

5 Noise Margins

IBIS simulations do not model noise levels within a system. Certain levels of noise, such as cross-talk, can be accounted for; but ground bounce, electromagnetic interference (EMI), and general power supply noise are not modeled. These uncertain noise sources must be taken into account when analyzing IBIS models. Figure 11 shows the noise margin for a typical signal during a falling edge with moderate amounts of ringing. For proper operation, the board designer must ensure that a signal is well within a valid high or low level.

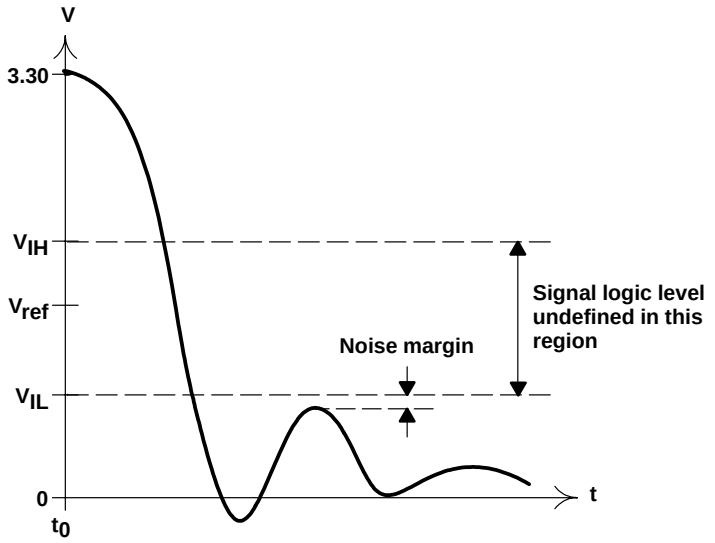


Figure 11. Noise Margin for a Typical Signal

Sporadic noise can easily achieve 100 mV-150 mV levels, depending on the environment in which the board is running. A shift of 150 mV on the ground plane can cause a signal to transition from a valid logic level to an invalid state, possibly causing an unknown behavior. A typical method of accounting for noise margin is to adjust the V_{IL} and V_{IH} levels within the IBIS simulation. Standard voltage levels for V_{IL} and V_{IH} are 0.8 V and 2.0 V, respectively. Using a V_{IL} voltage of 0.6 V and a V_{IH} voltage of 2.5 V are common numbers when adjusting for noise margins. Boards should be designed to ensure logic-low signals are well below the adjusted V_{IL} = 0.6 V, and logic-high signals are well above the adjusted V_{IH} = 2.5 V. This is a more stringent board-design requirement that provides an extra noise margin of 0.2 V for the logic-low signals, and a noise margin of 0.5 V for the logic-high signals.

To do so, edit the device IBIS models by changing V_{inl} from 0.8 V to 0.6 V, and V_{inh} from 2.0 V to 2.5 V. Then run IBIS simulations to obtain absolute timings at point B (Figure 3) measured at V_{IL} = 0.6 V and V_{IH} = 2.5 V.

6 IBIS Calculation Methods

Both the DSP and SDRAM have minimum timing requirements that must be adhered to. Switching characteristics are guaranteed by the part as long as the minimum operating conditions and requirements are met. The switching characteristics of one component must meet the requirements of the other component in order for a system to work properly.

It is important to emphasize here that switching characteristics, as well as timing requirements, are measured at the pins of the DSP and/or the SDRAM.

The clock line is an output of the DSP. There are no specific setup and hold-time requirements associated with this line. It is important that transition specifications given by the DSP meet the requirements needed by the SDRAM. Clock trace routing plays an important role in the system design process.

Control signals, including ADDRESS, RAS, CAS, CS, WE, etc., are outputs of the DSP. The switching characteristics of these signals must align with the SDRAM input requirements at the pins of the SDRAM.

Data signals are both outputs and inputs to the DSP. The switching characteristics of the DSP data output buffers must align with the SDRAM input requirements. The same signals must have the SDRAM data output buffers meeting the DSP data input requirements. For most DSPs, the output data signals have the same switching characteristics as the control signals.

Four critical parameters must be met when designing for a high-speed interface to SDRAM. These four parameters are:

- t_{isu} of the SDRAM (input setup time)
- t_{ih} of the SDRAM (input hold time)
- t_{isu} of the DSP (input setup time)
- t_{ih} of the DSP (input hold time)

Calculations for these parameters are discussed in sections 6.1 through 6.4. For the multiple data and control pins, the values for $C_0(Q_n)$ can be averaged to a constant to make calculations easier, or preferably, you can use the worst case of $C_0(Q_n)$. This should be taken into account when figuring acceptable margin values. The values for C_0 and B_0 must be calculated using an IBIS simulation package. B_0 will vary based on board characteristics and the system environment. Therefore, accurate accounting of noise and other system margins are necessary when using the IBIS simulation package to calculate these numbers.

6.1 Input Setup of the SDRAM

An input setup time is required by the control signals during reads and writes to the SDRAM, as well as the data signals when the DSP is writing to the SDRAM. To verify that setup times to the SDRAM are met, the margin defined in the following equation must be greater than zero. Refer to Figure 3 for points B and C.

$$margin = ECLK_{Per} - \overbrace{\left(\left[B_{0,weak}(Q_n) - C_{0,weak}(Q_n)\right]_{\max}\right.}^{\text{Tester Load Adjustment for Control/Data Lines}} + t_{Pd-Max} - \overbrace{\left.\left[B_{0,strong}(Clk) - C_{0,strong}(Clk)\right]\right)}^{\text{Tester Load Adjustment for Clock Signal}} - t_{isu}(SDRAM) \quad \textbf{(9)}$$

The above variables and constants are described in Table 1.

Table 1. SDRAM Input Setup Parameters

SDRAM Input Setup Constants		
$ECLK_{Per}$	:	EMIF clock period
$t_{isu(SDRAM)}$	:	Input setup requirement by the SDRAM. This parameter is derived from the SDRAM data sheet, and then adjusted from V_{ref} voltage reference to V_{IL}/V_{IH} voltage reference (see section 4.2).
t_{pd-max}	:	Maximum propagation delay given by the DSP. This parameter is obtained from the DSP data sheet.
$C_{0,weak}(Q_n)$	:	DSP data/control buffer propagation delay of a weak process buffer, measured from t_0 to when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
$C_{0,strong}(Clk)$	:	DSP clock buffer propagation delay of a strong process buffer, measured from t_0 to the when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
SDRAM Input Setup Variables		
$B_{0,weak}(Q_n)$	:	DSP data/control buffer propagation delay of a weak process buffer, measured from t_0 to **when the signal reaches a valid logic level** on the board at SDRAM pin (point B). Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.
$B_{0,strong}(Clk)$	:	DSP clock buffer propagation delay of a strong process buffer, measured from t_0 to **when the signal crosses the reference voltage V_{ref}** on the board at SDRAM pin (point B). Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.

The input setup of the SDRAM is a minimum requirement; therefore, the sum of all the parameters on the right side of the equation must be greater than zero. The only variables that can be adjusted are the clock and signal buffer propagation delays $B_0(Q_n)$ and $B_0(Clk)$. These are adjusted by varying the trace characteristics, such as length, impedance, etc. In other words, they can be adjusted by varying line delay Y in Figure 3.

When calculating the setup time to the SDRAM, the worst possible setup time is when the clock line is fast and the control/data lines are slow. In order to simulate this, a strong clock line is used in conjunction with a weak control/data line. This assumes that the clock signals are monotonic and the reflections are minimal.

Figure 12 shows the SDRAM input setup timing graphically.

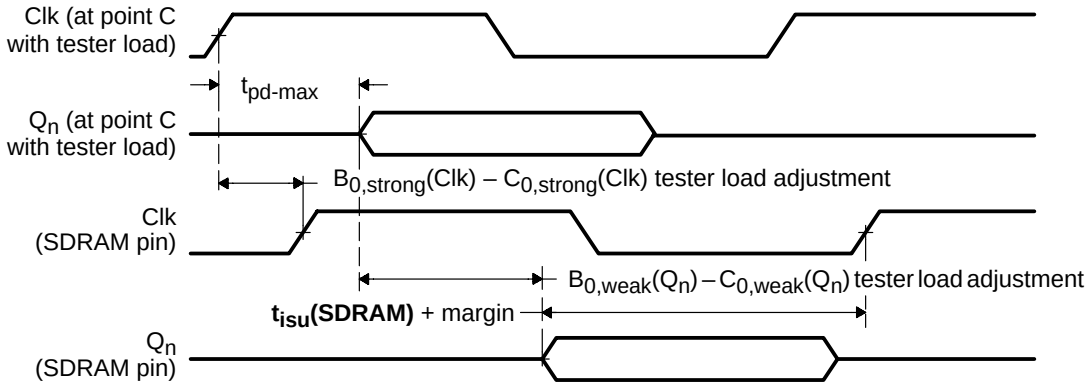


Figure 12. Input Setup of the SDRAM

Because of the multiple control and data signals, each trace must be calculated (using the method discussed above) to find the maximum difference between the board and test load. This maximum difference will result in the worst-case setup time to the SDRAM. Although all the data lines may use similar buffers within a given device, the package characteristics cause variations in the output signal at the pins. When calculating the difference between the board propagation delay and the test load propagation delay, it is important to use the same pin. Using separate pins to make this calculation will result in incorrect simulations.

6.2 Input Hold of the SDRAM

An input hold time is also required by the control signals during reads and writes to the SDRAM, as well as the data signals when the DSP is writing to the SDRAM. To verify that hold times to the SDRAM are met, the margin defined in the following equation must be greater than zero.

$$margin = \overbrace{\left[B_{0,strong}(Q_n) - C_{0,strong}(Q_n)\right]_{\min}}^{\text{Tester Load Adjustment for Control/Data Lines}} + t_{Pd-Min} - \overbrace{\left[B_{0,weak}(Clk) - C_{0,weak}(Clk)\right]}^{\text{Tester Load Adjustment for Clock Signal}} - t_{ih}(SDRAM) \quad \textbf{(10)}$$

The above variables and constants are described in Table 2.

Table 2. SDRAM Input Hold Parameters

SDRAM Input Hold Constants		
$t_{ih(SDRAM)}$	:	Input hold requirement by the SDRAM. This parameter is derived from the SDRAM data sheet, and then adjusted from V_{ref} voltage reference to V_{IL}/V_{IH} voltage reference (see section 4.2).
$t_{pd\text{-}min}$	:	Minimum propagation delay given by the DSP. This parameter is obtained from the DSP data sheet.
$C_{0,strong}(Q_n)$	:	DSP data/control buffer propagation delay of a strong process buffer, measured from to when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
$C_{0,weak}(Clk)$	:	DSP clock buffer propagation delay of a weak process buffer, measured from t_0 to when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
SDRAM Input Hold Variables		
$B_{0,strong}(Q_n)$	:	DSP data/control buffer propagation delay of a strong process buffer, measured from t_0 to **when the signal goes to an invalid logic level** on the board at the SDRAM input (point B). Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.
$B_{0,weak}(Clk)$	:	DSP clock buffer propagation delay of a weak process buffer, measured from t_0 to **when the signal crosses the reference voltage** on the board at the SDRAM input (point B). Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.

The input hold of the SDRAM is a minimum requirement; therefore the sum of all the parameters on the right side of the equation must be greater than zero. The only variables that can be adjusted are the clock and signal buffer propagation delays. These are adjusted by varying the trace characteristics (the delay Y) in Figure 3.

The worst-case input hold to the SDRAM is achieved when the clock signal is slow and the control/data signals are fast. Assuming monotonic signals and minimal reflections on the traces, a weak clock buffer and a strong control/data buffer should be used to simulate this worst-case situation.

Figure 13 shows the SDRAM input setup timing graphically.

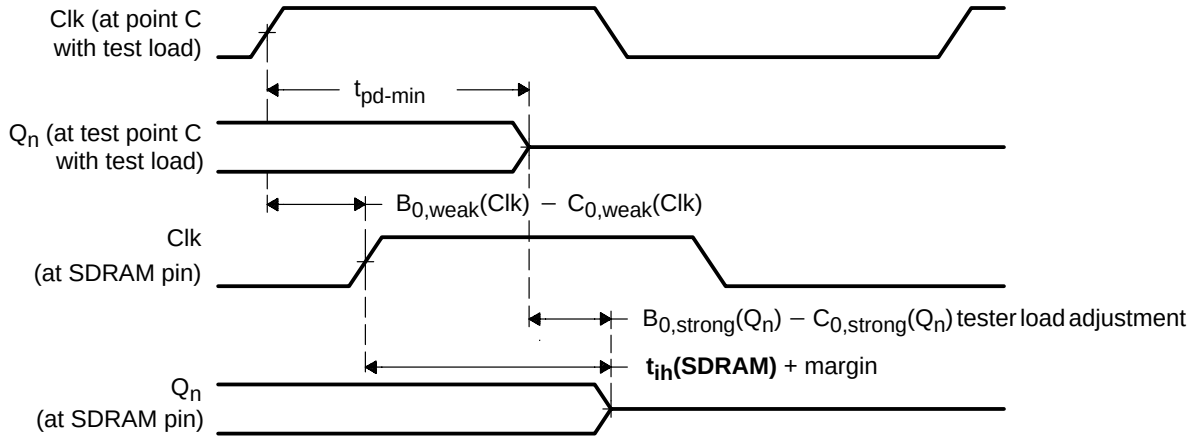


Figure 13. Input Hold of the SDRAM

Because of the multiple control and data signals, each trace must be calculated (using the method discussed above) to find the minimum difference between the board and test load. This minimum difference will result in the worst-case hold time to the SDRAM.

6.3 Input Setup of the DSP

DSP reads are different than writes, in the sense that reads have to take into account the propagation delay of the SDRAM as well as the board route delays to and from the DSP. The DSP input setup is required only when the SDRAM outputs data to the DSP. To verify that setup times to the DSP are met, the margin defined in the following equation must be greater than zero.

$$margin = ECLK_{Per} - \overbrace{\left(\left[B_{0,weak}(Q_n) - C_{0,weak}(Q_n)\right]_{\max}\right.}^{\text{Tester Load Adjustment for Data Lines}} + t_{Acc} + \overbrace{\left.\left[B_{0,weak}(Clk) - C_{0,weak}(Clk)\right]\right)}^{\text{Tester Load Adjustment for Clock Signal}} - t_{isu}(DSP) \quad \textbf{(11)}$$

The above variables and constants are described in Table 3.

Table 3. DSP Input Setup Parameters

DSP Input Setup Constants		
$ECLK_{Per}$	:	EMIF clock period
$t_{isu}(DSP)$	:	Input setup requirement by the DSP. This parameter is derived from the DSP data sheet, and then adjusted from V_{ref} voltage reference to V_{IL}/V_{IH} voltage reference (see section 4.2).
t_{Acc}	:	Maximum access time given by the SDRAM. This parameter is obtained from the SDRAM data sheet.
$C_{0,weak}(Q_n)$	:	SDRAM data buffer propagation delay of a weak process buffer, measured from when the SDRAM output buffer is enabled/disabled to when the signal crosses the reference voltage using only the SDRAM test load. Calculated using an IBIS simulation package, along with SDRAM IBIS model.
$C_{0,weak}(Clk)$	:	DSP clock buffer propagation delay of a weak process buffer, measured from t_0 to when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
DSP Input Setup Variables		
$B_{0,weak}(Q_n)$	:	SDRAM Data buffer propagation delay of a weak process buffer, measured from when the SDRAM output buffer is enabled to **when the signal reaches a valid logic leve**l on the board **at the pin of the DSP**. Calculated using an IBIS simulation package, along with SDRAM and DSP IBIS models.
$B_{0,weak}(Clk)$	:	DSP clock buffer propagation delay of a weak process buffer, measured from t_0 to **when the signal crosses the reference voltage** on the board at the SDRAM pin. Calculated using an IBIS simulation package, along with SDRAM and DSP IBIS models.

The input setup of the DSP is a minimum requirement; therefore the sum of all the parameters on the right side of the equation must be greater than zero. The only variables that can be adjusted are the clock and signal buffer propagation delays. These are adjusted by varying the trace characteristics, such as length, impedance, etc.

In the case of DSP reads from SDRAM, the worst-case input setup occurs when both the clock buffer and the SDRAM data buffers are slow. This means that weak buffers should be used for calculation purposes. Again, the assumption of minimal reflections and signal monotonicity remains.

Figure 14 shows the DSP input setup timing graphically.

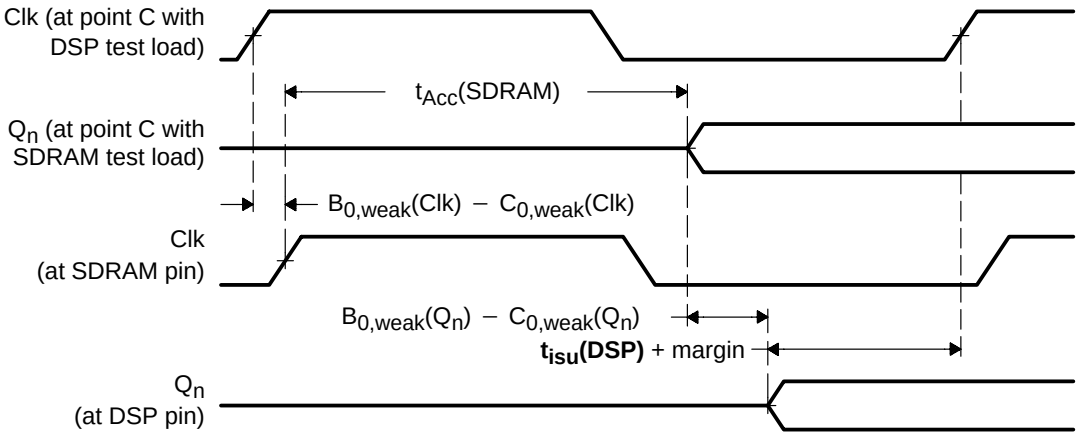


Figure 14. Input Setup of the DSP

Because of the multiple data signals, each trace must be calculated (using the method discussed above) to find the maximum difference between the board and test load. This maximum difference will result in the worst-case setup time to the DSP.

6.4 Input Hold of the DSP

To verify that hold times to the DSP are met, the margin defined in the following equation must be greater than zero.

$$margin = \overbrace{\left[B_{0,strong}(Q_n) - C_{0,strong}(Q_n)\right]_{\min}}^{\text{Tester Load Adjustment for Data Lines}} + t_{oh} + \overbrace{\left[B_{0,strong}(Clk) - C_{0,strong}(Clk)\right]}^{\text{Tester Load Adjustment for Clock Signal}} - t_{ih}(DSP) \quad \textbf{(12)}$$

The above variables and constants are described in Table 4.

Table 4. DSP Input Hold Parameters

DSP Input Hold Constants		
t_{ih}(DSP)	:	Input hold requirement by the DSP. This parameter is derived from the DSP data sheet, and then adjusted from V_{ref} voltage reference to V_{IL}/V_{IH} voltage reference (see section 4.2).
t_{oh}	:	Minimum hold time given by the SDRAM. This parameter is obtained from the SDRAM data sheet.
$C_{0,strong}(Q_n)$	:	SDRAM data buffer propagation delay of a strong process buffer, measured from when the SDRAM output buffer is enabled/disabled to when the signal crosses the reference voltage using only the SDRAM test load. Calculated using an IBIS simulation package, along with SDRAM IBIS model.
$C_{0,strong}$(Clk)	:	DSP clock buffer propagation delay of a strong process buffer, measured from t_0 to when the signal crosses the reference voltage using only the DSP test load. Calculated using an IBIS simulation package, along with DSP IBIS model.
DSP Input Hold Variables		
$B_{0,strong}(Q_n)$	:	SDRAM data buffer propagation delay of a strong process buffer, measured from when the SDRAM data buffer is disabled to the **when the signal goes to an invalid logic level** on the board at pin of the DSP. Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.
$B_{0,strong}$(Clk)	:	DSP clock buffer propagation delay of a strong process buffer, measured from t_0 to **when the signal crosses the reference voltage** on the board at the pin of the DSP. Calculated using an IBIS simulation package, along with DSP and SDRAM IBIS models.

The input hold of the DSP is a minimum requirement; therefore the sum of all the parameters on the right side of the equation must be greater than zero. The only variables that can be adjusted are the clock and signal buffer propagation delays. These are adjusted by varying the trace characteristics.

Input hold times to the DSP are worse when the clock line and the signal lines are fast. Therefore, strong buffers should be used in the calculation of DSP input hold time. Again, the assumption of minimal reflections and signal monotonicity remains.

Figure 15 shows the DSP input hold timing graphically.

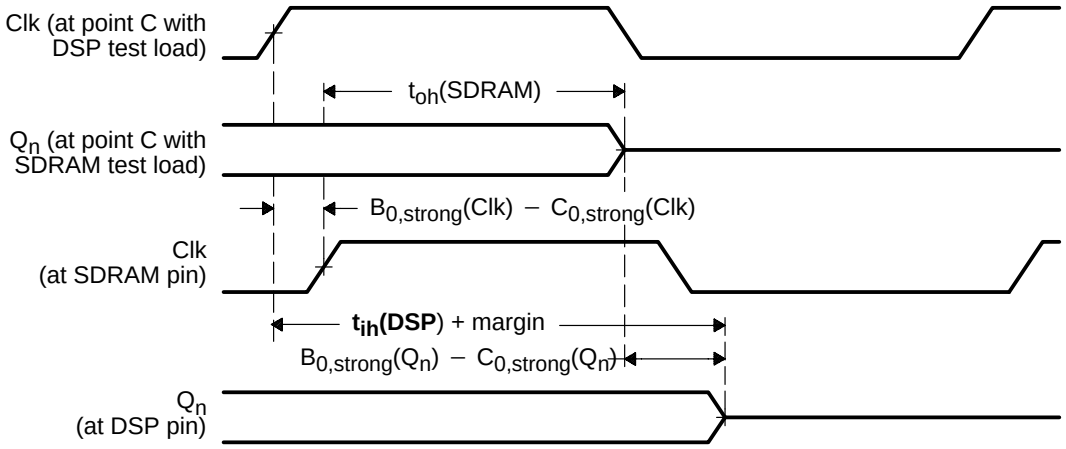


Figure 15. Input Hold of the DSP

Because of the multiple data signals, each trace must be calculated (using the method discussed above) to find the minimum difference between the board and test load. This minimum difference will result in the worst-case hold time to the DSP.

7 Summary of AC Timing Analysis Procedures

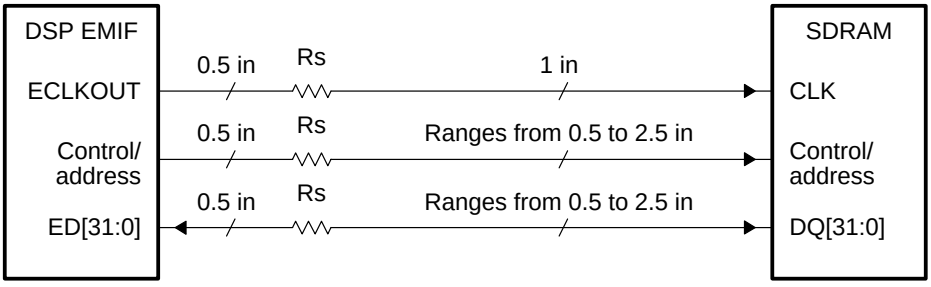
This section provides a summary of the procedures for AC timing analysis according to the method discussed in this application report. The subsections provide detailed explanation of the three steps involved: gathering information, IBIS simulations, and analysis.

7.1 Gathering Information

The first step in AC timing analysis is to gather all of the relevant information, including:

1. Data sheets for the DSP and SDRAM
2. IBIS models for the DSP and SDRAM
3. Board layout and characteristics

Figure 16 shows the board layout and trace characteristics for an example interface. The Rs in the figure are series termination resistors used to achieve signal integrity. The actual value varies depending on the board and input/output (I/O) buffer.



NOTE: Assume that all traces in this example have a characteristic impedance of Z0 = 50Ω, and require a 33-Ω series termination resistor (Rs) for signal integrity. Actual value of Rs depends on trace and input/output buffer characteristics.

Figure 16. Example DSP-SDRAM Interface Board Characteristics

7.2 IBIS Simulations

Before performing IBIS simulations on the DSP-SDRAM interface, you should first modify the IBIS models' V_{IL} and V_{IH} levels to account for noise margin, as discussed in section 5. Edit V_{inl} to 0.6 V, and V_{inh} to 2.5 V.

7.2.1 IBIS Simulations for DSP Outputs on the Board

The DSP outputs ECLKOUT and control/address to the SDRAM. In addition, the DSP outputs data ED[31:0] for a DSP write. Each of these signals can be represented in the IBIS package, as shown in Figure 17.

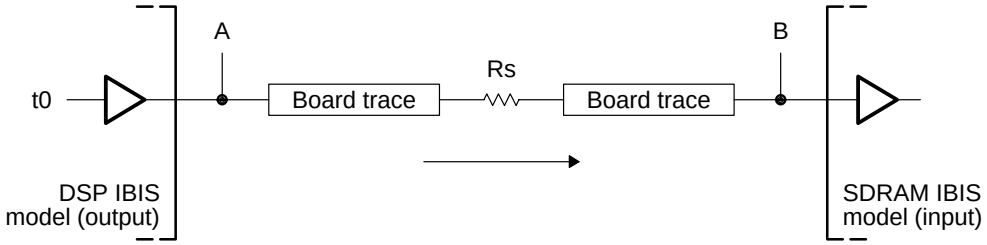


Figure 17. IBIS Representation of DSP Output on a Board

Perform IBIS simulations to obtain the absolute timing at point B (parameter B_0) at the SDRAM pin. For the clock signal, which must be monotonic at point B, measure the time B_0 at the reference voltage, V_{ref}. For data/control, which may not be monotonic at point B, measure the time B_0 at the new reference voltage V_{IL}/V_{IH}, as discussed in section 4.

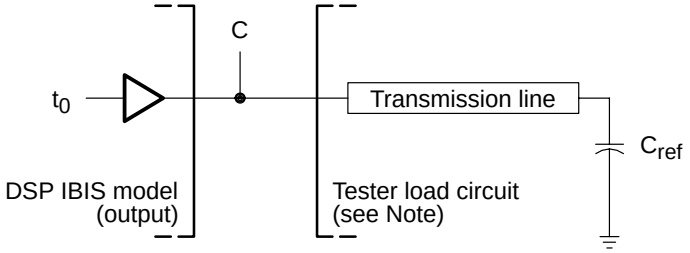
You should perform simulations twice: once with the weakest output drive strength to obtain parameter ($B_{0,weak}$), and once with the strongest output drive strength to obtain parameter ($B_{0,strong}$). See also section 3.3 for considerations on variations between the pins.

In summary, this step provides measurements for these parameters:

$B_{0,strong}$(Clk) for Table 1 and Table 4
$B_{0,weak}$(Clk) for Table 2 and Table 3
$B_{0,strong}$(control/address) for Table 2 and Table 4
$B_{0,weak}$(control/address) for Table 1 and Table 3
$B_{0,strong}(Q_n)$ for Table 2
$B_{0,weak}(Q_n)$ for Table 1

7.2.2 IBIS Simulations for DSP Outputs With Test Load

For each of the signals in section 7.2.1, the DSP data sheet provides measurement with the test load. Figure 18 shows how this is represented in the IBIS package.



NOTE: Tester load circuit differs on the various devices. Refer to the device data sheet for the exact tester load circuit.

Figure 18. IBIS Representation of DSP Output With Test Load

Perform IBIS simulations to obtain the absolute timing at point C (parameter C_0) with the DSP test load. Measure the time C_0 at the data sheet reference voltage, V_{ref}.

You should perform simulations twice: once with the weakest output drive strength to obtain parameter ($C_{0,weak}$), and once with the strongest output drive strength to obtain parameter ($C_{0,strong}$). See also section 3.3 for considerations on variations between the pins.

In summary, this step provides measurements for these parameters:

$C_{0,strong}$(Clk) for Table 1 and Table 4
$C_{0,weak}$(Clk) for Table 2 and Table 3
$C_{0,strong}$(control/address) for Table 2 and Table 4
$C_{0,weak}$(control/address) for Table 1 and Table 3
$C_{0,strong}(Q_n)$ for Table 2
$C_{0,weak}(Q_n)$ for Table 1

7.2.3 IBIS Simulations for SDRAM Outputs on the Board

The SDRAM outputs data DQ[31:0] for a DSP read. Each of these signals can be represented in the IBIS package as shown in Figure 19.

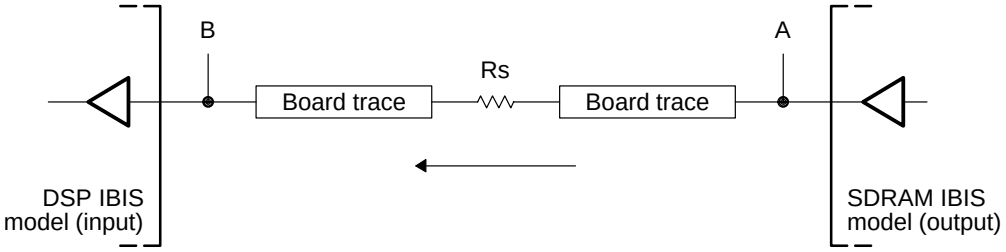


Figure 19. IBIS Representation of SDRAM Output on a Board

Perform IBIS simulations to obtain the absolute timing at point B (parameter B_0) at the DSP pin. Because the data signal may not be monotonic at the DSP pin (point B), measure the time B_0 at the new reference voltage V_{IL}/V_{IH}, as discussed in section 4.

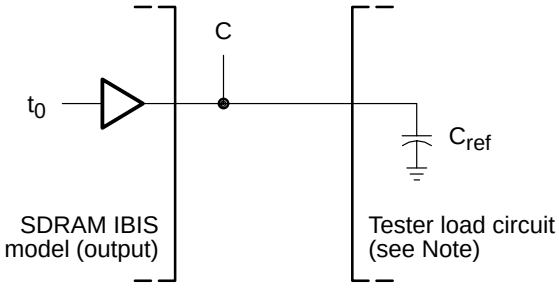
You should perform simulations twice: once with the weakest output drive strength to obtain parameter ($B_{0,weak}$), and once with the strongest output drive strength to obtain parameter ($B_{0,strong}$). See also section 3.3 for considerations on variations between the pins.

In summary, this step provides measurements for these parameters:

$B_{0,strong}(Q_n)$ for Table 4
$B_{0,weak}(Q_n)$ for Table 3

7.2.4 IBIS Simulations for SDRAM Outputs With Test Load

For the data signals in section 7.2.4, the SDRAM data sheet provides measurement with the test load. Figure 20 shows how this is represented in the IBIS package.



NOTE: Tester load circuit differs on the various devices. Refer to the device data sheet for the exact tester load circuit.

Figure 20. IBIS Representation of SDRAM Output With Test Load

Perform IBIS simulations to obtain the absolute timing at point C (parameter C_0) with the SDRAM test load. Measure the time C_0 at the data sheet reference voltage, V_{ref}.

You should perform simulations twice: once with the weakest output drive strength to obtain parameter ($C_{0,weak}$), and once with the strongest output drive strength to obtain parameter ($C_{0,strong}$). See also section 3.3 for considerations on variations between the pins.

In summary, this step provides measurements for these parameters:

$C_{0,strong}(Q_n)$ for Table 4
$C_{0,weak}(Q_n)$ for Table 3

7.3 Calculations

With the data gathered in the above sections, you are now ready to perform timing analysis, as discussed in section 6.

7.3.1 Input Setup of the SDRAM

Fill out Table 1 in section 6.1:

- Enter the desired EMIF clock period $ECLK_{Per}$.
- Enter the input setup requirement derived from the SDRAM data sheet. Do not directly input the value from the SDRAM data sheet. Instead, adjust the data sheet value by translating it from voltage reference V_{ref} to V_{IL}/V_{IH} as discussed in section 4. For example, assuming that the SDRAM datasheet specifies:
  - Tester input slew rate or transition time of 1 V/ns at the input pin
  - Reference voltage (V_{ref}) is 1.5 V.
  - V_{IL} = 0.8 V, V_{IH} = 2.0 V
  - Input setup requirement (t_{isu}) of 2 ns referenced at V_{ref}

The adjusted SDRAM input setup requirement referenced at V_{IL}/V_{IH} is calculated according to the formula in Figure 10:

– $t_1 = t_{isu} – (1/m) * (V_{ref} – V_{IL}) = 2 – (1/1) * (1.5 – 0.8) = 1.3$ ns

– $t_2 = t_{isu} – (1/m) * (V_{ref} – V_{IH}) = 2 – [1/(–1)] * (1.5 – 2.0) = 1.5$ ns

t_2 is a larger number, and therefore a more stringent new t_{isu} requirement. Enter t_2 into Table 1.

- Enter the $t_{pd\text{-}max}$ from the DSP data sheet.
- Enter the B_0 and C_0 parameters obtained in sections 7.2.1 and 7.2.2.

Then, calculate the SDRAM input setup margin using the formula in section 6.1.

7.3.2 Input Hold of the SDRAM

Fill out Table 2 in section 6.2:

- Enter the input hold requirement derived from the SDRAM data sheet. Do not directly input the value from the SDRAM data sheet. Instead, adjust the data sheet value by translating it from voltage reference V_{ref} to V_{IL}/V_{IH}, as discussed in section 4.
- Enter the $t_{pd\text{-}min}$ from the DSP data sheet.
- Enter the B_0 and C_0 parameters obtained in sections 7.2.1 and 7.2.2.

Then, calculate the SDRAM input hold margin using the formula in section 6.2.

7.3.3 Input Setup of the DSP

Fill out Table 3 in section 6.3:

- Enter the desired EMIF clock period $ECLK_{Per}$.
- Enter the input setup requirement derived from the DSP data sheet. Do not directly input the value from the DSP data sheet. Instead, adjust the data sheet value by translating it from voltage reference V_{ref} to V_{IL}/V_{IH}, as discussed in section 4.
- Enter the t_{Acc} from the SDRAM data sheet.
- Enter the B_0 and C_0 parameters obtained in sections 7.2.1 through 7.2.4.

Then, calculate the DSP input setup margin using the formula in section 6.3.

7.3.4 Input Hold of the DSP

Fill out Table 4 in section 6.4:

- Enter the input hold requirement derived from the DSP data sheet. Do not directly input the value from the DSP data sheet. Instead, adjust the data sheet value by translating it from voltage reference V_{ref} to V_{IL}/V_{IH}, as discussed in section 4.
- Enter the t_{oh} from the SDRAM data sheet.
- Enter the B_0 and C_0 parameters obtained in sections 7.2.1 through 7.2.4.

Then, calculate the DSP input hold margin using the formula in section 6.4.

8 Conclusion

Using the equations discussed in this application report, IBIS models and simulations can be used to reflect timings for point-to-point connections between an SDRAM and a DSP. Iterations on these equations may be necessary to obtain desired signal integrity and the proper timings for both setup and hold to the SDRAM and the DSP. This technique is not limited to SDRAMs or the EMIF interface. All DSP signals have characteristic setup and hold times that must be adhered to. Using the techniques discussed in this application report, IBIS analysis can used to determine proper timing relations for all relevant signals.

An understanding of the tester is needed to properly back calculate timings, to correct for variations in loading on the signals. Noise level margins can be accounted for by modifying the valid logic levels. The equations discussed in this application report give a representation of how much margin can be expected. Acceptable margin levels must be determined based on system environment and operating conditions.

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