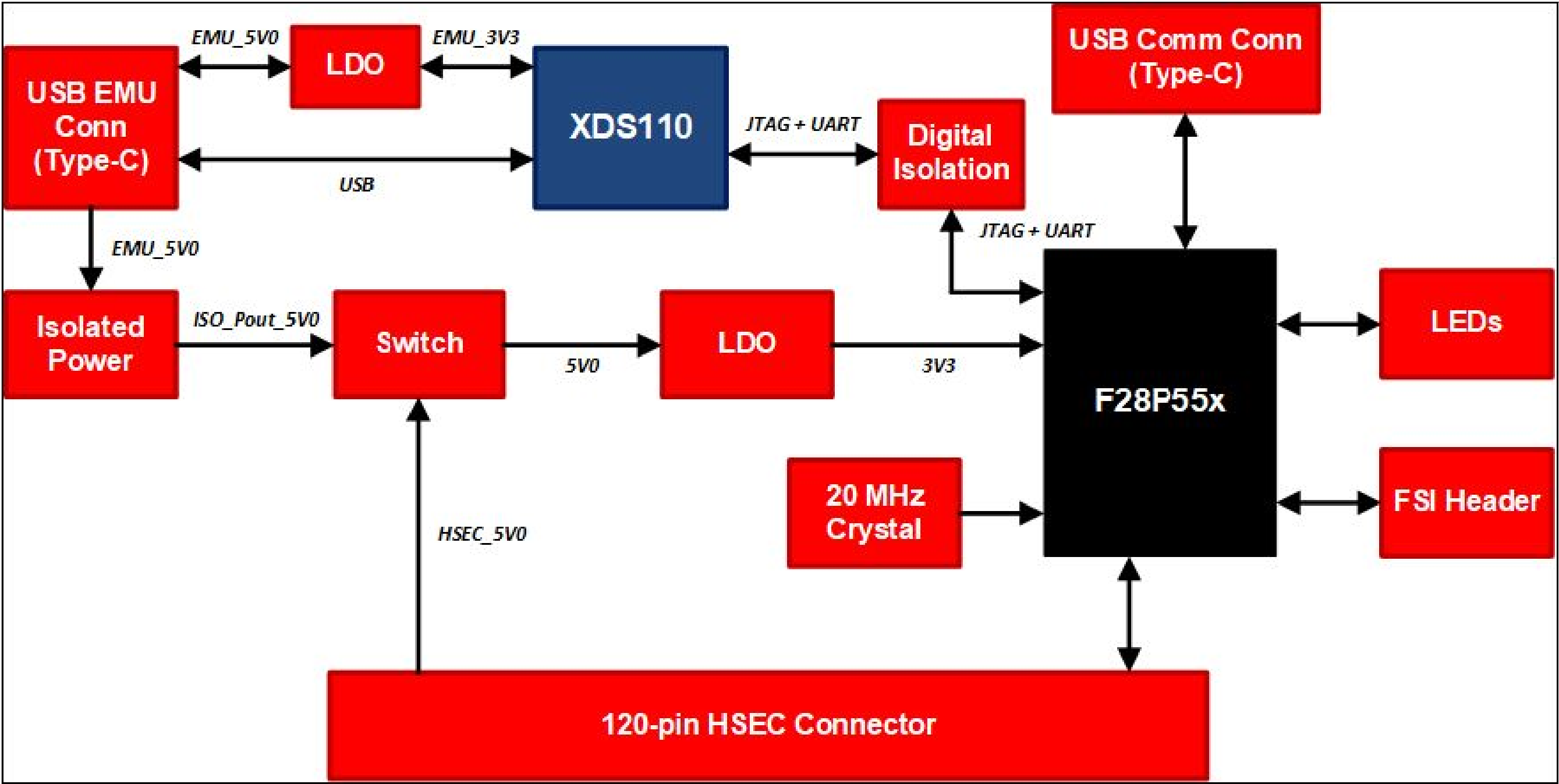


1) USB Differential Pairs - 90 Ohm
(A) XDS_D_P and XDS_D_N
(B) USB_D_P (GPIO41) and USB_D_N (GPIO23)

2) ADC PGA Differential pair Impedance Matching - 90 Ohm
(A) HSEC_PGAx_IN_P pins should match with HSEC_PGAx_IN_N, where x is between 1-3
(B) MCU_PGAx_IN_P pins should match with MCU_PGAx_IN_N, where x is between 1-3

Revision History

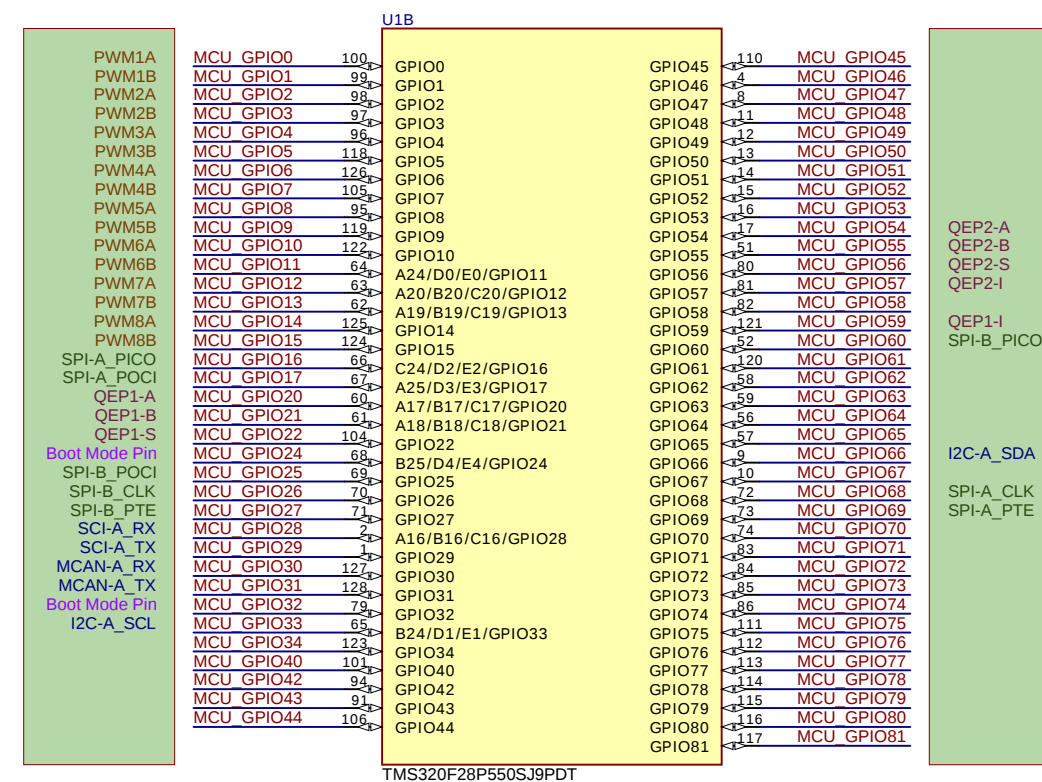
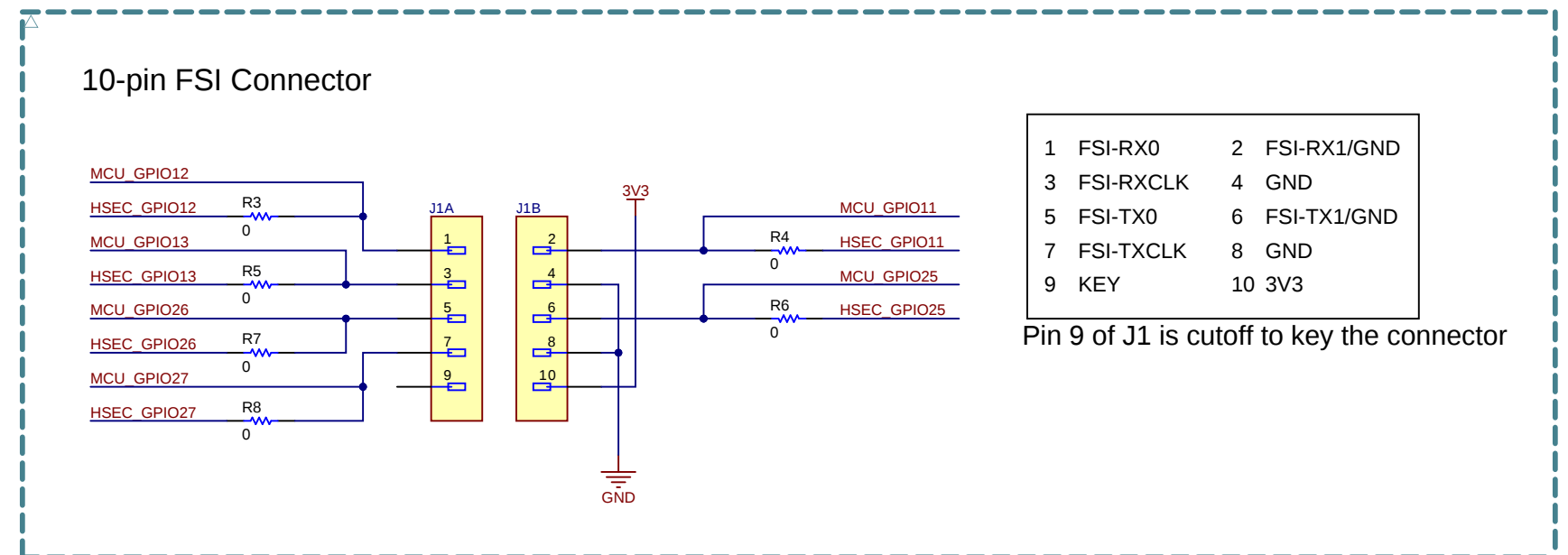
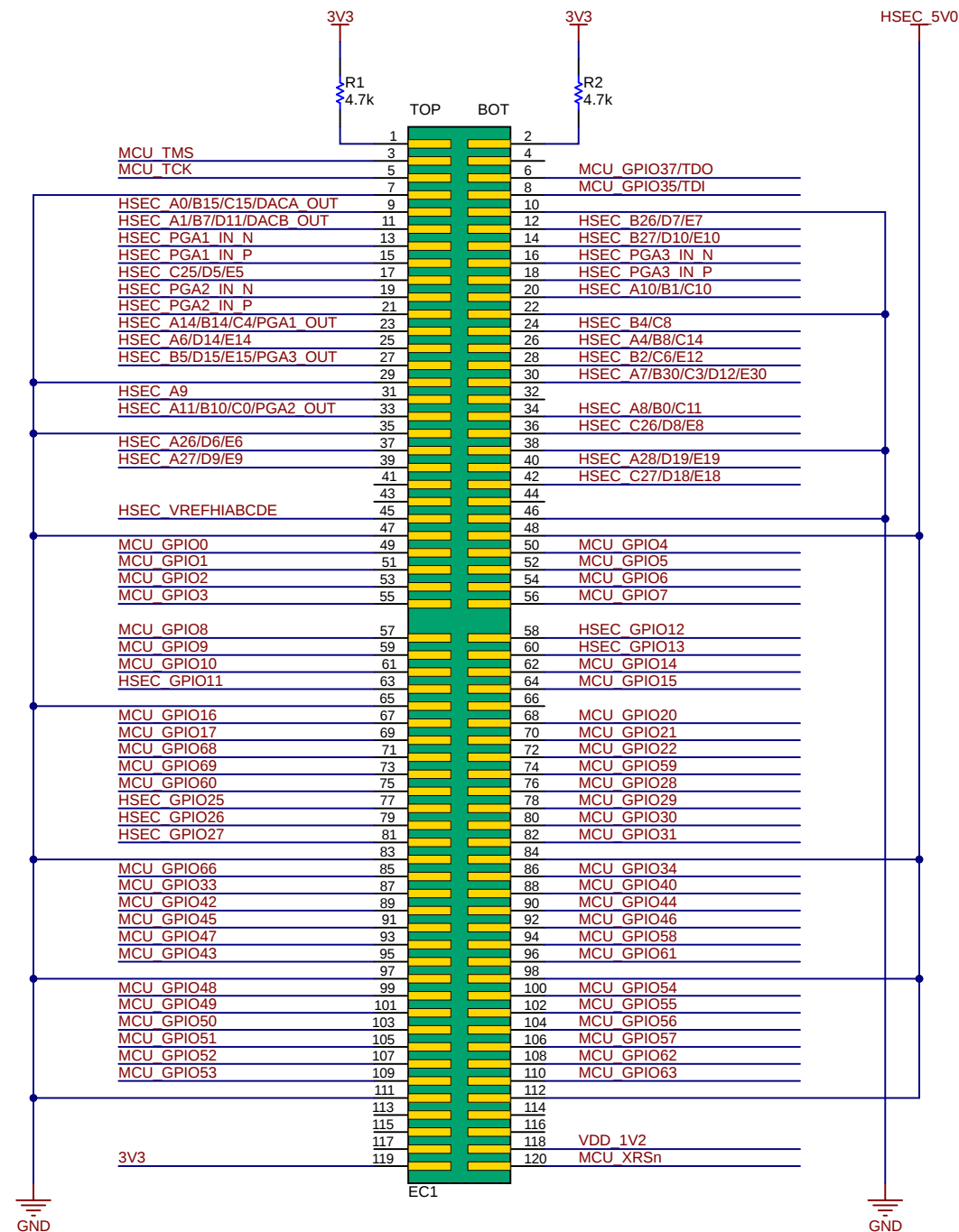
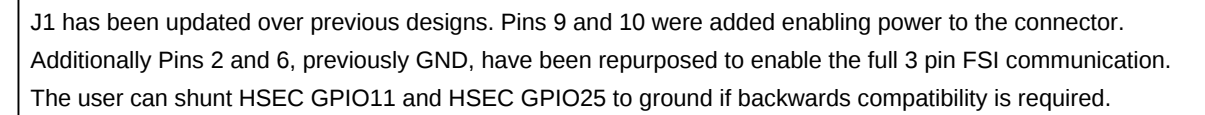
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	Sept 13, 2023	PL	Initial Draft
A	N/A	Jan 29, 2024	PL	Added Test Point for 5V0 and 3V3 Dampening resistor tuned per characterization Switched U1 from PBK to PDT package Minor changes to silkscreen and GND pour Adjustments to analog signal routing



Power to the MCU is either supported by the USB-C on the left or through the HSEC

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Orderable: TMDSCNCD28P55X	Designed for: Public Release	Mod. Date: 1/31/2024
TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 10
Drawn By: Peter Luong	File: MCU132A_CoverSheet.SchDoc	Size: B
Engineer: Peter Luong	Contact: http://www.ti.com/support	



A

B

C

D

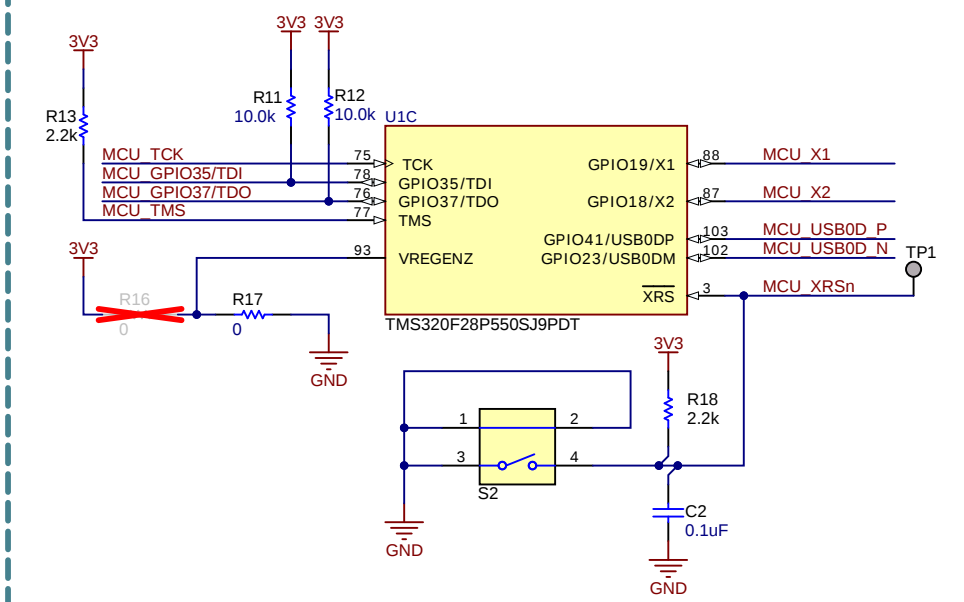
A

B

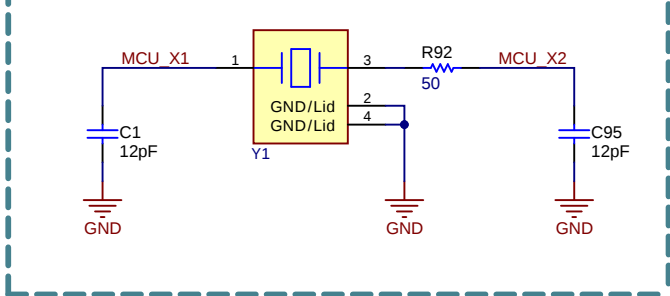
C

D

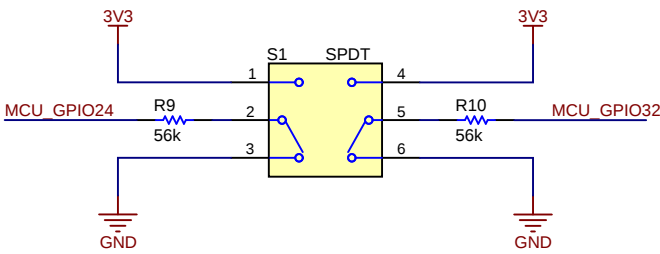
JTAG and Reset



20 MHz External Crystal



Boot Mode Switch

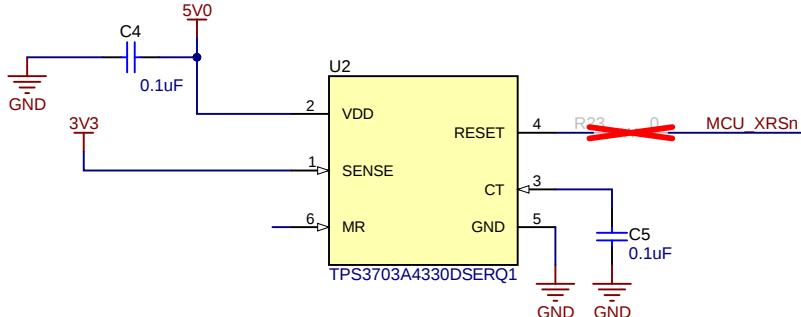


Boot Mode Selection Chart

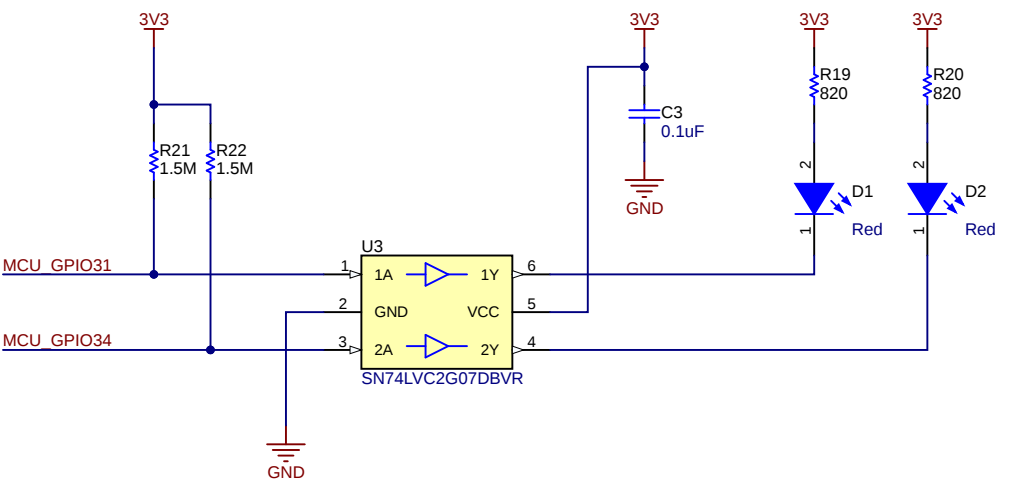
(S2: UP is '1', DOWN is '0')

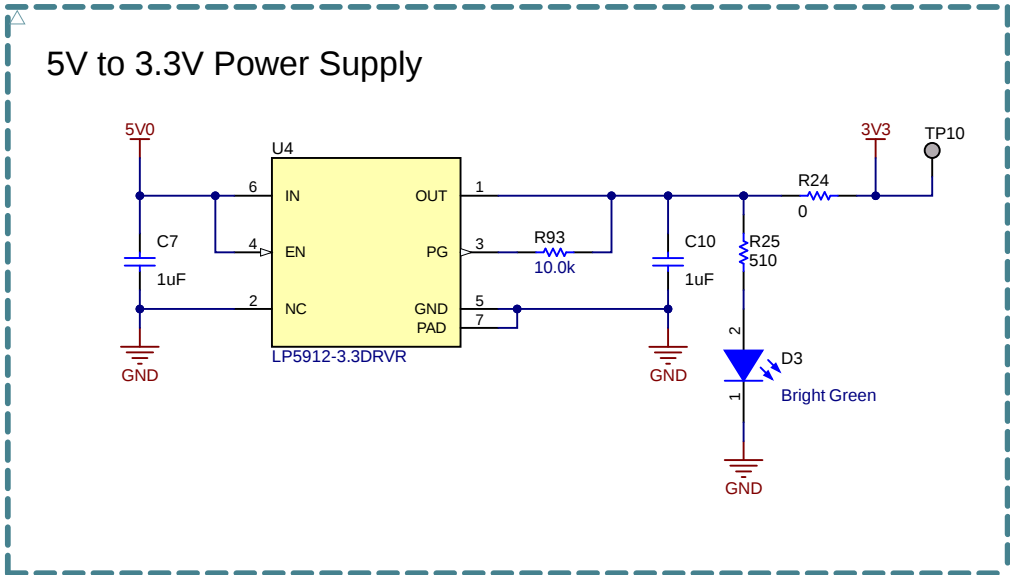
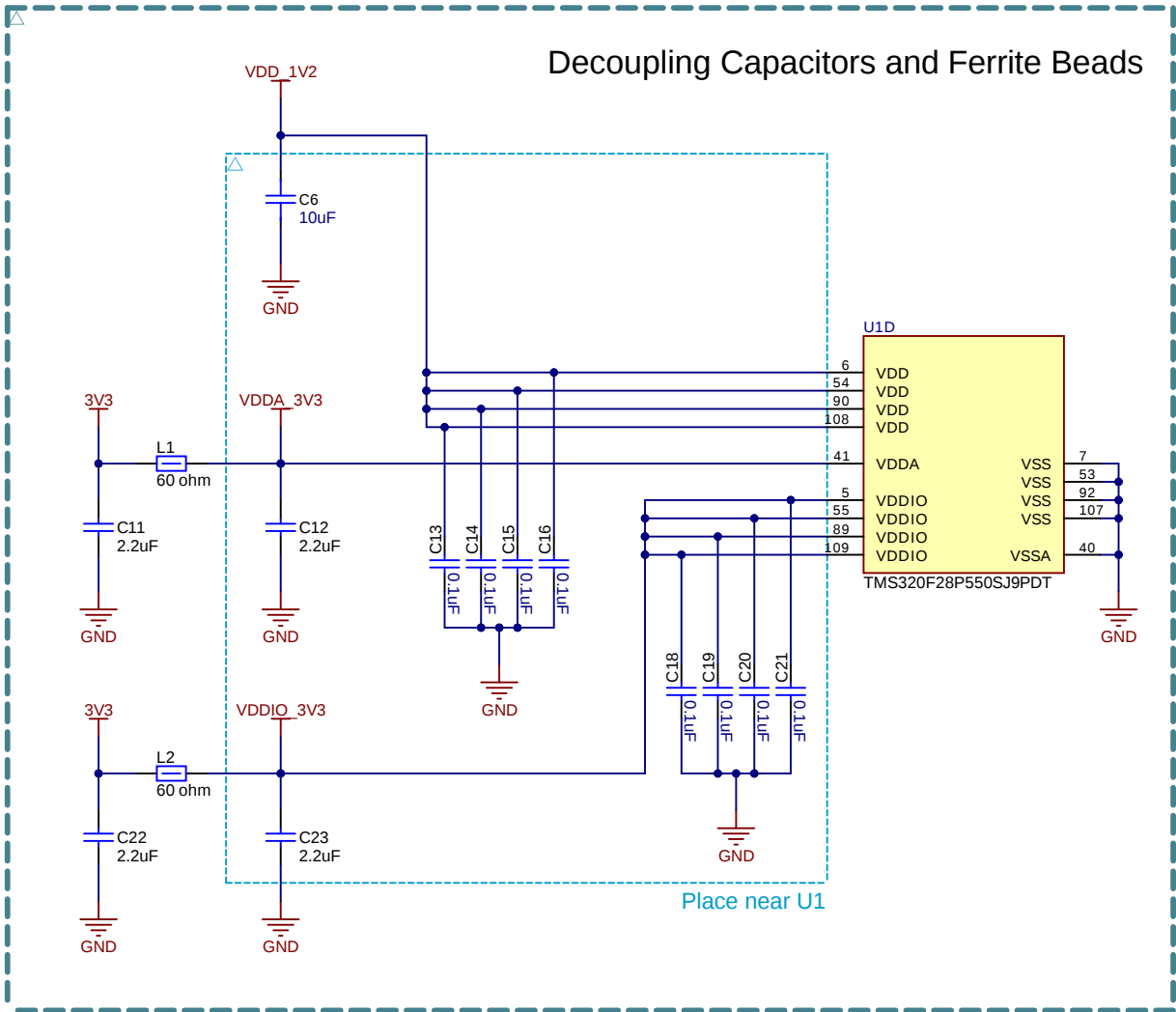
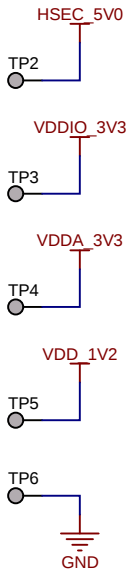
Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN (MCAN-NONFD)
03	1	1	Boot from Flash (USB)

System Supervisory Circuitry



LEDs





The F28P55x controlCARD uses the internal VREG to generate the 1.2V voltage rail for VDD.

For custom boards using external VREG mode, recommend to use dual-output DC-DC (e.g., TPS62441) to generate both 3.3V and 1.2V supplies.

The schematic diagram illustrates the USB to UART bridge circuit. The central component is the TPD4E05U06DQAR (U10) chip. The USB D+ and D- lines (pins 1 and 2) connect to the MCU USB0D P and N lines through resistors R54 and R55. The USB CC1 and CC2 lines (pins 4 and 5) connect to GND. The MCU USB0D P and N lines are also connected to GPIO41 and GPIO23 respectively.

Switch Truth Table		
MCU_GPIO70 STATUS	DESCRIPTION	USB_MODE
1 (HIGH)	UB_CC1 & USB_CC2 are pulled up	Host mode (DFP)
0 (LOW)	UB_CC1 & USB_CC2 are strongly pulled down	Device mode (UFP)

In this controlCARD, a standard GPIO is used to detect changes to these signals.

USB Type-C Connector - XDS110 side

USB Type-C Connector - XDS110 side

EMU_5V0

J3

A4 VBUS B4 VBUS

A9 VBUS B9 VBUS

XDS D N A7 DN1 B7 XDS D N

XDS D P A6 DP1 B6 XDS D P

A3 SSTXN1 B3

A2 SSTXP1 B2

A10 SSRXN2 B10

A11 SSRXP2 B11

XDS CC1 A5 CC1 B5 XDS CC2

A8 SBU1 B8

A1 GND B1

A12 GND B12

M1 GND M2

S1 Shield S4

S2 Shield S3

632723300011

R65 5.1k

EMU_GND

R62 1.00M

C62 3.3nF

EMU_GND

R64 5.1k

EMU_GND

U13

1 D1+ 10 XDS D P

2 D1- 9 XDS D N

3 GND 8

XDS CC1 4 D2+ 7 XDS CC1

XDS CC2 5 D2- 6 XDS CC2

TPD4E05U06DQAR

USB Isolated Power

The diagram illustrates a USB Isolated Power supply circuit. The input is a USB connection (VCC, EN, CLK) connected to an SN6505BDBVR (U12) isolator. The isolator's output (D1, D2, GND) is connected to a transformer (T1). The transformer's secondary (1, 2, 3, 4) is connected to a full-bridge rectifier (D9, D10). The rectifier's output is filtered by capacitors C65 (0.1uF) and C66 (10uF) to produce an isolated 5V output (ISO_Pout_5V0). A 10uF capacitor (C63) is connected between the transformer's primary and the isolated output. A 0.1uF capacitor (C64) is connected between the USB input and the isolator's input. A 10uF capacitor (C67) is connected between the isolated output and ground. A 10uF capacitor (C63) is connected between the transformer's primary and the isolated output. A 10uF capacitor (C63) is connected between the transformer's primary and the isolated output.

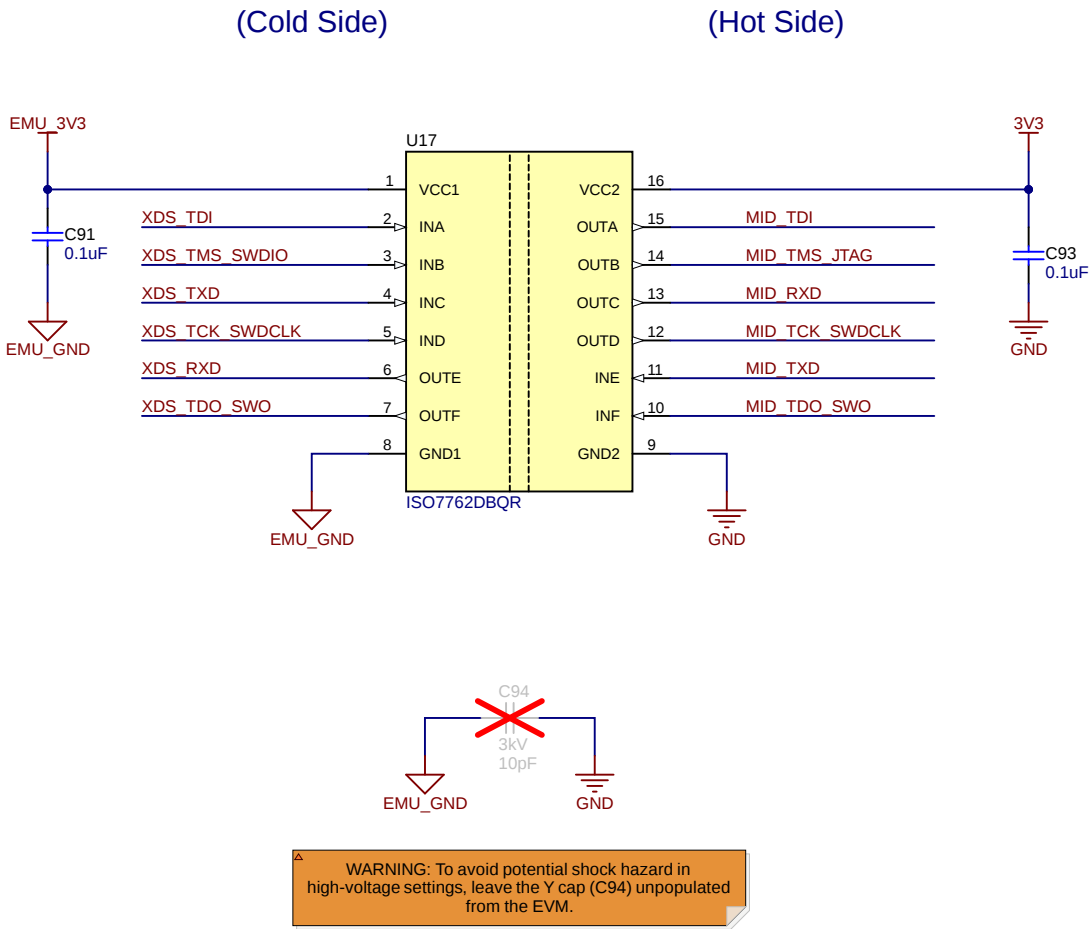
Power Selection Switch

The circuit diagram illustrates a Power Selection Switch using the TPS2113ADRBR IC (U14). The IC is configured to select between two 5V0 power sources: HSEC_5V0 and ISO_Pout_5V0. The selection is based on the voltage levels of these sources relative to GND. The circuit includes several passive components: capacitors C69 (0.1uF), C70 (10uF), C71 (0.1uF), and C68 (10uF); resistors R66 (2.2k), R67 (10k), R68 (10k), R69 (10k), R70 (4.7k), R71 (1.00k), R72 (430), R73 (1.2k), and R74 (0). A red LED (D6) provides visual feedback. The output of the switch is labeled POWER_SWITCH_OUT.

HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

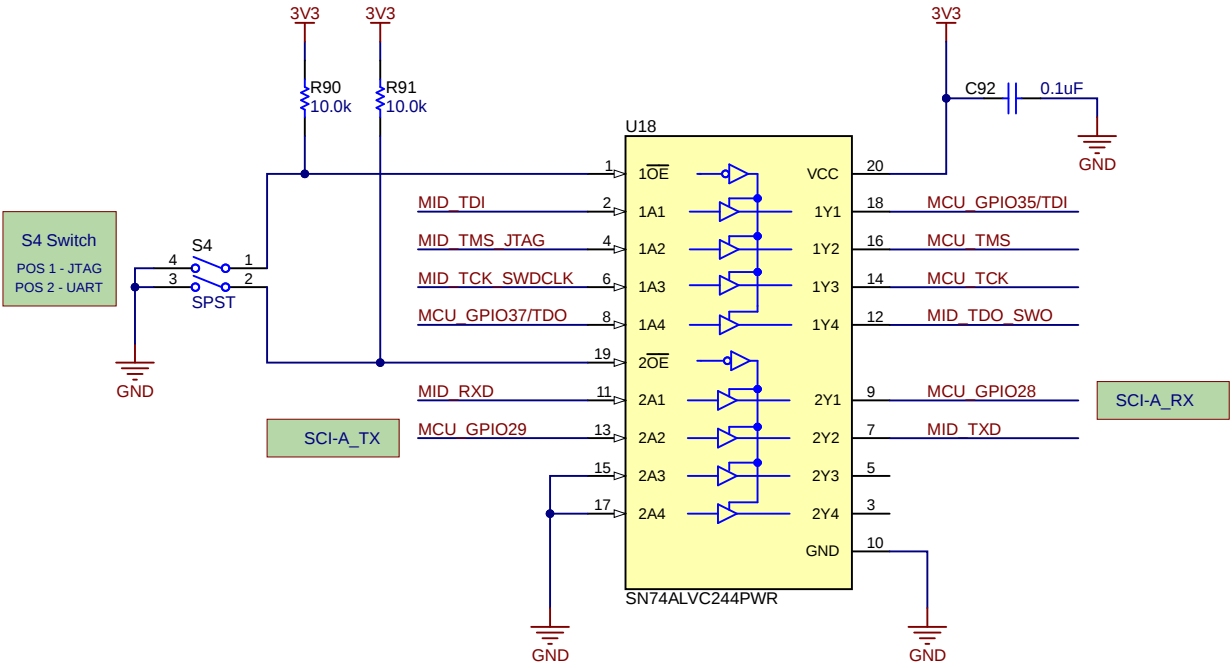
Switch Truth Table		
HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.



S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins





PCB Number: MCU132
PCB Rev: A

PCB
LOGO
Texas Instruments



PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

LBL1
PCB Label

THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5
Assembly Note
Clip off KEY pin 9 of J1 connector header

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Orderable: TMDSCNCD28P55X		Designed for: Public Release	Mod. Date: 10/10/2023
TID #: N/A		Project Title: F28P55x controlCARD	
Number: MCU132	Rev: A	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 10 of 10
Drawn By: Peter Luong		File: MCU132A_Hardware.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

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