TMS320DM646x DMSoC
Video Port Interface (VPIF)

User's Guide

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About This Manual

Describes the operation of the video port interface (VPIF) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUEP8 — ***TMS320DM646x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRUEP9 — ***TMS320DM646x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

SPRUEQ0 — ***TMS320DM646x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRAA84 — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — *TMS320C64x+ DSP Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Video Port Interface (VPIF)

1 Introduction

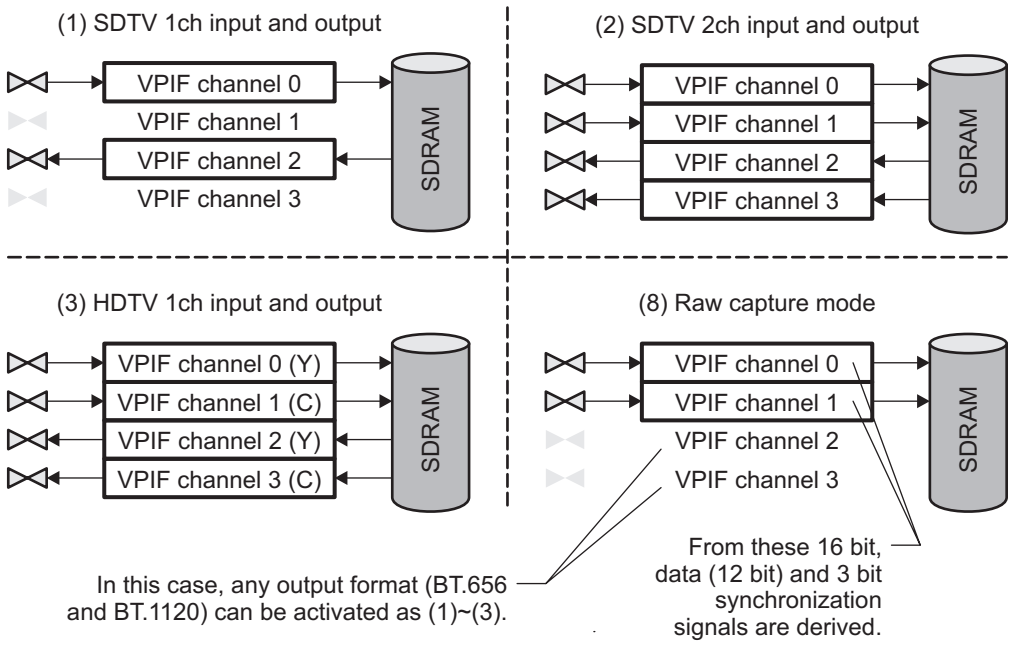
This document describes the operation of the video port interface (VPIF) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

1.1 Overview

The video port interface (VPIF) is a receiver and transmitter of video data with two input channels (channel 0 and 1) and two output channels (channel 2 and 3). Channels 0 and 1 have the same architecture, and channels 2 and 3 have the same architecture.

The input and output channel combinations of the VPIF are shown in Figure 1.

Figure 1. Input and Output Channels of VPIF



1.2 Features

The functional features of the VPIF are:

- Three speed grades (99 MHz, 108 MHz, and 150 MHz) available for the VPIF. See device-specific data manual for the part number associated with each speed grade.
- ITU-BT.656 format is supported.
- ITU-BT.1120, such as 1080I60, 1080P30, and 1080P60 (150 MHz VPIF devices only), and SMTPE 296 formats are supported.
- Raw data capturing function (receiver only; 8/10/12-bit format) is supported.
- VBI data storage is supported on BT.656 (SDTV) mode.
- Data clipping function for output (silicon revision 3.0 and later revisions only).

1.3 Features Not Supported

The following functions are not supported:

- ITU-BT.601 format
- Separated synchronization format (which needs vertical and horizontal synchronization signal and field ID signal in independence to pixel data) is not supported (except in case of raw data capturing mode).

1.4 Functional Block Diagram

A block diagram of the VPIF is shown in Figure 2. A block diagram of the internal architecture of the VPIF is shown in Figure 3.

Figure 2. Video Port Interface (VPIF) Block Diagram

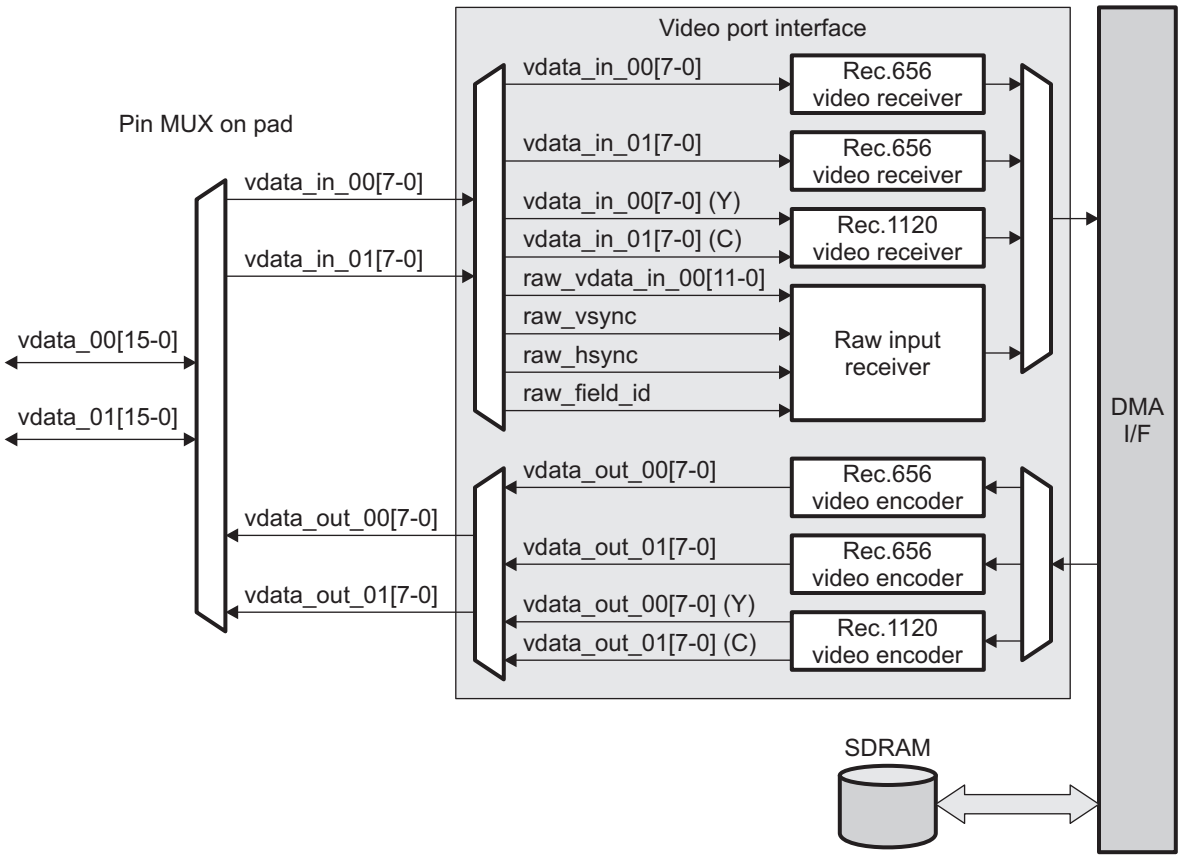
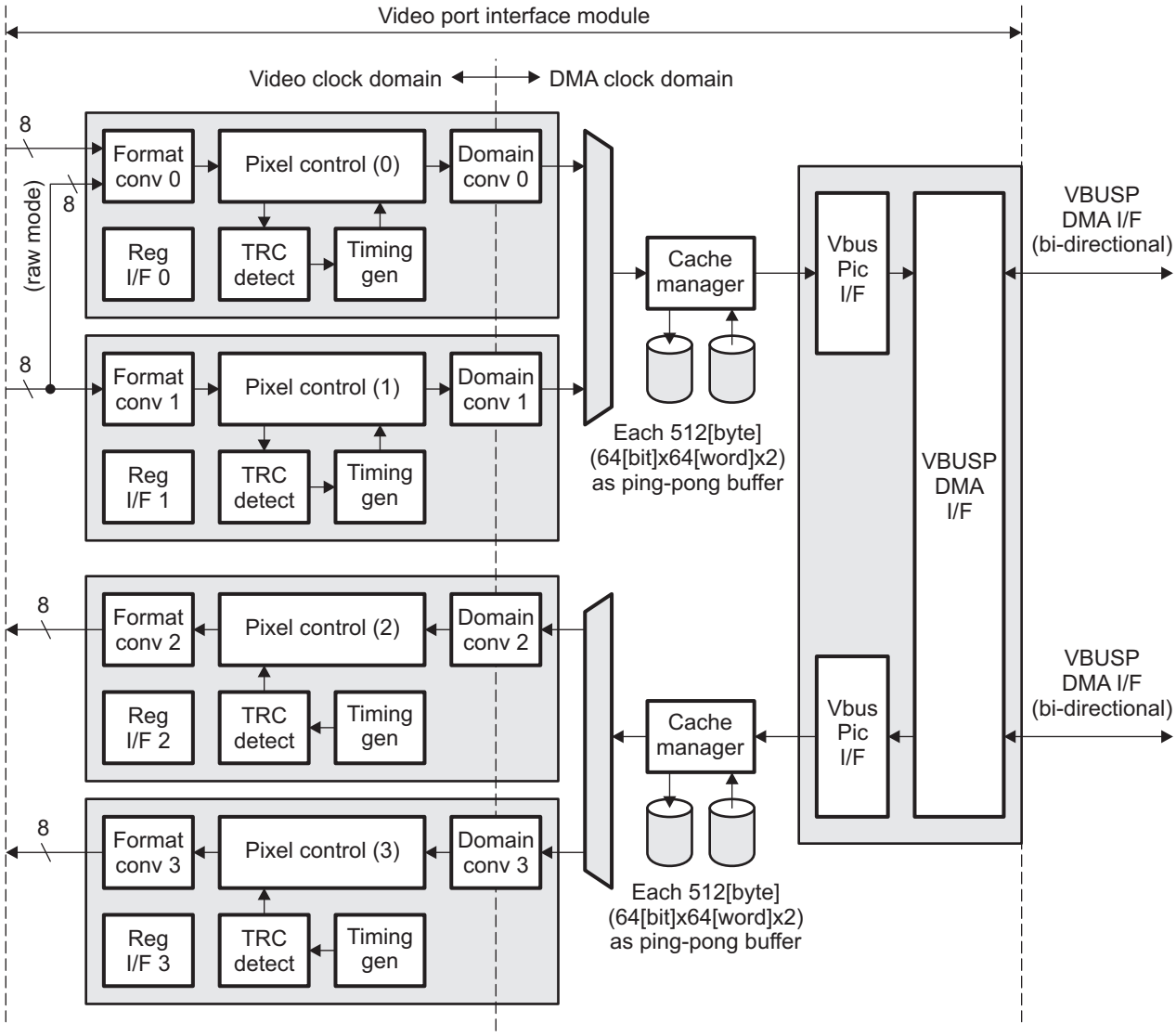


Figure 3. VPIF Architecture Block Diagram



1.5 Supported Use Cases

The VPIF module has two input channels and two output channels. All channels can be activated simultaneously (see Table 1). One VPIF module has 4 GL type buffers (64 bit × 64 word single port SRAM).

- Channels 0 and 1 are prepared only for input.
- Channels 2 and 3 are prepared only for output.

As shown in Table 1, both NTSC and PAL formats are supported. Note that VBI is not supported for ITU-BT.1120 (HDTV). VBI support is necessary only for ITU-BT.656 (SDTV); in this case, VBI format has to be based on ITU-BT.1364. Table 2 describes the usage combinations that are supported in the VPIF.

Table 1. Supported Formats on VPIF

	TV Definition Format	
TV System Format	**HDTV (rec. 1120) (no support of ancillary data)**	**SDTV (rec. 656) (ancillary data is based on BT.1364)**
NTSC	1125 line/60 field (vertical)	525 line/60 field (vertical)
	2200 pixel (horizontal)	858 pixel (horizontal)
PAL	1250 line/50 field (vertical)	625 line/50 field (vertical)
	2304 pixel (horizontal)	864 pixel (horizontal)
Square pixel common image format	1080P30, 1080P60(1)	-

(1) 1080P60 is supported on 150 MHz VPIF devices only.

Table 2. Input and Output Usage Combinations on VPIF

	Output Format		
Input Format	**HDTV Output**	**SDTV Output**	**No Output**
HDTV input (1 channel only)	√	√	√
Raw capture mode	√	√	√
SDTV input	√ (both 1-channel and 2-channel input)	√ (both 1-channel and 2-channel input/output)	√ (both 1-channel and 2-channel input)
No input	√	√ (both 1-channel and 2-channel output)	

2 Architecture

This section describes the architecture of the video port interface module (VPIF).

2.1 Clock Control

The VPIF has 4 clock input pins and 2 clock output pins. Each channel has 1 clock input pin and has clock edge control using the CLK_EDGE_CTRL_CH*n* bit in the channel *n* control register (CH*n*_CTRL). You can provide a clock for an external device on channel 2 or 3 using the CH2_CLKEN bit in CH2_CTRL or the CH3_CLKEN bit in CH3_CTRL. The source clocks for the VPIF are selected using the video interface clock control register (VIDCLKCTL) in the System module. You must enable the source clock for the VPIF using the video interface source clock disable register (VSCLKDIS) in the System module. The VSCLKDIS is also used to disable the clock inputs when changing the source clock to ensure glitch-free operation.

2.2 Signal Descriptions

Table 3 describes the pin assignment on the VPIF. The video data input ports are for receiving video stream and capturing raw data; the two modes are controlled by the CH0_FORMAT bit in the channel 0 control register (CH0_CTRL). Shaded signals in Table 3 are synchronization signals that are necessary for capturing raw data.

Table 3. Pin Multiplexing Control

Pin Name	Role on rec. 656	Role on Raw Data Capturing	Pin Name	Role on rec. 656	Role on Raw Data Capturing
VP_D[0]	vin_data_00[0]	vin_data_raw[0]	VP_D[8]	vin_data_01[0]	vin_data_raw[8]
VP_D[1]	vin_data_00[1]	vin_data_raw[1]	VP_D[9]	vin_data_01[1]	vin_data_raw[9]
VP_D[2]	vin_data_00[2]	vin_data_raw[2]	VP_D[10]	vin_data_01[2]	vin_data_raw[10]
VP_D[3]	vin_data_00[3]	vin_data_raw[3]	VP_D[11]	vin_data_01[3]	vin_data_raw[11]
VP_D[4]	vin_data_00[4]	vin_data_raw[4]	VP_D[12]	vin_data_01[4]	not used
VP_D[5]	vin_data_00[5]	vin_data_raw[5]	VP_D[13]	vin_data_01[5]	raw_field_id
VP_D[6]	vin_data_00[6]	vin_data_raw[6]	VP_D[14]	vin_data_01[6]	raw_h_sync
VP_D[7]	vin_data_00[7]	vin_data_raw[7]	VP_D[15]	vin_data_01[7]	raw_v_sync
VP_CLKIN0	vin_data_00_clk	vin_data_raw_clk	VP_CLKIN1	vin_data_01_clk	vin_data_raw_clk

2.3 Pin Multiplexing

On the DM646x DMSoC, the VPIF is pin multiplexed to accommodate multiple peripheral functions in a smaller possible package. Pin multiplexing is controlled by using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the VPIF.

2.4 Video Stream Capture Mode

The video stream capture mode is for digital interface of video data that is defined by BT.656/1120 and SMTPE 296.

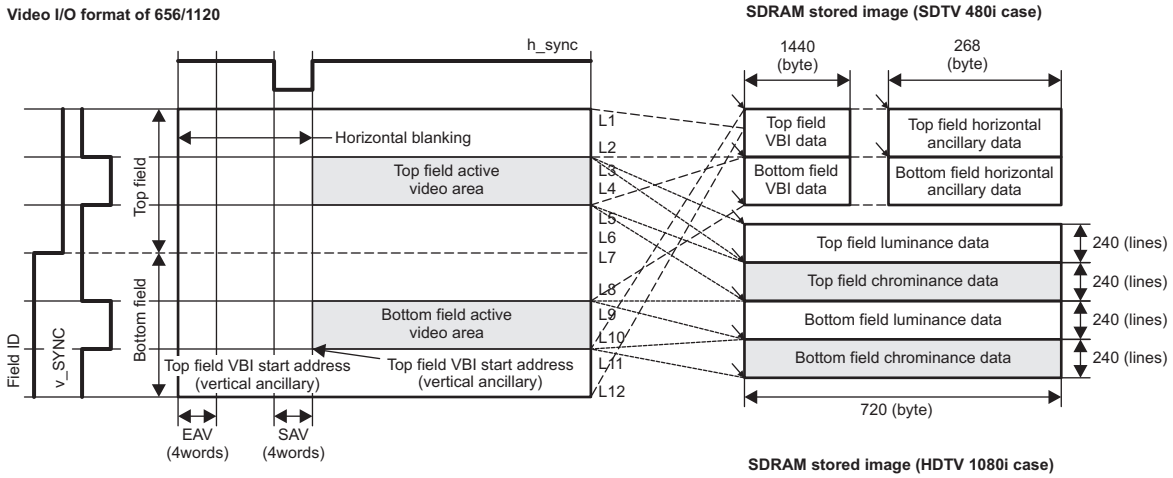
2.4.1 Line Format

In the VPIF, both the input data and output data are stored in SDRAM. All video data is divided into image data and VBI data. The image data is divided into luminance and chrominance data in each field, independently. Each start address to be stored in SDRAM can be configured by the ARM processor through the register interface.

2.4.1.1 Interlaced Image

The stored image of the video I/O data is shown in Figure 4 (for interlaced image).

Figure 4. Storage Format of Data in SDRAM (Interlaced Image)



	Role of each line number	HDTV case	SDTV case	F	V
L1	First line of top field	1 (1)	4 (1)	0	1
L2	Last line of digital field blanking for top-field	40 (44)	19 (22)	0	1
L3	First line of top field for active video area	41 (45)	20 (23)	0	0
L4	Last line of top-field for active video area	557 (620) (video size = 517/576)	263 (310)	0	0
L5	First line of digital field blanking for bottom of field	556 (621)	264 (311)	0	1
L6	Last line of top-field	563 (625)	265 (312)	0	1
L7	First line of bottom field	564 (626)	266 (313)	1	1
L8	Last line of digital field blanking for bottom field	602 (669)	282 (335)	1	1
L9	First line of bottom field for active video area	603 (670)	283 (336)	1	0
L10	Last line of bottom field for active video area	1120 (1245)	525 (623)	1	0
L11	First line of digital field blanking for top-field	1121 (1246)	1 (624)	1	1
L12	Last line of bottom field	1125 (1250)	3 (625)	1	1

NOTE: L11 is regarded as the start line of the frame in the VPIF. The line number written is the same as the standard book of BT.656 and BT.1120. In interlace case, all register values, such as SDRAM base address, are detected at timing of L11.

All parameters (L1 to L11) and vertical screen size (distance between L1 to L12) in Figure 4 is configured by the software register. If the V-sync value on the EAV/SAV signal is different from the configured value on registers L1 to L12, the configured value has a higher priority than the detected V-sync value.

In Figure 4, the video data is distinguished into eight categories:

- Top field VBI data in vertical ancillary area
- Top field VBI data in horizontal ancillary area
- Bottom field VBI data in vertical ancillary area
- Bottom field VBI data in horizontal ancillary area
- Top field luminance data
- Top field chrominance data
- Bottom field luminance data
- Bottom field chrominance data

For each data, the following elements are a configuration parameter of each function:

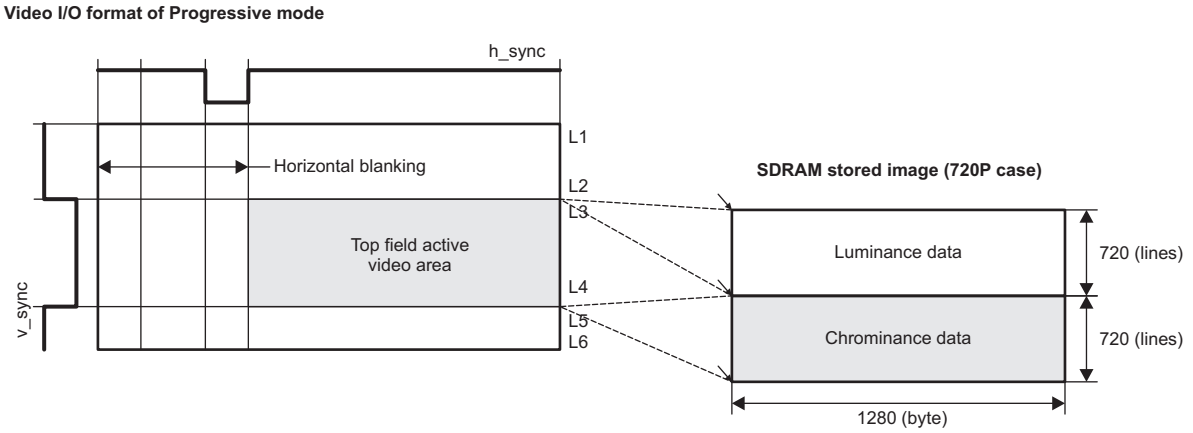
- Start address in SDRAM (corresponding to the start position of the storage area). (This data is prepared for top field and bottom field, independently. Other data is prepared for common use in top and bottom field.)

- Start position (horizontal and vertical), which is defined as a related position from the (0,0) position defined for VBI data output (VBI data only).
- Horizontal data size (VBI data only) to be read from SDRAM.
- Vertical image size to be stored in SDRAM.
- Address line offset (byte: minimum unit size = 8 bytes).
- Sub-picture size (byte) in horizontal direction (image data only).

2.4.1.2 Progressive Image

The stored image of the video I/O data is shown in Figure 5 (for progressive image).

Figure 5. Storage Format of Data in SDRAM (Progressive Image)



	Role of each line number	720P	1080P	F	V
L1	First line of upper blanking for the frame	1	1	0	1
L2	Last line of upper blanking for the frame	25	41	0	1
L3	First line of the frame for active video area	26	42	0	0
L4	Last line of the frame for active video area	745	1121	0	0
L5	First line of lower blanking for the frame	746	1122	0	1
L6	Last line of lower blanking for the frame	750	1125	0	1

(1) The register value (such as SDRAM storage address) is detected at timing of L1 in progressive case. Data on L5 to L6 is stored into a different SDRAM area from data on L1 to L2 because the base address is changed at timing of L1. If you would like to use ancillary data, you need to insert the ancillary data on the L1 to L2 area.

(2) 1080P60 is supported on 150 MHz VPIF devices only.

All parameters (L1 to L6) and vertical screen size (distance between L1 to L6) in Figure 5 is configured by the software register. If the V-sync value on the EAV/SAV signal is different from the configured value on registers L1 to L6, the configured value has a higher priority than the detected V-sync value.

In Figure 5, the video data is distinguished into four categories:

- VBI data in vertical ancillary area
- VBI data in horizontal ancillary area
- Luminance data
- Chrominance data

For each data, the following elements are a configuration parameter of each function:

- Start address in SDRAM (in VBI, two area start address values should be configured).
- Start position (horizontal and vertical), which is defined as related position from the (0,0) position defined for VBI data output (VBI data only).

- Horizontal data size (VBI data only) to be read from SDRAM.
- Vertical image size to be stored in SDRAM.
- Address line offset (byte: minimum unit size = 8 bytes).
- Sub-picture size (byte) in horizontal direction (image data only).

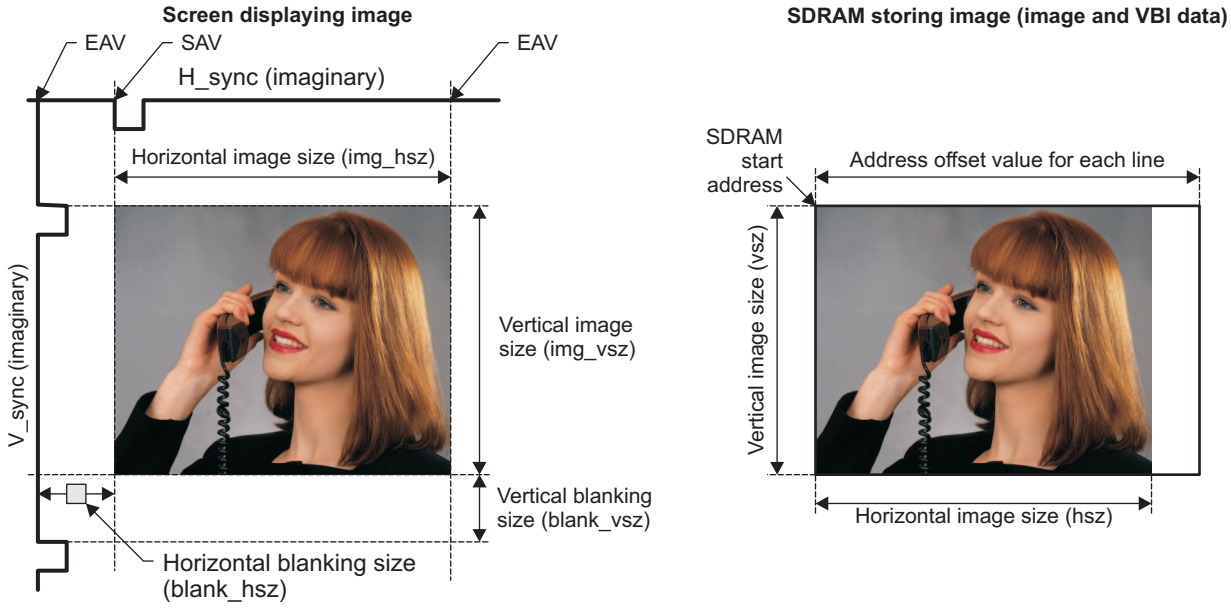
2.4.2 Functional Performance Image

In this section, we describe the functional performance that is related to the SDRAM storage format. These are two functions, the receiver (VPIF receives input video data) and the transmitter (VPIF transmits video data stored in SDRAM).

- Image Data Input: In interlace mode (Figure 4), the VPIF starts to store the input image data in SDRAM horizontally between the SAV code and the EAV code and vertically between L3 to L4 or L9 to L10. In progressive mode (Figure 5), the video image data exists only between L3 to L4.
- Horizontal VBI Data Input: In interlace mode (Figure 4), the VPIF starts to store the input horizontal blanking data in SDRAM just after the EAV code in the horizontal blanking area between L1 to L12. In progressive mode (Figure 5), in the horizontal blanking area between L1 to L6.
- Vertical VBI Data Input: In interlace mode (Figure 4), the VPIF module starts to store the input vertical blanking data in SDRAM horizontally between the SAV code and EAV code and vertically between L1 to L2, L5 to L8, or L11 to L12. In progressive mode (Figure 5), between L1 to L2 or L5 to L6.
- Image Data Output: In interlace mode (Figure 4), the VPIF starts to read the source image data from SDRAM and asserts the read data to display horizontally between the SAV code and the EAV code and vertically between L3 to L4 or L9 to L10. In progressive mode (Figure 5), only L3 to L4 is displayed.
- Horizontal VBI Data Output: The VPIF starts to read the source horizontal blanking data from SDRAM and asserts the data from the configured start position with the configured size (both horizontal and vertical). Other than the configured area in horizontal blanking area should be filled with 10h (luminance position) or 80h (chrominance position).
- Vertical VBI Data Output: The VPIF starts to read the store vertical blanking data from SDRAM and asserts the data from the configured start position with the configured size (both horizontal and vertical), Other than the configured area in horizontal blanking area should be filled with 10h (luminance position) or 80h (chrominance position).

The functional image is shown in Figure 6. Addressing methods are discussed in Section 2.4.3.

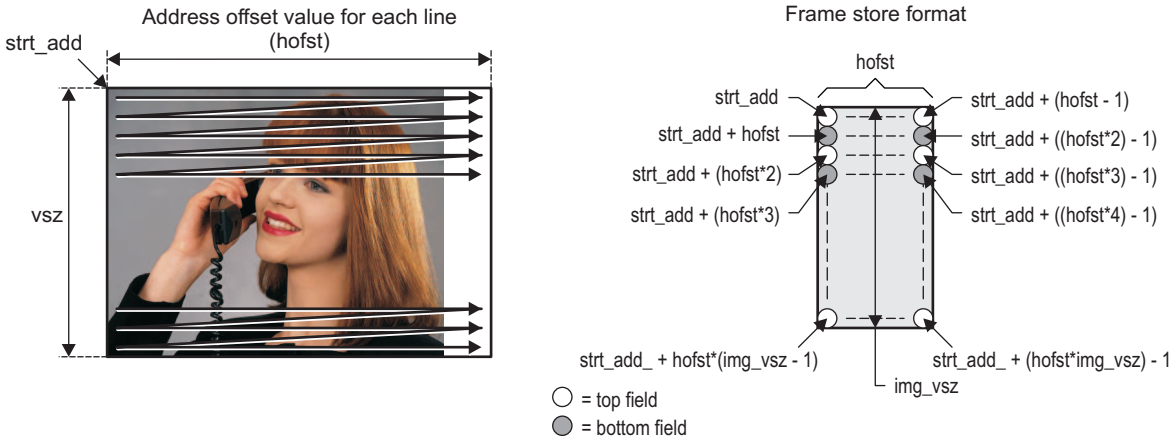
Figure 6. Relationship Between SDRAM Stored Image and Incoming (Outgoing) Image



2.4.3 SDRAM Addressing

You have to define the address offset value for each line and select the storage method in SDRAM from two methods, field mode and frame mode, as shown in Figure 7.

Figure 7. SDRAM Storage Method



In Figure 7, the upper illustration is a functional image of the SDRAM storage method. With register configuration (horizontal and vertical image size, and horizontal sub-picture size), a detailed address for each pixel is defined. The lower left illustration shows the raster scanning format addressing in field format and the lower right illustration shows the frame format.

The INPUT_FIELD_OR_FRAME bit in the channel 0 control register (CH0_CTRL) and the OUTPUT_FIELD_OR_FRAME bit in the channel 2 control register (CH2_CTRL) defines the SDRAM storage format and these bits have no effect on the storage format in raster scanning mode. You should configure each register in field/frame mode as follows (based on the parameters shown in Figure 7):

- Field format:
  - Top and bottom field start address is *strt_add*
  - Line offset value per one field line is equal to *hofst*
- Frame format:
  - Top field start address is *strt_add*
  - Bottom field start address is *strt_add* + *hofst*
  - Line offset value per each field line is equal to *hofst* × *2*

2.4.4 VBI Data Transmit Function

The VPIF can insert VBI data in the horizontal and vertical blanking intervals. The source VBI data is prepared in SDRAM as a result of processing by the CPU (DSP or ARM). The VPIF reads the source data based on the register configuration of the VPIF and transmits to outside the DSP.

To reduce any redundant load of processing in the CPU (DSP or ARM), the CPU writes the result of the VBI data only into SDRAM and no stuffing data is prepared in SDRAM. You need to configure the control registers (shown in Figure 8 for interlaced mode) on the VPIF, in order to receive and transmit VBI data.

In Figure 8, two assignments are prepared for both horizontal ancillary data and vertical ancillary data in interlaced mode because ancillary data exists in both the top and bottom field blanking interval.

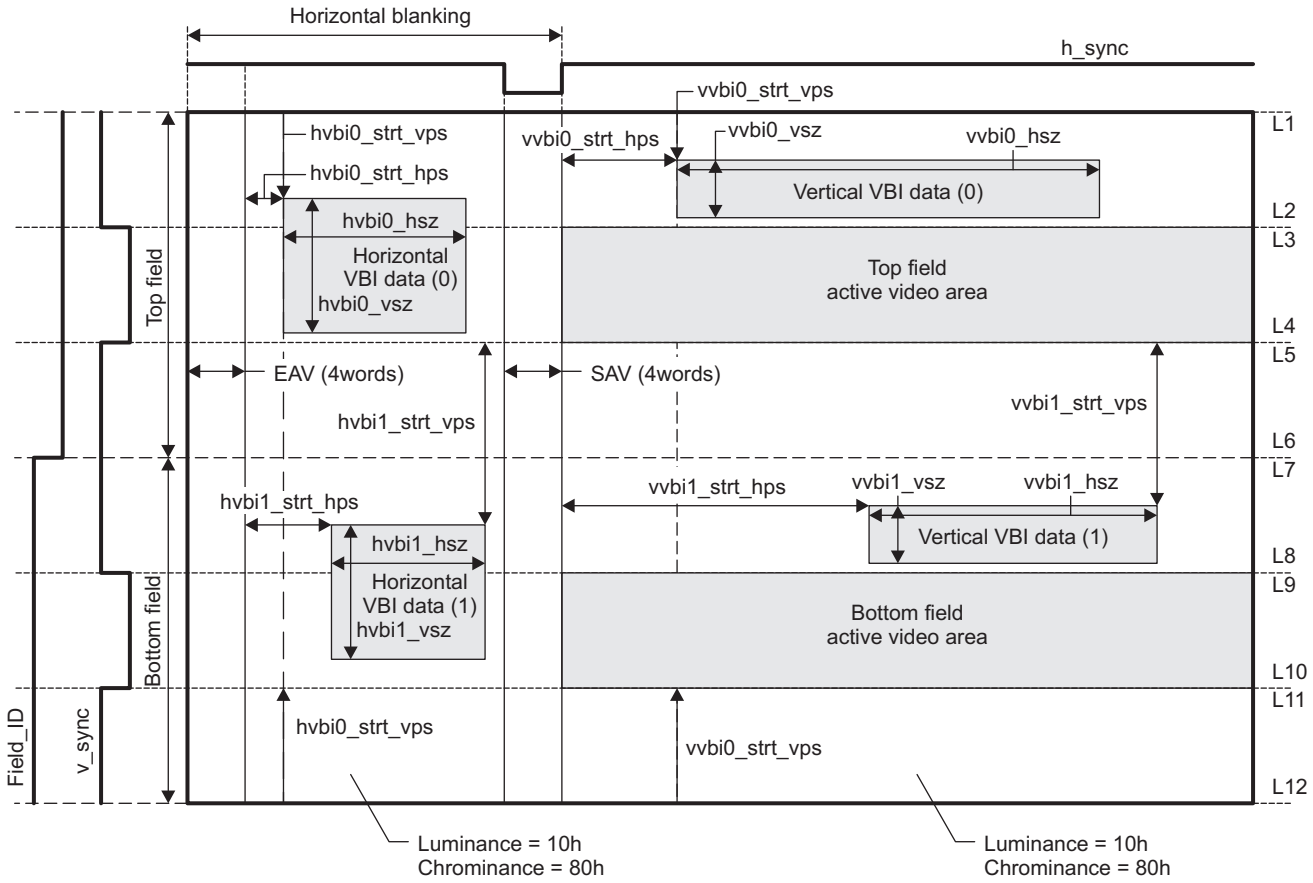
Each parameter is configured by the register interface of the VPIF. Note that the V-origin of each parameter in Figure 8 is a falling edge of the vertical synchronization signal that is defined in each video standard such as BT.656 or BT.1120.

In this register map,

- HANC = horizontal ancillary data between EAV and SAV (horizontal blanking interval).
- VANC = vertical ancillary data between SAV and EAV (horizontal active video area).

The value of the horizontal start position should be a multiple of 8 on both the horizontal and vertical ancillary data areas. You can define any value as the horizontal size that does not exceed each data area.

Figure 8. VBI Result Data Transmit Image for Interlaced Image



2.4.5 VBI Data Receive Function

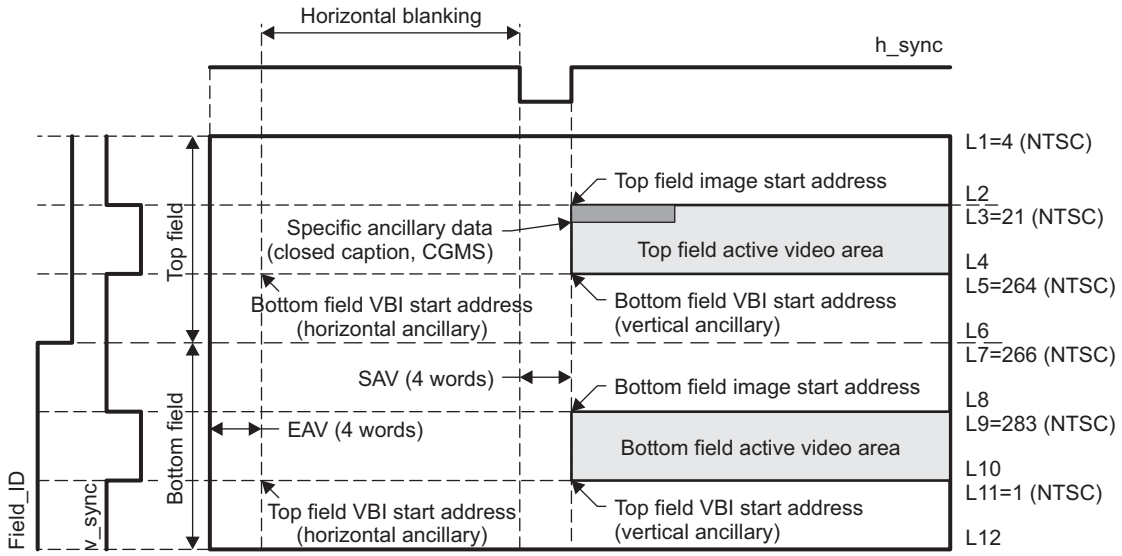
The VPIF receives VBI data in the horizontal and vertical blanking interval. If the VBI receive function is enabled, the VPIF receives all data in the horizontal and vertical blanking data. The VPIF cannot receive VBI data from any selectable area. The CPU has to receive valid data from this data and you have to prepare for the correct size of data buffer. For example in the NTSC case, the horizontal ancillary data needs 268 bytes × 525 lines and the vertical ancillary data needs 1440 bytes × 38 lines buffer.

The address line offset for the vertical ancillary data uses the channel *n* image data address offset register (CH*n*_IMG_ADD_OFST).

2.4.6 Processing Method for Specific Ancillary Data

The VPIF has the ability to capture/assert video ancillary data (Figure 9) that is not video image data but is VBI data. In most cases, video ancillary data is inserted in the blanking interval for either the horizontal or vertical direction. But in some cases, such as CGMS or closed-caption that is in Japanese and US applications, the line number where these kinds of ancillary data is inserted is in the active video area. In the case that ancillary data is inserted in the active video area, the VPIF regards the incoming (or stored data) as video data.

Figure 9. Image of Specific Ancillary Data on NTSC



2.4.7 Raw Data Capturing Function

The VPIF supports raw data capturing. With this function, you can connect a camera AFE output signal directly into an input port of the DSP. Usually, the output format of the camera AFE device is in raw format that consists of an RGB component (sometimes RGrGbB format). The following functions are supported:

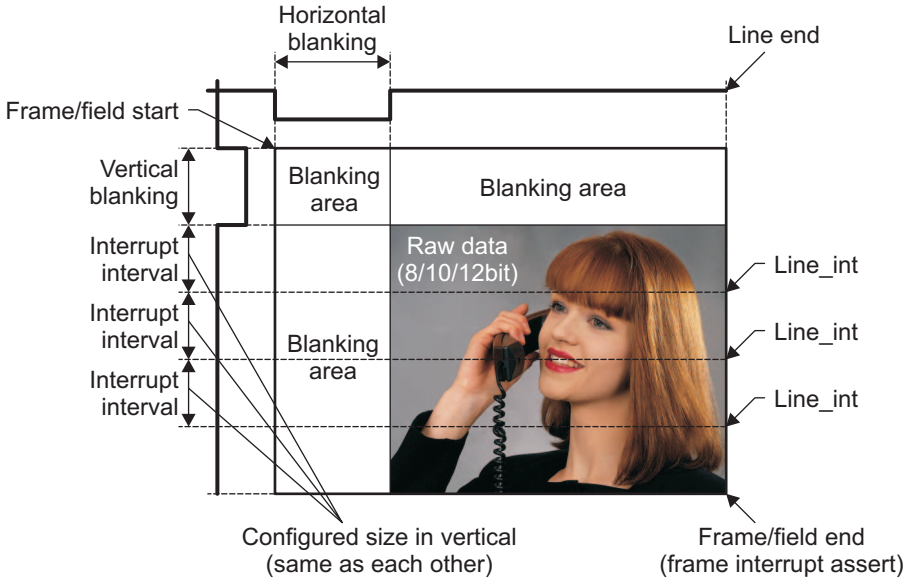
- Storing pixel data in SDRAM (no storage of blanking data).
- Data bit width varies from 8 bits/pixel, 10 bits/pixel, and 12 bits/pixel mode.
- Maximum screen size with valid pixel is 2048(H) × 1536(V) in frame format.
- All data should be stored in SDRAM in byte-aligned format.
- Selectable polarity for H/V pixel valid signal and field ID signal.
- Separated field storage (top field and bottom field are stored independently) and interleaved field storage (normal frame format) support in SDRAM storage.
- Two kinds of interrupt support. One is asserted once per each configured line size (line_interrupt) and the other is asserted at the end of the capture area (frame_interrupt). See Figure 10. Note that line_interrupt is only supported in raw mode. In other modes (BT.656, BT.1120, and SMPTE 296M), line_interrupt is not supported.
- Only raster scan format is supported in SDRAM storage format.

The following functions are not supported:

- No support of color space conversion from RGB to YCbCr.
- No CFA interpolation for each raw data pattern (such as Bayer or Foveon).
- No push-storage function on non-byte aligned data format (10 bits/pixel and 12 bits/pixel). Data should be stored in SDRAM in byte-aligned format.

The active period of each synchronization signal is regarded as the blanking area and any other area is regarded as the active video area that is stored in SDRAM. See Figure 10.

Figure 10. Functional Image of Raw Data Capturing Mode



NOTE: All register configurations related to raw capture mode are reflected with the falling edge of the internal V-sync, which source is raw_v_valid, in normal polarity (low = blanking, high = data).

2.4.7.1 Timing Chart on Raw Capture Mode

Both interlace and progressive interface modes are supported. The following signals are assigned to the interface signal of the raw capture mode:

- raw_h_valid: horizontal pixel valid signal (regarded as horizontal synchronization signal)
- raw_v_valid: vertical line valid signal (regarded as vertical synchronization signal)
- raw_field_id: field ID signal
- vin_data_raw[11:0]: raw data input (8 bits/pixel, 10 bits/pixel, and 12 bits/pixel)

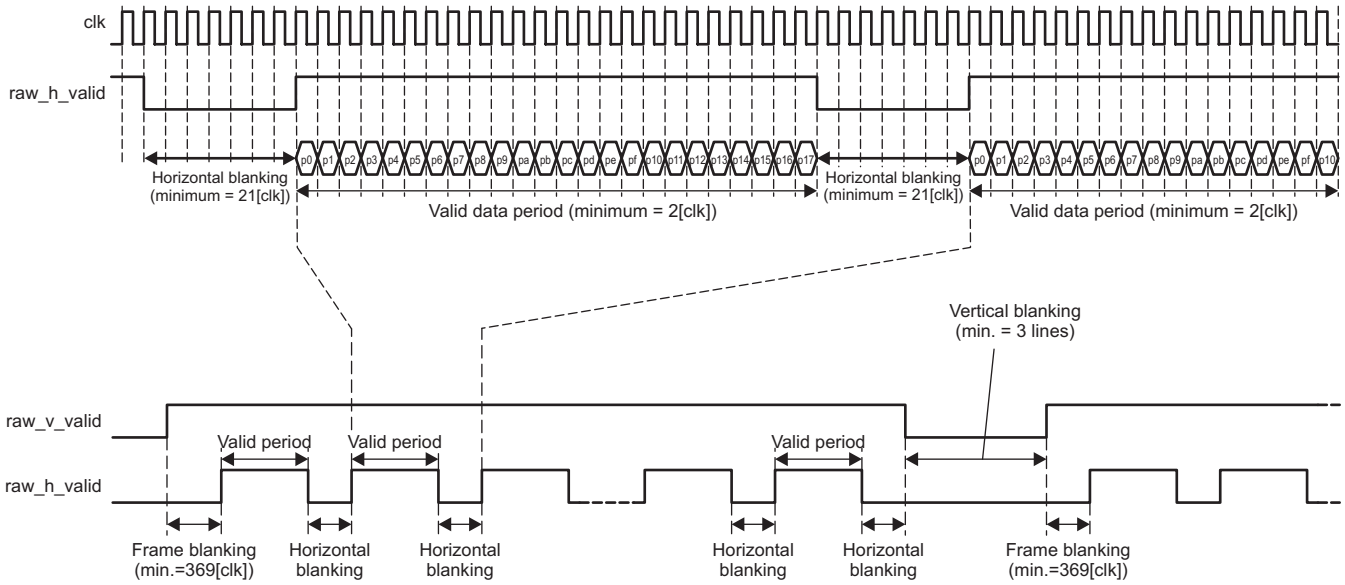
2.4.7.1.1 Progressive CCD Raw Capture Mode

See Figure 11. The falling edge of the vertical valid signal (raw_v_valid) and the horizontal valid signal (raw_h_valid) is regarded as the normal vertical and horizontal synchronization signals, respectively. The description of the detail value in Figure 11 is based on the description on the Micron Image sensor device specification sheet.

In this mode, data with an active period of both of raw_v_valid and raw_h_valid is detected by the VPIF and the VPIF stores the valid data in SDRAM. The falling edge of the two signals is regarded as the vertical and horizontal synchronization signals (the valid signal polarity can be configured by the channel 0 control register (CH0_CTRL)). You have to set the image address offset.

In this mode, without the activated period of raw_v_valid, no raw_h_valid signal is activated. Only in the period when both raw_v_valid and raw_h_valid signals are activated, the incoming data is regarded as valid data.

Figure 11. Waveform on Raw Capture Interface Normal Mode

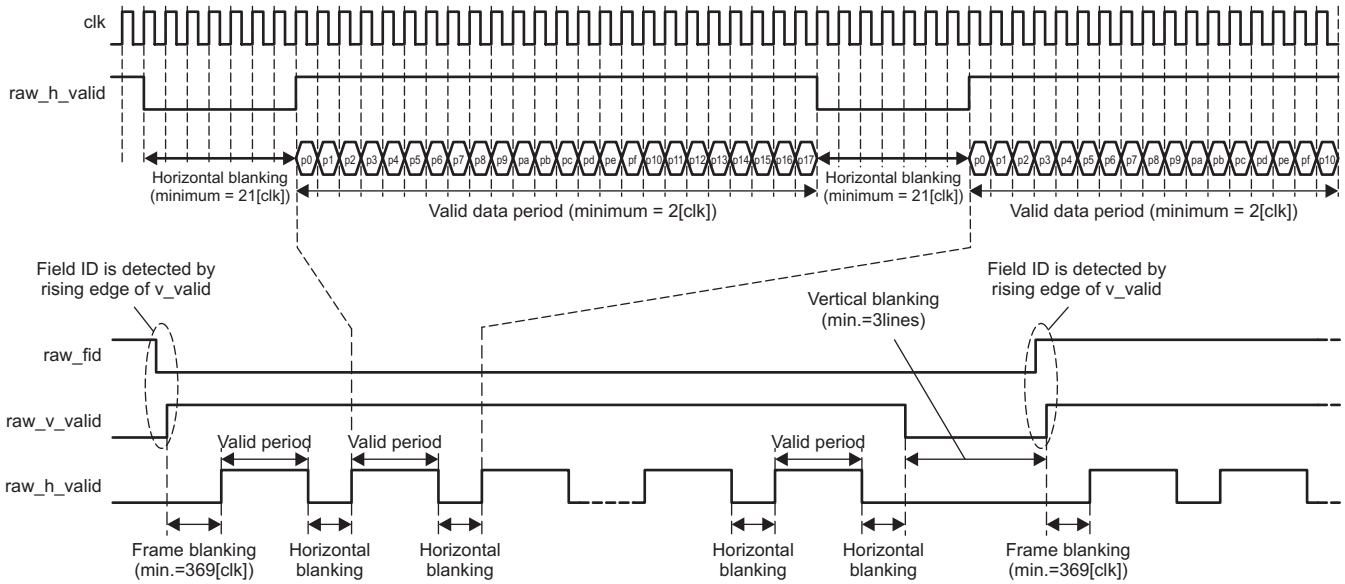


2.4.7.1.2 Interlace CCD Raw Capture Mode

See Figure 12. The falling edge of the vertical valid signal (raw_v_valid) and the horizontal valid signal (raw_h_valid) is regarded as the normal vertical and horizontal synchronization signals, respectively. The field ID (raw_fid) is detected at the rising edge of the raw_v_valid signal. The description of the detail value in Figure 11 is based on the description on the Micron Image sensor device specification sheet.

In this mode, data with an active period of both of raw_v_valid and raw_h_valid is detected by the VPIF and the VPIF stores the valid data in SDRAM. The falling edge of the two signals is regarded as the vertical and horizontal synchronization signals (the valid signal polarity and the field ID polarity can be configured by the channel 0 control register (CH0_CTRL)). You have to set the image address offset.

Figure 12. Waveform on Raw Capture Interface Interlaced Normal Mode



2.4.7.2 SDRAM Format on Raw Capture Mode

All active video data shall be stored in SDRAM in byte-aligned format. In order to do this, you have to stuff blanked room of data in 10 bits/pixel and 12 bits/pixel mode (see Figure 13. The MSB side of each data is stuffed by 0 and pixel 0 is the first pixel of each line.

Figure 13. Stuffing Manner in SDRAM Storage

	63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0
8[bit/pixel] mode	Pixel 7	Pixel 6	Pixel 5	Pixel 4	Pixel 3	Pixel 2	Pixel 1	Pixel 0
10[bit/pixel] mode	“000000” & pixel 3[9:0]		“000000” & pixel 2[9:0]		“000000” & pixel 1[9:0]		“000000” & pixel 0[9:0]	
12[bit/pixel] mode	“0000” & pixel 3[11:0]		“0000” & pixel 2[11:0]		“0000” & pixel 1[11:0]		“0000” & pixel 0[11:0]	

2.5 Clipping Function for Output

NOTE: The data clipping function for output is supported only on silicon revision 3.0 and later revisions.

In certain cases, the active video data or the ancillary data contains a combination of FF-00-00-XY, which is the same as the TRC (EAV/SAV). Many video encoders will consider this combination as the TRC. As a result, the synchronization might fail. In order to avoid this issue, the VPIF module is capable of clipping the output data, with the exception of the TRC, to be between 01h and FEh. The value 00h is clipped to 01h and the value FFh is clipped to FEh. All other values are kept unchanged.

The cliping function is enabled for both channel 2 and channel 3; and it can be activated in each channel separately. Each channel has two types of data region other than the TRC: the blanking region and the active video region; and the clipping function can be activated in each region separately. The following shows the register setup needed to activate clipping:

- To enable clipping in the blanking region for channel 2: set CH2_CTRL[14] = 1.
- To enable clipping in the active region for channel 2: set CH2_CTRL[13] = 1.
- To enable clipping in the blanking region for channel 3: set CH3_CTRL[14] = 1.
- To enable clipping in the active region for channel 3: set CH3_CTRL[13] = 1.

2.6 Reset Considerations

The VPIF does not have a software reset. When a hardware reset is asserted, all VPIF registers are set to their default values.

2.7 Initialization

The general procedure for VPIF initialization is:

NOTE: The VDD 3.3V I/O power-down control register (VDD3P3V_PWDN) in the System Module only controls the power to the I/O buffers. The Power and Sleep Controller (PSC) determines the clock/power state of the VPIF, see Section 2.9.

1. Enable I/O VDD power using the VDD 3.3V I/O power-down control register (VDD3P3V_PWDN) in the System Module (see Figure 14 and Table 4).
2. Program the corresponding bits in the DMA size control register (DMA_SIZE) and the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG).
3. Program the Emulation related registers, such as the emulation suspend control register (EMU_CTRL) in the VPIF and the emulation suspend source register (SUSPSRC) in the System Module (see Section 2.10 for more detail). The default values of SUSPSRC are configured to the ARM as the main processor.

Figure 14. VDD 3.3V I/O Power-Down Control Register (VDD3P3V_PWDN)

31		29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			USBV	CLKOUT	Rsvd	SPI	VLYNQ	Reserved		GMII	MII	MCASP1	MCASP0	PCIHPI1	PCIHPI0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO	WDTIM	TIM23	TIM01	PWM1	PWM0	UR2FC	UR2DAT	UR1FC	UR1DAT	UR0MDM	UR0DF	VPIF3	VPIF2	VPIF1	VPIF0

Table 4. VDD 3.3V I/O Power-Down Control Register (VDD3P3V_PWDN) Field Descriptions

Bit	Field	Value	Description
3-0	VPIF*n*		VPIF*n* power-down control.
		0	I/O cells powered up
		1	I/O cells powered down

2.8 Interrupt Support

2.8.1 Interrupt Events and Requests

The VPIF sends interrupt events (Table 5) to the ARM and/or the DSP. The VP_ERRINT interrupt is generated for the following reasons:

- For channels 0 or 1:
  - Internal buffer overflow
  - Length of eav2sav or sav2eav is not the same as the configured value
  - Bit error detected on 4th field of TRC
- For channels 2 or 3:
  - Internal buffer overflow

Table 5. VPIF Module Interrupts

ARM Event	Acronym	Source
0	VP_VERTINT0	VPIF
1	VP_VERTINT1	VPIF
2	VP_VERTINT2	VPIF
3	VP_VERTINT3	VPIF
4	VP_ERRINT	VPIF

2.8.2 Field/Frame Interrupt to CPU

This section describes the conditions of the field/frame based interrupt assertion from the VPIF. The VPIF interrupt is designed to make the processor identify the timing for updating the address register of the VPIF module. The timing of the interrupt from the VPIF module is different from the timing of the V-sync. The interrupt is generated when the last data transfer between the VPIF module and the VBUS is finished.

2.8.2.1 Interrupt Condition

The interrupt signal from the VPIF described in this section means the beginning of a field (or frame). A way to indicate the beginning of a field (or a frame) varies from the function mode; normal YC receive/transmit mode and CCD/CMOS capture mode differ because of the vertical synchronization signal.

The VPIF generates the following events as conditions for interrupt assertion:

- In normal YC receive/transmit mode, EAV on line L1 (and EAV on line L7 in field interrupt for bottom field). Both L1 and L7 are described in Figure 4 and Figure 5.
- In CCD/CMOS capture mode, starting edge for first line of vertical valid pixel area.

2.8.2.2 First Interrupt from VPIF

NOTE: The first vertical synchronization signal is defined as the transition from the L10 line to the L11 line in the interlace mode or from the L4 line to the L5 line in the progressive mode.

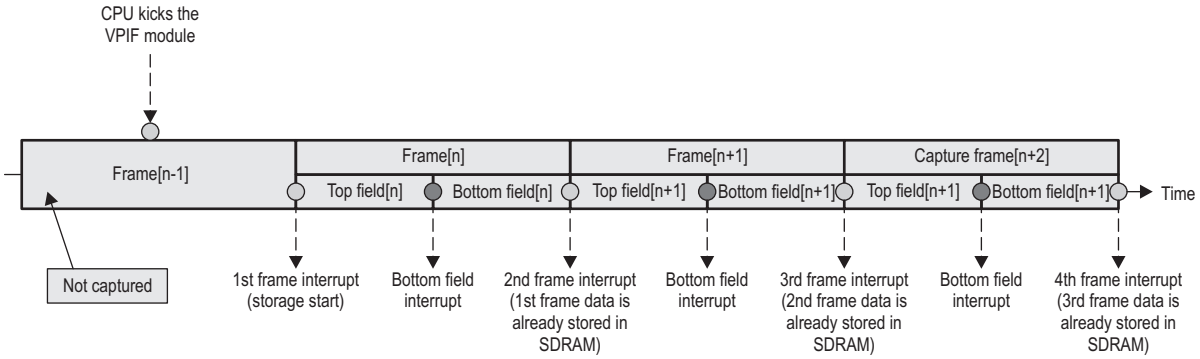
For raw capture mode, the VPIF immediately starts to capture the data if you enable middle of frame.

In channels 0 and 1, the VPIF starts to capture incoming picture data from the first vertical synchronization signal after the CPU activates the VPIF with register configuration. The interrupt signal from the VPIF is asserted when the vertical synchronization signal is received. So, no incoming data is written in SDRAM when the first interrupt is asserted from the VPIF (Figure 15).

As shown in Figure 15, the lighter point is the top-field interrupt and the darker point is the bottom-field interrupt. It depends on the register configuration, if these interrupt pulses are asserted.

If the CPU uses this interrupt signal not only for the time interval between each video frame but also for the timing to read the stored data from the defined area in SDRAM, note that the CPU has to ignore the first interrupt signal from the VPIF.

Figure 15. Relationship Between the First Interrupt and Incoming Data

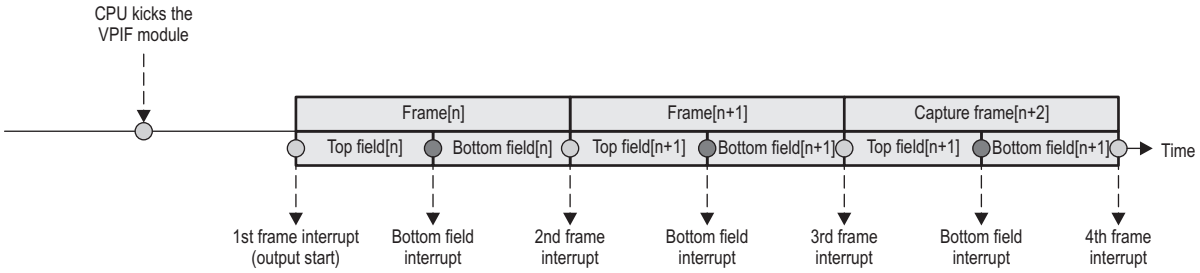


In channels 2 and 3, the VPIF starts to assert displaying picture data after the CPU activates the VPIF with register configuration. The output displaying data is asserted from the VPIF just after the VPIF reads the output data from SDRAM (Figure 16).

So, any redundant data such as the frame[n - 1] area in Figure 15 is not necessary to be prepared. The relationship between the interrupt pulse activation and the register configuration is the same as for capturing data.

If the Figure 16 described relationship with the CPU activates the VPIF and the incoming data and frame[n] start the L11 line for the interlace mode or the L5 line for the progressive mode, the VPIF starts the data store from frame[n+1] not frame[n]. The first frame interrupt happens after frame[n] (at the 2nd frame interrupt in Figure 16), because at the start of the incoming data, there is no first vertical synchronization signal.

Figure 16. Relationship Between the First Interrupt and Outgoing Data



2.9 Power Management

The VPIF can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

The VPIF uses two LPSC domains and you have to set the same state for these two domains. The LPSC controls only when all channels are disabled. If some channels are enabled, the LPSC can not change the VPIF state. You have to disable all channels before powering down using the LPSC.

2.10 Emulation Considerations

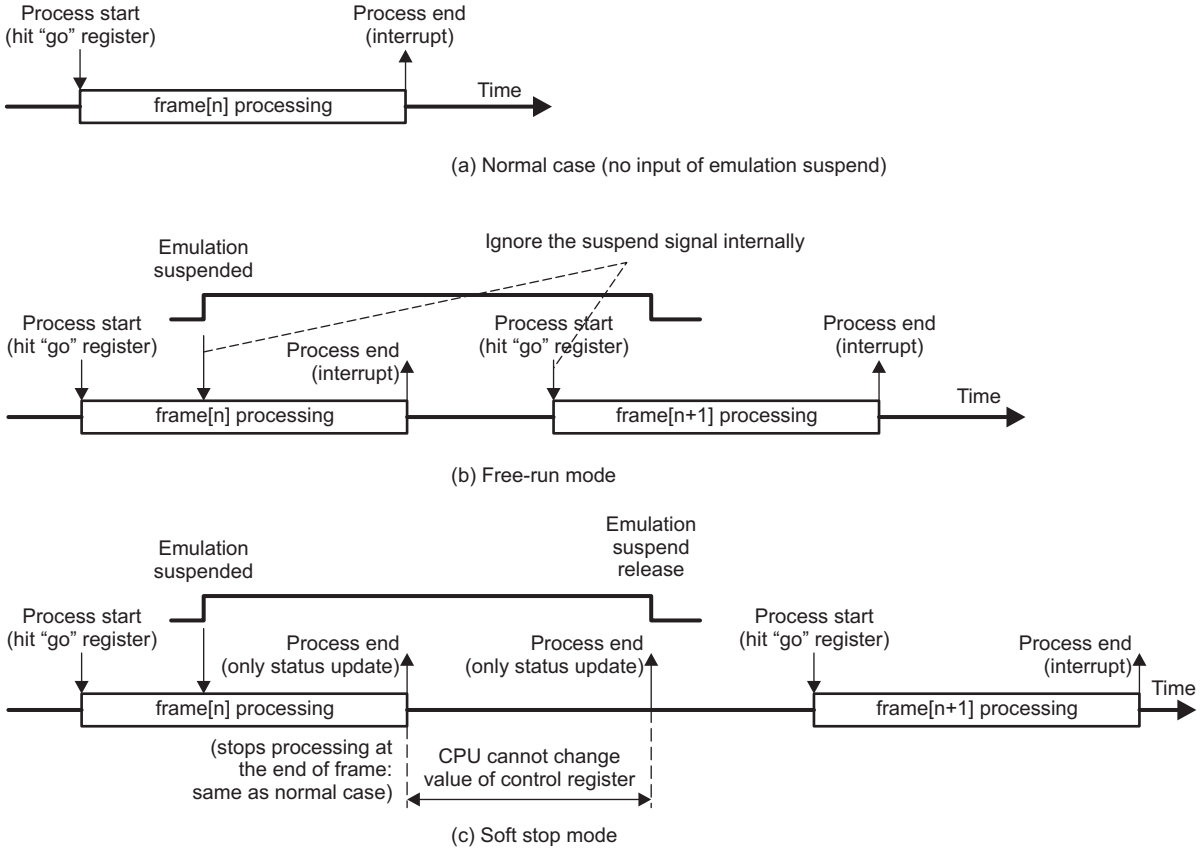
In this section, the CPU is the processor that is selected by the emulation suspend source register (SUSPSRC) in the System Module.

2.10.1 Emulation Suspend Mode Support

The VPIF supports the emulation suspend signal from the CPU. The emulation suspend signal (a high signal indicates that the CPU is suspended) is asserted by the CPU when the CPU is halted with a breakpoint or any other reason during debug.

Functional performance, when the emulation suspend signal is received, is defined by the register configuration and is different for each use (receiver and transmitter). Because the VPIF has to process real-time incoming (or outgoing) data that has a unit size of 1 frame, the VPIF can be stalled at the nearest end of the present processing frame when the emulation suspend signal is received. The fundamental performance of emulation suspend is shown in Figure 17.

Figure 17. Module Performance with Emulation Suspend Signal



2.10.1.1 Receiver (Channels 0 and 1)

The VPIF receives input data from an external video device. The input format is BT.656 or BT.1120 (see Section 2.4.1). If the emulation suspend comes from the CPU during image processing, the VPIF will first try to run at the end of the present frame and then the VPIF will be stalled (see Figure 17 (c)).

The VPIF should have only a software stop mode; the hardware stop mode is not supported. If the CPU changes the register configuration during an emulation suspended period, the new configuration should be validated at the first V-sync after the suspended period.

2.10.1.2 Transmitter (Channels 2 and 3)

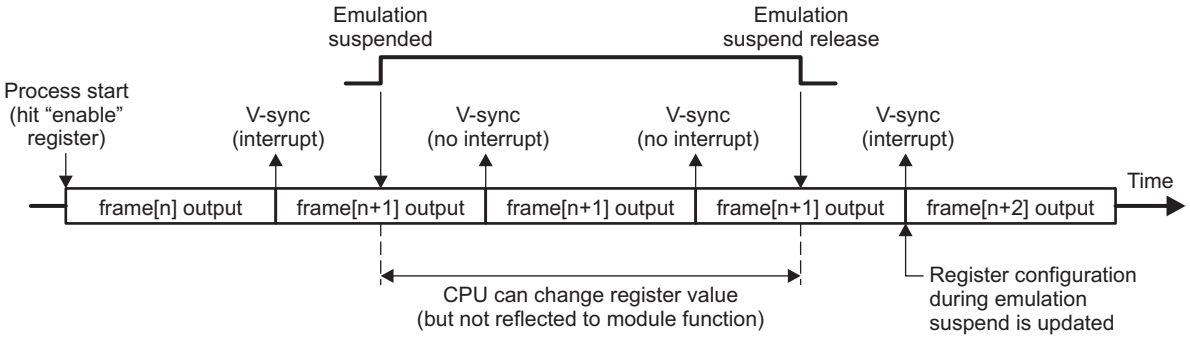
The VPIF transmits output data to an external video device. Source data for this output data is stored in SDRAM. The VPIF needs information about the start address of the source data stored in SDRAM. The output format is BT.656 or BT.1120 (see Section 2.4.1).

In this mode, any suspend function should not be activated because you would like to see a displayed picture, taking usage of this signal into consideration. From a system's stand point, the VPIF should act in the following sequence if the emulation suspend signal is detected:

1. The VPIF continues processing at the end of the present frame.
2. If the present frame is finished, interrupt assertion is stalled.
3. At phase (b), during the active period of the emulation suspend signal, the VPIF continues reading the same frame data from SDRAM (no register change is reflected to module performance during this period).
4. After the CPU returns back to the normal state, the VPIF performs as usual. New register configurations done during an emulation suspend period are reflected in the functional performance at the first V-sync after deassertion of the suspend signal.

If the CPU changes the register configuration during an emulation suspended period, the new configuration should be validated at the first V-sync after the suspended period. Functional performance of this mode is shown in Figure 18.

Figure 18. Emulation Suspend Function on Channels 2 and 3 (Transmit)



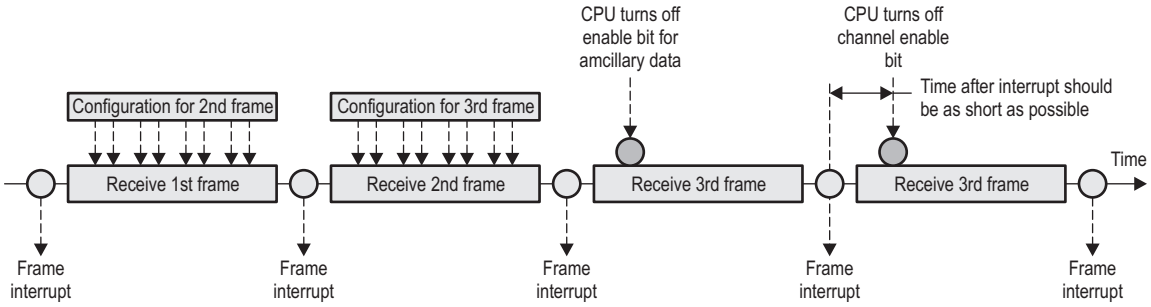
2.11 Rules for Module Control

When you turn off the VPIF, see Figure 19, follow this sequence:

1. If you activate transmitting or capturing ancillary data (both of horizontal and vertical), turn off the enable bit before deactivating a channel of the VPIF.
2. Wait for frame interrupt of the channel.
3. Turn off the channel enable bit of the channel.

The VPIF stops immediately after writing 0 to the CH*n*_EN bit in the channel *n* control register (CH*n*_CTRL). Writing to CH*n*_CTRL takes effect exactly at the same time you write to it, it does not wait to be latched by the VSYNC.

Figure 19. Method for Turning off Module Channel



2.12 PIXEL Enable

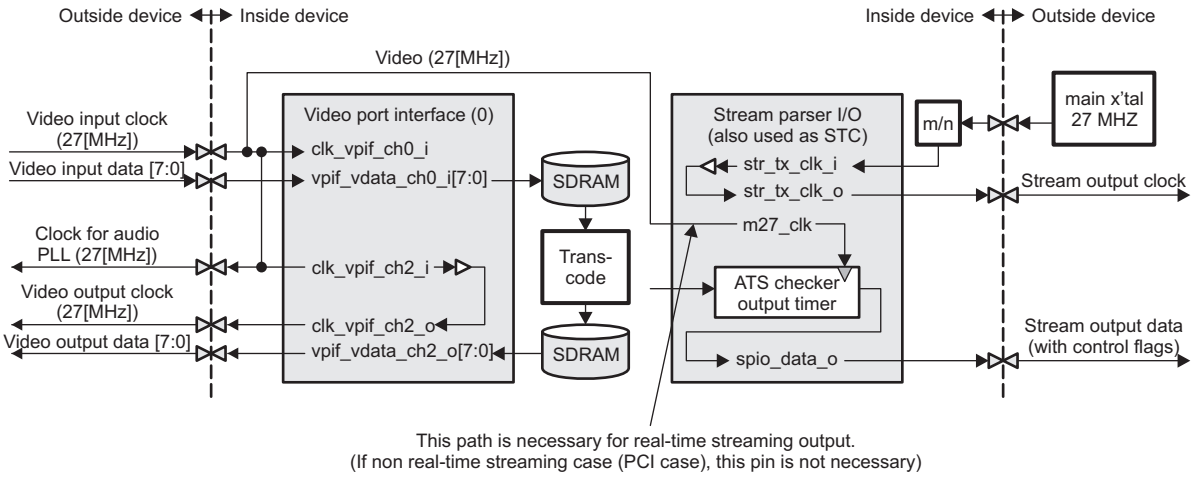
The VPIF channels 2 and 3 pixel enable/disable is controlled by the CH*n*_PIX_EN bit in the channel *n* control register (CH*n*_CTRL). Note that when you enable a pixel while the VPIF is enabled, the output pixel is not correct during reaching the next V-sync and you also receive a FIFO underflow error during that period.

2.13 Operation

2.13.1 BT.656 Mode

See Figure 20. The input clock source of 27 MHz is used for the source clock of the video output. In BT.656 mode, either channel of the input port on the VPIF is used as the actual input of the data. Note that you have to provide the same 27 MHz clock to the transport stream interface (TSIF) module as the video input clock, if you would like to transmit the encoded stream data in real-time; otherwise (for example, using a PCI module that has non real-time interface), you do not have to provide the 27 MHz clock to the TSIF module. Also, you have to provide a 27-MHz output to the external PLL device that provides the audio clock synchronized to the video output clock.

Figure 20. Clock Control on Video Input and Output with SDTV Encoding



2.13.1.1 Parameter Configuration for BT.656 Mode

The configuration for each register in BT.656 mode is shown in Table 6.

Table 6. Register Configuration on BT.656 Input/Output (Unit Size = Byte in unsigned)

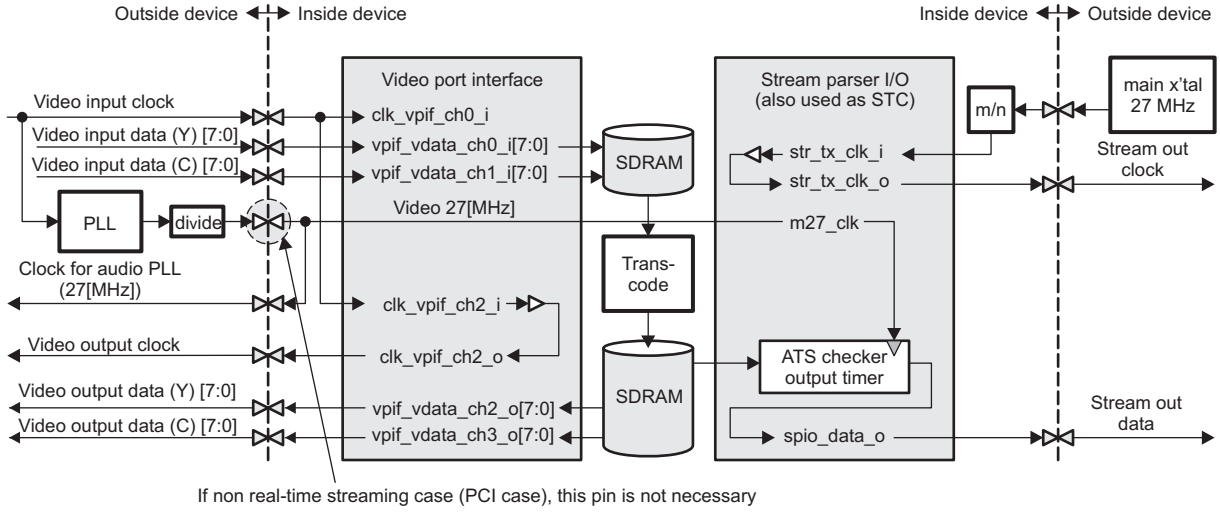
Parameter	Register	Bit Name	NTSC	PAL
EAV2SAV	CH*n*_HSIZE_CFG	CH*n*_EAV2SAV	268	280
SAV2EAV	CH*n*_HSIZE_CFG	CH*n*_SAV2EAV	1440	1440
Vertical frame size	CH*n*_VSIZE	CH*n*_VSZ	525	625
L1	CH*n*_VSIZE_CFG0	CH*n*_L1	4	1
L3	CH*n*_VSIZE_CFG0	CH*n*_L3	20	23
L5	CH*n*_VSIZE_CFG1	CH*n*_L5	264	311
L7	CH*n*_VSIZE_CFG1	CH*n*_L7	266	313
L9	CH*n*_VSIZE_CFG2	CH*n*_L9	283	336
L11	CH*n*_VSIZE_CFG2	CH*n*_L11	1	624

2.13.2 BT.1120 Mode

The BT.1120 mode requires the same clock control for the VPIF as in BT.656 mode. The video input clock (74.25 MHz or 148.5 MHz) is also connected to another VPIF that manages the output image data. The BT.1120 format is necessary to support HDTV input and output for the VPIF. So, two VPIFs are necessary to receive (encode) an input image and to display (local decode) the output image. The functional image and clock control is shown in Figure 21. In this case, VPIF channels 0 and 1 are used for input and VPIF channels 2 and 3 are used for output.

The BT.1120 mode also requires a 27 MHz system clock that is synchronized to the video input clock. To develop the 27 MHz clock, you have to prepare the PLL and divider logic outside the DM646x DMSoC. If you do not need any real-time transmission of the encoded stream data (meaning that you use a non real-time interface module for the encoded stream transmission such as a PCI), you do not have to prepare the PLL and divider logic. Also, you have to provide the 27 MHz (or some other frequency, if an external PLL can receive it) output to another external PLL device that provides an audio clock that is synchronized to the video output clock.

Figure 21. Clock Control on Video Input and Output with HDTV Encoding



2.13.2.1 Parameter Configuration for BT.1120 Mode (1080I60 and 1080I50 system)

The configuration for each register in BT.1120 mode (1080I60 and 1080I50 system) is shown in Table 7.

Table 7. Register Configuration on BT.1120 (1080I60 and 1080I50 System) Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	1080I60	1080I50
EAV2SAV	CH*n*_HSIZE_CFG	CH*n*_EAV2SAV	272	376
SAV2EAV	CH*n*_HSIZE_CFG	CH*n*_SAV2EAV	1920	1920
Vertical frame size	CH*n*_VSIZE	CH*n*_VSZ	1125	1250
L1	CH*n*_VSIZE_CFG0	CH*n*_L1	1	1
L3	CH*n*_VSIZE_CFG0	CH*n*_L3	41	45
L5	CH*n*_VSIZE_CFG1	CH*n*_L5	558	621
L7	CH*n*_VSIZE_CFG1	CH*n*_L7	564	626
L9	CH*n*_VSIZE_CFG2	CH*n*_L9	603	670
L11	CH*n*_VSIZE_CFG2	CH*n*_L11	1121	1246

2.13.2.2 Parameter Configuration for BT.1120 Mode (1080P30 and 1080P60 system)

The configuration for each register in BT.1120 mode (1080P30 and 1080P60 system) is shown in Table 8. Note that the 1080P60 system is supported on 150 MHz VPIF devices only.

Table 8. Register Configuration on BT.1120 (1080P30 and 1080P60 System) Input/Output (Unit Size = Byte in unsigned)

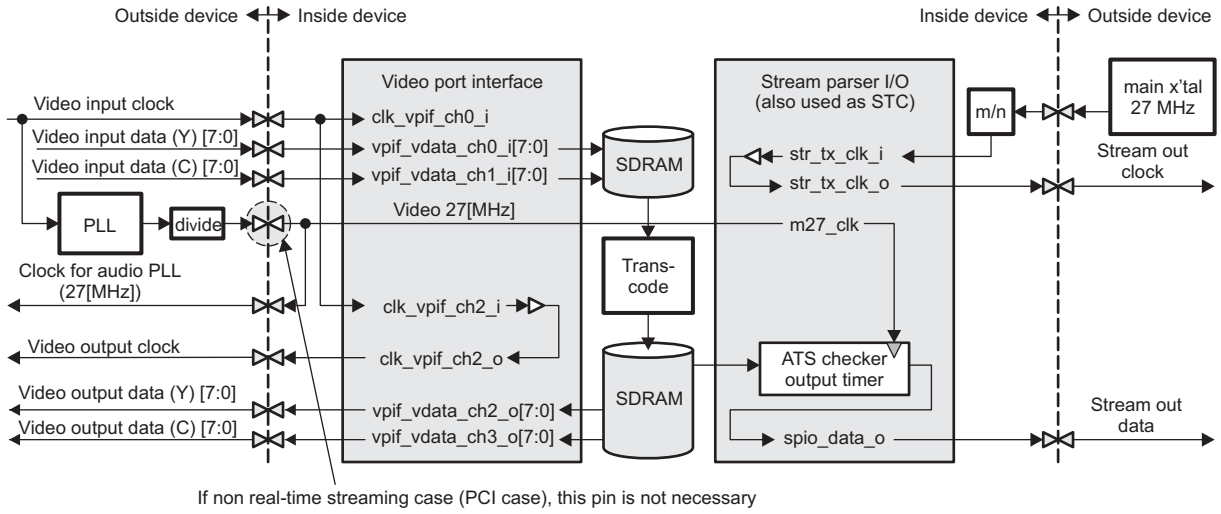
Parameter	Register	Bit Name	Value
EAV2SAV	CH*n*_HSIZE_CFG	CH*n*_EAV2SAV	272
SAV2EAV	CH*n*_HSIZE_CFG	CH*n*_SAV2EAV	1920
Vertical frame size	CH*n*_VSIZE	CH*n*_VSZ	1125
L1	CH*n*_VSIZE_CFG0	CH*n*_L1	1
L3	CH*n*_VSIZE_CFG0	CH*n*_L3	42
L5	CH*n*_VSIZE_CFG1	CH*n*_L5	1122

2.13.3 SMPTE 296M Mode

The SMPTE 296M mode requires the same clock control for the VPIF module as in BT.656 and BT.1120 modes. The video input clock (74.25 MHz) is also connected to another VPIF that manages the output image data. The SMPTE 296M format is necessary to support HDTV input and output for the VPIF. So, two VPIFs are necessary to receive (encode) an input image and to display (local decode) the output image. The functional image and clock control is shown in Figure 22. In this case, VPIF channels 0 and 1 are used for input and VPIF channels 2 and 3 are used for output.

The SMPTE 296M mode also requires a 27 MHz system clock that is synchronized to the video input clock. To develop the 27 MHz clock, you have to prepare the PLL and divider logic outside the DM646x DMSoC. If you do not need any real-time transmission of the encoded stream data (meaning that you use a non real-time interface module for the encoded stream transmission such as a PCI), you do not have to prepare the PLL and divider logic. Also, you have to provide the 27 MHz (or some other frequency, if an external PLL can receive it) output to another external PLL device that provides an audio clock that is synchronized to the video output clock.

Figure 22. Clock Control on Video Input and Output with HDTV Encoding



2.13.3.1 Parameter Configuration for SMPTE 296M Mode

The configuration for each register in SMPTE 296M mode is shown in Table 9.

Table 9. Register Configuration on SMPTE 296M Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	Value
EAV2SAV	CH*n*_HSIZE_CFG	CH*n*_EAV2SAV	362
SAV2EAV	CH*n*_HSIZE_CFG	CH*n*_SAV2EAV	1280
Vertical frame size	CH*n*_VSIZE	CH*n*_VSZ	750
L1	CH*n*_VSIZE_CFG0	CH*n*_L1	1
L3	CH*n*_VSIZE_CFG0	CH*n*_L3	26
L5	CH*n*_VSIZE_CFG1	CH*n*_L5	746

2.13.4 Raw Capture Mode

The raw capture mode requires the same input clock for VPIF channel 0 and channel 1 (clock skew has to be aligned). There are 2 options for this requirement:

- connect the same clock signal to the VP_CLKIN0 and VP_CLKIN1 pins
- use the video clock control register (VIDCLKCTL) in the System Module (see Figure 23 and Table 10). You can use the VP_CLKIN0 pin for the VPIF channel 1 clock.

Figure 23. Video Clock Control Register (VIDCLKCTL)

31															16
Reserved															

15	14 12	11	10 8	7 5	4	3 0
Rsvd	VCH3CLK	Rsvd	VCH2CLK	Reserved	VCH1CLK	Reserved

Table 10. Video Clock Control Register (VIDCLKCTL) Field Descriptions

Bit	Field	Value	Description
4	VCH1CLK		Video channel 1 clock source. Selects the clock source for the channel 1 input clock.
		0	VP_CLKIN0 (external pin)
		1	VP_CLKIN1 (external pin)

2.13.4.1 Parameter Configuration for Raw Capture Mode

When the VPIF sets the raw capture mode, the VPIF recognizes the image size automatically using the H/V valid signals. You do not need to configure the image size in the following registers:

- channel *n* horizontal data size configuration register (CH*n*_HSIZE_CFG)
- channel *n* vertical data size configuration 0 register (CH*n*_VSIZE_CFG0)
- channel *n* vertical data size configuration 1 register (CH*n*_VSIZE_CFG1)
- channel *n* vertical image size register (CH*n*_VSIZE)

However, you still need to configure the SDRAM address control related registers.

2.14 Burst Size Between VPIF Module and SDRAM Control

You can control the burst size for DMA transfers between the VPIF module and the SDRAM using the DMA size control register (DMA_SIZE). This register adjusts transfer traffic with other modules.

3 Registers

All register values should be configured before you set the CH*n*_EN bit in the channel *n* control register (CH*n*_CTRL) to 1. Also note that all register values except the CH*n*_EN bit in CH*n*_CTRL are detected by the first falling edge of the vertical synchronization signal on each channel as shown in Figure 24.

Table 11 lists the memory-mapped registers for the video port interface (VPIF). See the device-specific data manual for the memory address of these registers.

Figure 24. Relationship Between Register and Data Access

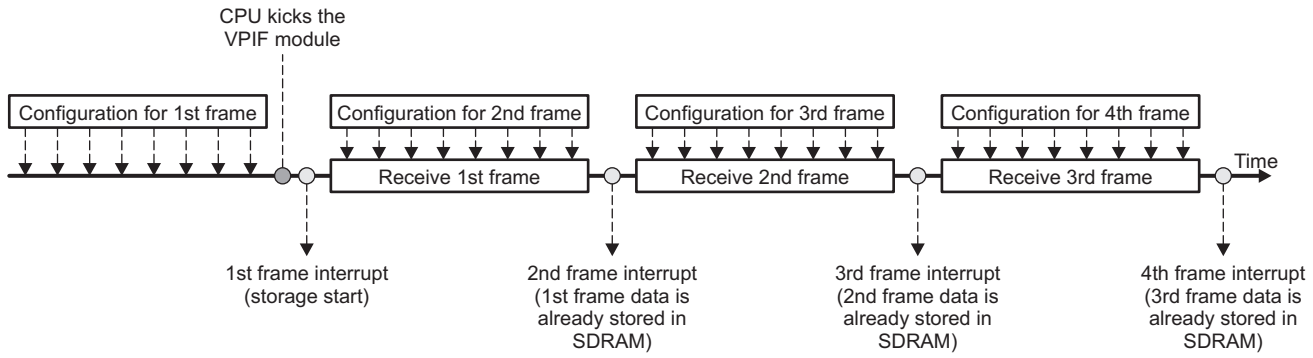


Table 11. Video Port Interface (VPIF) Registers

Offset	Acronym	Register Description	Section
0h	PID	VPIF peripheral identification register	Section 3.1
4h	CH0_CTRL	Channel 0 control register	Section 3.2
8h	CH1_CTRL	Channel 1 control register	Section 3.3
Ch	CH2_CTRL	Channel 2 control register	Section 3.4
10h	CH3_CTRL	Channel 3 control register	Section 3.5
20h	INTEN	Interrupt enable register	Section 3.6
24h	INTENSET	Interrupt enable set register	Section 3.7
28h	INTENCLR	Interrupt enable clear register	Section 3.8
2Ch	INTSTAT	Interrupt status register	Section 3.9
30h	INTSTATCLR	Interrupt status clear register	Section 3.10
34h	EMU_CTRL	Emulation suspend control register	Section 3.11
38h	DMA_SIZE	DMA size control register	Section 3.12
		Channel 0	
40h	CH0_TY_STRTADR	Channel 0 top field luminance buffer start address register	Section 3.13
44h	CH0_BY_STRTADR	Channel 0 bottom field luminance buffer start address register	Section 3.14
48h	CH0_TC_STRTADR	Channel 0 top field chrominance buffer start address register	Section 3.15
4Ch	CH0_BC_STRTADR	Channel 0 bottom field chrominance buffer start address register	Section 3.16
50h	CH0_THA_STRTADR	Channel 0 top field horizontal ancillary data buffer start address register	Section 3.17
54h	CH0_BHA_STRTADR	Channel 0 bottom field horizontal ancillary data buffer start address register	Section 3.18
58h	CH0_TVA_STRTADR	Channel 0 top field vertical ancillary data buffer start address register	Section 3.19
5Ch	CH0_BVA_STRTADR	Channel 0 bottom field vertical ancillary data buffer start address register	Section 3.20
60h	CH0_SUBPIC_CFG	Channel 0 sub-picture configuration register	Section 3.21
64h	CH0_IMG_ADD_OFST	Channel 0 image data address offset register	Section 3.22

Table 11. Video Port Interface (VPIF) Registers (continued)

Offset	Acronym	Register Description	Section
68h	CH0_HA_ADD_OFST	Channel 0 horizontal ancillary data address offset register	Section 3.23
6Ch	CH0_HSIZE_CFG	Channel 0 horizontal data size configuration register	Section 3.24
70h	CH0_VSIZE_CFG0	Channel 0 vertical data size configuration 0 register	Section 3.25
74h	CH0_VSIZE_CFG1	Channel 0 vertical data size configuration 1 register	Section 3.26
78h	CH0_VSIZE_CFG2	Channel 0 vertical data size configuration 2 register	Section 3.27
7Ch	CH0_VSIZE	Channel 0 vertical image size register	Section 3.28
		Channel 1	
80h	CH1_TY_STRTADR	Channel 1 top field luminance buffer start address register	Section 3.13
84h	CH1_BY_STRTADR	Channel 1 bottom field luminance buffer start address register	Section 3.14
88h	CH1_TC_STRTADR	Channel 1 top field chrominance buffer start address register	Section 3.15
8Ch	CH1_BC_STRTADR	Channel 1 bottom field chrominance buffer start address register	Section 3.16
90h	CH1_THA_STRTADR	Channel 1 top field horizontal ancillary data buffer start address register	Section 3.17
94h	CH1_BHA_STRTADR	Channel 1 bottom field horizontal ancillary data buffer start address register	Section 3.18
98h	CH1_TVA_STRTADR	Channel 1 top field vertical ancillary data buffer start address register	Section 3.19
9Ch	CH1_BVA_STRTADR	Channel 1 bottom field vertical ancillary data buffer start address register	Section 3.20
A0h	CH1_SUBPIC_CFG	Channel 1 sub-picture configuration register	Section 3.21
A4h	CH1_IMG_ADD_OFST	Channel 1 image data address offset register	Section 3.22
A8h	CH1_HA_ADD_OFST	Channel 1 horizontal ancillary data address offset register	Section 3.23
ACh	CH1_HSIZE_CFG	Channel 1 horizontal data size configuration register	Section 3.24
B0h	CH1_VSIZE_CFG0	Channel 1 vertical data size configuration 0 register	Section 3.25
B4h	CH1_VSIZE_CFG1	Channel 1 vertical data size configuration 1 register	Section 3.26
B8h	CH1_VSIZE_CFG2	Channel 1 vertical data size configuration 2 register	Section 3.27
BCh	CH1_VSIZE	Channel 1 vertical image size register	Section 3.28
		Channel 2	
C0h	CH2_TY_STRTADR	Channel 2 top field luminance buffer start address register	Section 3.29
C4h	CH2_BY_STRTADR	Channel 2 bottom field luminance buffer start address register	Section 3.30
C8h	CH2_TC_STRTADR	Channel 2 top field chrominance buffer start address register	Section 3.31
CCh	CH2_BC_STRTADR	Channel 2 bottom field chrominance buffer start address register	Section 3.32
D0h	CH2_THA_STRTADR	Channel 2 top field horizontal ancillary data buffer start address register	Section 3.33
D4h	CH2_BHA_STRTADR	Channel 2 bottom field horizontal ancillary data buffer start address register	Section 3.34
D8h	CH2_TVA_STRTADR	Channel 2 top field vertical ancillary data buffer start address register	Section 3.35
DCh	CH2_BVA_STRTADR	Channel 2 bottom field vertical ancillary data buffer start address register	Section 3.36
E0h	CH2_SUBPIC_CFG	Channel 2 sub-picture configuration register	Section 3.37
E4h	CH2_IMG_ADD_OFST	Channel 2 image data address offset register	Section 3.38
E8h	CH2_HA_ADD_OFST	Channel 2 horizontal ancillary data address offset register	Section 3.39
ECh	CH2_HSIZE_CFG	Channel 2 horizontal data size configuration register	Section 3.40
F0h	CH2_VSIZE_CFG0	Channel 2 vertical data size configuration 0 register	Section 3.41
F4h	CH2_VSIZE_CFG1	Channel 2 vertical data size configuration 1 register	Section 3.42
F8h	CH2_VSIZE_CFG2	Channel 2 vertical data size configuration 2 register	Section 3.43

Table 11. Video Port Interface (VPIF) Registers (continued)

Offset	Acronym	Register Description	Section
FCh	CH2_VSIZE	Channel 2 vertical image size register	Section 3.44
100h	CH2_THA_STRTPOS	Channel 2 top field horizontal ancillary data insertion start position register	Section 3.45
104h	CH2_THA_SIZE	Channel 2 top field horizontal ancillary data size register	Section 3.46
108h	CH2_BHA_STRTPOS	Channel 2 bottom field horizontal ancillary data insertion start position register	Section 3.47
10Ch	CH2_BHA_SIZE	Channel 2 bottom field horizontal ancillary data size register	Section 3.48
110h	CH2_TVA_STRTPOS	Channel 2 top field vertical ancillary data insertion start position register	Section 3.49
114h	CH2_TVA_SIZE	Channel 2 top field vertical ancillary data size register	Section 3.50
118h	CH2_BVA_STRTPOS	Channel 2 bottom field vertical ancillary data insertion start position register	Section 3.51
11Ch	CH2_BVA_SIZE	Channel 2 bottom field vertical ancillary data size register	Section 3.52
		Channel 3	
140h	CH3_TY_STRTADR	Channel 3 top field luminance buffer start address register	Section 3.29
144h	CH3_BY_STRTADR	Channel 3 bottom field luminance buffer start address register	Section 3.30
148h	CH3_TC_STRTADR	Channel 3 top field chrominance buffer start address register	Section 3.31
14Ch	CH3_BC_STRTADR	Channel 3 bottom field chrominance buffer start address register	Section 3.32
150h	CH3_THA_STRTADR	Channel 3 top field horizontal ancillary data buffer start address register	Section 3.33
154h	CH3_BHA_STRTADR	Channel 3 bottom field horizontal ancillary data buffer start address register	Section 3.34
158h	CH3_TVA_STRTADR	Channel 3 top field vertical ancillary data buffer start address register	Section 3.35
15Ch	CH3_BVA_STRTADR	Channel 3 bottom field vertical ancillary data buffer start address register	Section 3.36
160h	CH3_SUBPIC_CFG	Channel 3 sub-picture configuration register	Section 3.37
164h	CH3_IMG_ADD_OFST	Channel 3 image data address offset register	Section 3.38
168h	CH3_HA_ADD_OFST	Channel 3 horizontal ancillary data address offset register	Section 3.39
16Ch	CH3_HSIZE_CFG	Channel 3 horizontal data size configuration register	Section 3.40
170h	CH3_VSIZE_CFG0	Channel 3 vertical data size configuration 0 register	Section 3.41
174h	CH3_VSIZE_CFG1	Channel 3 vertical data size configuration 1 register	Section 3.42
178h	CH3_VSIZE_CFG2	Channel 3 vertical data size configuration 2 register	Section 3.43
17Ch	CH3_VSIZE	Channel 3 vertical image size register	Section 3.44
180h	CH3_THA_STRTPOS	Channel 3 top field horizontal ancillary data insertion start position register	Section 3.45
184h	CH3_THA_SIZE	Channel 3 top field horizontal ancillary data size register	Section 3.46
188h	CH3_BHA_STRTPOS	Channel 3 bottom field horizontal ancillary data insertion start position register	Section 3.47
18Ch	CH3_BHA_SIZE	Channel 3 bottom field horizontal ancillary data size register	Section 3.48
190h	CH3_TVA_STRTPOS	Channel 3 top field vertical ancillary data insertion start position register	Section 3.49
194h	CH3_TVA_SIZE	Channel 3 top field vertical ancillary data size register	Section 3.50
198h	CH3_BVA_STRTPOS	Channel 3 bottom field vertical ancillary data insertion start position register	Section 3.51
19Ch	CH3_BVA_SIZE	Channel 3 bottom field vertical ancillary data size register	Section 3.52

3.1 VPIF Peripheral Identification Register (PID)

The VPIF peripheral identification register (PID) is shown in Figure 25 and described in Table 12.

Figure 25. VPIF Peripheral Identification Register (PID)

31	30	29	28	27	16
SCHEME		Reserved		FUNC	
R-1		R-0		R-C08h	

15	11	10	8	7	6	5	0
RTL		MAJOR		CUSTOM		MINOR	
R-0		R-0		R-0		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 12. VPIF Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	0-3h	Used to distinguish between old scheme and current.
29-28	Reserved	0	Reserved
27-16	FUNC	0-FFFh	Function indicates the software-compatible module family.
15-11	RTL	0-1Fh	Indicates RTL version.
10-8	MAJOR	0-7h	Major revision number.
7-6	CUSTOM	0-3h	Indicates a special version for a particular device.
5-0	MINOR	0-3Fh	Minor revision number.

3.2 Channel 0 Control Register (CH0_CTRL)

The channel 0 control register (CH0_CTRL) is shown in Figure 26 and described in Table 13.

Figure 26. Channel 0 Control Register (CH0_CTRL)

31	30	29	28	27	16
CLK_EDGE_CTRL_CH0	Rsvd	DATA_BIT_WIDTH(1)		INTERVAL_LINE_INT(1)	
R/W-0	R-0	R/W-0		R/W-0	

15	14	13	12	11	10	9	8
FID_POL(1)	V_VALID_POL(1)	H_VALID_POL(1)	INPUT_FIELD _OR_FRAME	Reserved	CH0_NIP	CH0_VANC_EN	CH0_HANC_EN
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CH0_INT_CTRL		CH0_FID	CH0_SDR_FMT	CH0_YC_MUX	CH0_FORMAT		CH0_EN
R/W-0		R-0	R/W-0	R/W-0	R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) This bit is activated only when the CH0_FORMAT bit is 2h or 3h; otherwise, this bit is ignored.

Table 13. Channel 0 Control Register (CH0_CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLK_EDGE_CTRL_CH0		Clock edge control. Defines timing relationship between data phase and clock edge for video input data that is connected to VPIF channel 0 (at the device pin level). Edge control is carried out outside the VPIF (just register signal is only asserted from the VPIF).
		0	Data phase is changed at rising edge of the input clock.
		1	Data phase is changed at falling edge of the input clock.
30	Reserved	0	Reserved
29-28	DATA_BIT_WIDTH	0-3h	Data bit width.
		0	8 bits/pixel
		1h	10 bits/pixel
		2h	12 bits/pixel
		3h	Reserved
27-16	INTERVAL_LINE_INT	0-FFFh	Line interrupt interval. If the interrupt register bit of this interrupt is activated, the interrupt signal is asserted to the CPU at the end of each interval lines. This interrupt signal is controlled by the interrupt enable register (INTEN). A value 0 is invalid.
15	FID_POL		Field ID polarity inverting control bit. If the polarity of the incoming field ID signal is inverted to the VPIF, you have to interpret the incoming signal value into the desired polarity.
		0	No inversion.
		1	Invert incoming field ID signal inside the VPIF.
14	V_VALID_POL		Vertical pixel valid signal polarity control. If the polarity of the incoming vertical pixel valid signal is inverted to the VPIF, you have to interpret the incoming signal value into desired polarity.
		0	No inversion.
		1	Invert incoming vertical pixel valid signal inside the VPIF.
13	H_VALID_POL		Horizontal pixel valid signal polarity control. If the polarity of the incoming horizontal pixel valid signal is inverted to the VPIF, you have to interpret the incoming signal value into desired polarity.
		0	No inversion.
		1	Invert incoming horizontal pixel valid signal inside the VPIF.
12	INPUT_FIELD_OR_FRAME		SDRAM storage mode of input picture. Note that this bit is effective only when the CH0_NIP bit is 0 (interlaced), and only in sub-picture mode. In progressive mode, only the frame-based storage method is supported.
		0	Field-based storage
		1	Frame-based storage
11	Reserved	0	Reserved
10	CH0_NIP		Output display format.
		0	Interlaced
		1	Progressive
9	CH0_VANC_EN		Channel 0 vertical ancillary data enable. If you would like to detect vertical ancillary data (VBI; vertical blanking interval) in a BT.656 byte stream, set this bit to 1.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled. The VPIF should store all ancillary data that is inserted in the vertical blanking interval (all data placed between SAV and EAV (horizontal valid pixel period) in vertical blanking area) into SDRAM.
8	CH0_HANC_EN		Channel 0 horizontal ancillary data enable. Controls activation of SDRAM write access when horizontal ancillary data is assigned as incoming data.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled. The VPIF should store all ancillary data that is inserted in the horizontal blanking interval (all data placed between EAV and SAV (horizontal invalid pixel period) in horizontal blanking area) into SDRAM.

Table 13. Channel 0 Control Register (CH0_CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
7-6	CH0_INT_CTRL	0-3h	Channel 0 frame level interrupt to CPU.
		0	Top field V-sync only
		1h	Bottom field V-sync
		2h	Top and bottom field
		3h	Reserved
5	CH0_FID		Channel 0 field identification. This bit allows the CPU to monitor the field ID when an interrupt is asserted from the VPIF to the CPU, due to a reason of channel 0. Only when the interrupt pulse is asserted, this bit will be updated to present field ID. In raw data capturing mode, value of the field ID signal is also reflected in this bit.
		0	Top field
		1	Bottom field
4	CH0_SDR_FMT		SDRAM address format control. Note that this bit is valid only if the VPIF is configured to process HDTV data. Sub-picture mode can be activated for luminance image data. For video ancillary data (in horizontal or vertical blanking interval), the storage format is fixed to be raster scanning format. This bit is effective only when the CH0_FMT bit is 0; otherwise, in raw data capturing mode, this bit has no effect.
		0	Channel 0 raster scanning mode
		1	Channel 0 sub-picture mode
3	CH0_YC_MUX		Channel 0 input data format.
		0	Channel 0 Y/C non-multiplexed mode (either Y or C is in a byte stream). Note that you must set the CH0_EN and the CH1_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start. Also, the CH1_YC_MUX bit is automatically set to 1.
		1	Channel 0 Y/C multiplexed mode (both of Y and C are in a byte stream). Note that in BT. video mode, you can activate each channel independently.
2-1	CH0_FORMAT	0-3h	Channel 0 data mode to be processed.
		0-1h	BT. video (Y/C format) capture mode (sync signal is multiplexed).
		2h-3h	CCD/CMOS data capture mode (sync signal is independently prepared). Note that value on the CH0_FORMAT and the CH1_FORMAT bits should be the same. Also note that you must set the CH0_EN and the CH1_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start.
0	CH0_EN		VPIF channel 0 enable. All register values should be configured before you set this bit. All register configurations are detected by the first falling edge of the vertical synchronization signal when this bit is activated as shown in Figure 24.
		0	Channel 0 is disabled.
		1	Channel 0 is enabled.

3.3 Channel 1 Control Register (CH1_CTRL)

The channel 1 control register (CH1_CTRL) is shown in Figure 27 and described in Table 14.

Figure 27. Channel 1 Control Register (CH1_CTRL)

31	30	16
CLK_EDGE_CTRL_CH1	Reserved	
R/W-0	R-0	

15	11	10	9	8
Reserved		CH1_NIP	CH1_VANC_EN	CH1_HANC_EN
R-0		R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CH1_INT_CTRL		CH1_FID	CH1_SDR_FMT	CH1_YC_MUX	CH1_FORMAT		CH1_EN
R/W-0		R-0	R/W-0	R/W-0	R/W-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Channel 1 Control Register (CH1_CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLK_EDGE_CTRL_CH1		Clock edge control. Defines timing relationship between data phase and clock edge for video input data that is connected to VPIF channel 1 (at the device pin level). Edge control is carried out outside the VPIF (just register signal is only asserted from the VPIF).
		0	Data phase is changed at rising edge of the input clock.
		1	Data phase is changed at falling edge of the input clock.
30-11	Reserved	0	Reserved
10	CH1_NIP		Output display format.
		0	Interlaced
		1	Progressive
9	CH1_VANC_EN		Channel 1 vertical ancillary data enable. If you would like to detect vertical ancillary data (VBI; vertical blanking interval) in a BT.656 byte stream, set this bit to 1.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled. The VPIF should store all ancillary data that is inserted in the vertical blanking interval (all data placed between SAV and EAV (horizontal valid pixel period) in vertical blanking area) into SDRAM.
8	CH1_HANC_EN		Channel 1 horizontal ancillary data enable. Controls activation of SDRAM write access when horizontal ancillary data is assigned as incoming data.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled. The VPIF should store all ancillary data that is inserted in the horizontal blanking interval (all data placed between EAV and SAV (horizontal invalid pixel period) in horizontal blanking area) into SDRAM.
7-6	CH1_INT_CTRL	0-3h	Channel 1 frame level interrupt to CPU.
		0	Top field V-sync only.
		1h	Bottom field V-sync.
		2h	Top and bottom field.
		3h	Reserved
5	CH1_FID		Channel 1 field identification. This bit allows the CPU to monitor the field ID when an interrupt is asserted from the VPIF to the CPU, due to a reason of channel 0. Only when the interrupt pulse is asserted, this bit will be updated to present field ID. In raw data capturing mode, value of the field ID signal is also reflected in this bit.
		0	Top field.
		1	Bottom field.

Table 14. Channel 1 Control Register (CH1_CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
4	CH1_SDR_FMT		SDRAM address format control register. Note that this bit is valid only in the case of processing HDTV (BT.1120) or SDTV (BT.656). And also, this bit is prepared only for luminance image data. For ancillary data, raster scanning mode is fixed to be used.
		0	Channel 1 raster scanning mode.
		1	Channel 1 sub-picture mode.
3	CH1_YC_MUX		Channel 1 input data format.
		0	Channel 1 Y/C non-multiplexed mode (either Y or C is in a byte stream). Note that you must set the CH0_EN and the CH1_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start. Also, the CH0_YC_MUX bit is automatically set to 1.
		1	Channel 1 Y/C multiplexed mode (both of Y and C are in a byte stream). Note that in BT. video mode, you can activate each channel independently.
2-1	CH1_FORMAT	0-3h	Channel 1 data mode to be processed.
		0-1h	BT. video (Y/C format) capture mode (sync signal is multiplexed).
		2h-3h	CCD/CMOS data capture mode (sync signal is independently prepared). Note that value on the CH0_FORMAT and the CH1_FORMAT bits should be the same. Also note that you must set the CH0_EN and the CH1_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start.
0	CH1_EN		VPIF channel 1 enable.
		0	Channel 1 is disabled.
		1	Channel 1 is enabled.

3.4 Channel 2 Control Register (CH2_CTRL)

The channel 2 control register (CH2_CTRL) is shown in Figure 28 and described in Table 15.

Figure 28. Channel 2 Control Register (CH2_CTRL)

31	30						16
CLK_EDGE_CTRL_CH2	Reserved						
R/W-0	R-0						

15	14	13	12	11	10	9	8
Reserved	CLIP_ANC_EN	CLIP_ACTIVE_EN	OUTPUT_FIELD_OR_FRAME	CH2_NIP	CH2_PIX_EN	CH2_VANC_EN	CH2_HANC_EN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CH2_INT_CTRL		CH2_FID	CH2_SDR_FMT	CH2_YC_MUX	Reserved	CH2_CLKEN	CH2_EN
R/W-0		R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 15. Channel 2 Control Register (CH2_CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLK_EDGE_CTRL_CH2		Clock edge control. Defines timing relationship between data phase and clock edge for video input data that is connected to VPIF channel 2 (at the device pin level). Edge control is carried out outside the VPIF (just register signal is only asserted from the VPIF).
		0	Data phase is changed at rising edge of the input clock.
		1	Data phase is changed at falling edge of the input clock.
30-15	Reserved	0	Reserved
14	CLIP_ANC_EN		Activates clipping function of output data in the blanking region for channel 2.
		0	Clipping in the blanking region for channel 2 is disabled.
		1	Clipping in the blanking region for channel 2 is enabled.
13	CLIP_ACTIVE_EN		Activates clipping function of output data in the active region for channel 2.
		0	Clipping in the active region for channel 2 is disabled.
		1	Clipping in the active region for channel 2 is enabled.
12	OUTPUT_FIELD_OR_FRAME		SDRAM storage mode of output picture. Note that this bit is effective only when the CH2_NIP bit is 0 (interlaced), and only in sub-picture mode. In progressive mode, only the frame-based storage method is supported.
		0	Field-based storage
		1	Frame-based storage
11	CH2_NIP		Output display format.
		0	Interlaced
		1	Progressive
10	CH2_PIX_EN		Controls pixel data on area of displaying image data when the CH2_EN bit is activated. If this bit and the CH2_EN bit are activated, image data read from SDRAM is displayed. If this bit is inactivated and the CH2_EN bit is activated, data placed in image area is filled with 10h (luminance) and 80h (chrominance).
		0	Pixel data is disabled (fixed value of 10h (Y) and 80h are displayed).
		1	Pixel data is enabled (image data read from SDRAM is displayed).
9	CH2_VANC_EN		Channel 2 vertical ancillary data enable. If you would like to detect vertical ancillary data (VBI; vertical blanking interval) in a BT.656 byte stream, set this bit to 1.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled. The VPIF should read ancillary data from SDRAM. You should configure start position and size of source ancillary data in both of horizontal and vertical direction, and the VPIF inserts the source data that is read from SDRAM in outgoing byte stream data of BT.656. Other area that is out of configured area to be placed by ancillary data has to be filled with Y = 10h and C = 80h.

Table 15. Channel 2 Control Register (CH2_CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
8	CH2_HANC_EN		Channel 2 horizontal ancillary data enable. Controls SDRAM write access when horizontal ancillary data is assigned as incoming data.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled. The VPIF should read ancillary data from SDRAM. You should configure start position and size of source ancillary data in both of horizontal and vertical direction, and the VPIF inserts the source data that is read from SDRAM in outgoing byte stream data of BT.656. Other area that is out of configured area to be placed by ancillary data has to be filled with Y = 10h and C = 80h.
7-6	CH2_INT_CTRL	0-3h	Channel 2 frame level interrupt to CPU.
		0	Top field V-sync only.
		1h	Bottom field V-sync
		2h	Top and bottom field.
		3h	Reserved
5	CH2_FID		Channel 2 field identification. This bit allows the CPU to monitor the field ID when an interrupt is asserted from the VPIF to the CPU, due to a reason of channel 0. Only when the interrupt pulse is asserted, this bit will be updated to present field ID.
		0	Top field.
		1	Bottom field.
4	CH2_SDR_FMT		SDRAM address format control register. Note that this bit is valid only if the VPIF is configured to process SDTV data. And also, this bit is prepared only for luminance image data. For chrominance image data and ancillary data, raster scanning mode is fixed to be used.
		0	Channel 2 raster scanning mode.
		1	Channel 2 sub-picture mode.
3	CH2_YC_MUX		Channel 2 output data format.
			If Y/C non-multiplexed mode is selected (bit = 0), register configuration for chrominance (such as SDRAM access start address) only is activated.
		0	Channel 2 Y/C non-multiplexed mode (either Y or C is in a byte stream). Note that you must set the CH2_EN and the CH3_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start. Also, the CH3_YC_MUX bit is automatically set to 1.
		1	Channel 2 Y/C multiplexed mode (both of Y and C are in a byte stream). Note that in BT. video mode, you can activate each channel independently.
2	Reserved	0	Reserved
1	CH2_CLKEN		This bit controls the clock enable of VPIF channel 2. Note that this signal is not sampled by V-sync signal; this bit should be configured to 1 before activating this channel, and should be configured to 0 after deactivating this channel.
			Also, this bit value is directly reflected to the value of output signals vdata_ch2_oe_n and clk_ch2_oe_n.
		0	VPIF channel 2 clock is disabled.
		1	VPIF channel 2 clock is enabled.
0	CH2_EN		VPIF channel 2 enable.
		0	Channel 2 is disabled.
		1	Channel 2 is enabled.

3.5 Channel 3 Control Register (CH3_CTRL)

The channel 3 control register (CH3_CTRL) is shown in Figure 29 and described in Table 16.

Figure 29. Channel 3 Control Register (CH3_CTRL)

31	30						16
CLK_EDGE_CTRL_CH3	Reserved						
R/W-0	R-0						

15	14	13	12	11	10	9	8
Reserved	CLIP_ANC_EN	CLIP_ACTIVE_EN	Reserved	CH3_NIP	CH3_PIX_EN	CH3_VANC_EN	CH3_HANC_EN
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CH3_INT_CTRL		CH3_FID	CH3_SDR_FMT	CH3_YC_MUX	Reserved	CH3_CLKEN	CH3_EN
R/W-0		R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. Channel 3 Control Register (CH3_CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLK_EDGE_CTRL_CH3		Clock edge control. Defines timing relationship between data phase and clock edge for video input data that is connected to VPIF channel 3 (at the device pin level). Edge control is carried out outside the VPIF (just register signal is only asserted from the VPIF).
		0	Data phase is changed at rising edge of the input clock.
		1	Data phase is changed at falling edge of the input clock.
30-15	Reserved	0	Reserved
14	CLIP_ANC_EN		Activates clipping function of output data in the blanking region for channel 3.
		0	Clipping in the blanking region for channel 3 is disabled.
		1	Clipping in the blanking region for channel 3 is enabled.
13	CLIP_ACTIVE_EN		Activates clipping function of output data in the active region for channel 3.
		0	Clipping in the active region for channel 3 is disabled.
		1	Clipping in the active region for channel 3 is enabled.
12	Reserved	0	Reserved
11	CH3_NIP		Output display format.
		0	Interlaced
		1	Progressive
10	CH3_PIX_EN		Controls pixel data on area of displaying image data when the CH3_EN bit is activated. If this bit and the CH3_EN bit are activated, image data read from SDRAM is displayed. If this bit is inactivated and the CH3_EN bit is activated, data placed in image area is filled with 10h (luminance) and 80h (chrominance).
		0	Pixel data is disabled (fixed value of 10h (Y) and 80h are displayed).
		1	Pixel data is enabled (image data read from SDRAM is displayed).
9	CH3_VANC_EN		Channel 3 vertical ancillary data enable. If you would like to detect vertical ancillary data (VBI; vertical blanking interval) in a BT.656 byte stream, set this bit to 1.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled. The VPIF should read ancillary data from SDRAM. You should configure start position and size of source ancillary data in both of horizontal and vertical direction, and the VPIF inserts the source data that is read from SDRAM in outgoing byte stream data of BT.656. Other area that is out of configured area to be placed by ancillary data has to be filled with Y = 10h and C = 80h.

Table 16. Channel 3 Control Register (CH3_CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
8	CH3_HANC_EN		Channel 3 horizontal ancillary data enable. Controls activation of SDRAM write access when horizontal ancillary data is assigned as incoming data.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled. The VPIF should read ancillary data from SDRAM. You should configure start position and size of source ancillary data in both of horizontal and vertical direction, and the VPIF inserts the source data that is read from SDRAM in outgoing byte stream data of BT.656. Other area that is out of configured area to be placed by ancillary data has to be filled with Y = 10h and C = 80h.
7-6	CH3_INT_CTRL	0-3h	Channel 3 frame level interrupt to CPU.
		0	Top field V-sync only.
		1h	Bottom field V-sync.
		2h	Top and bottom field.
		3h	Reserved
5	CH3_FID		Channel 3 field identification. This bit allows the CPU to monitor the field ID when an interrupt is asserted from the VPIF to the CPU, due to a reason of channel 0. Only when the interrupt pulse is asserted, this bit will be updated to present field ID.
		0	Top field.
		1	Bottom field.
4	CH3_SDR_FMT		SDRAM address format control register. Note that this bit is valid only if the VPIF is configured to process SDTV data. And also, this bit is prepared only for luminance image data. For chrominance image data and ancillary data, raster scanning mode is fixed to be used.
		0	Channel 3 raster scanning mode.
		1	Channel 3 sub-picture mode.
3	CH3_YC_MUX		Channel 3 output data format.
			If Y/C non-multiplexed mode is selected (bit = 0), register configuration for chrominance (such as SDRAM access start address) only is activated.
		0	Channel 1 Y/C non-multiplexed mode (either Y or C is in a byte stream). Note that you must set the CH2_EN and the CH3_EN bits to 1 in order to activate the VPIF; otherwise, the VPIF does not start. Also, the CH2_YC_MUX bit is automatically set to 1.
		1	Channel 3 Y/C multiplexed mode (both of Y and C are in a byte stream). Note that in BT. video mode, you can activate each channel independently.
2	Reserved	0	Reserved
1	CH3_CLKEN		This bit controls the clock enable of VPIF channel 3. Note that this signal is not sampled by V-sync signal; this bit should be configured to 1 before activating this channel, and should be configured to 0 after deactivating this channel.
			Also, this bit value is directly reflected to the value of output signals vdata_ch3_oe_n and clk_ch3_oe_n.
		0	VPIF channel 3 clock is disabled.
		1	VPIF channel 2 clock is enabled.
0	CH3_EN		VPIF channel 3 enable.
		0	Channel 3 is disabled.
		1	Channel 3 is enabled.

3.6 Interrupt Enable Register (INTEN)

The interrupt enable register (INTEN) is shown in Figure 30 and described in Table 17.

Figure 30. Interrupt Enable Register (INTEN)

31					16
Reserved					
R-0					

15					8
Reserved					
R-0					

7	4	3	2	1	0
Reserved	INTEN _ERROR	INTEN _FRAME_CH3	INTEN _FRAME_CH2	INTEN _FRAME_CH1	INTEN _FRAME_CH0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. Interrupt Enable Register (INTEN) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	INTEN_ERROR		Controls error interrupt (VP_ERRINT) from the VPIF to ARM processor. The interrupt should be asserted if the VPIF detects any error on the input/output byte stream data. To activate asserting this interrupt to ARM, configure this bit to 1, and then configure the INTEN_ERROR_SET bit in INTENSET to 1.
		0	Error interrupt is disabled.
		1	Error interrupt is enabled.
3	INTEN_FRAME_CH3		Channel 3 frame interrupt enable. Controls frame level interrupt (1 pulse per 1 frame) from the VPIF to ARM processor. To activate asserting this interrupt to ARM, configure this bit to 1, and then configure the INTEN_FRAME_CH3_SET bit in INTENSET to 1.
		0	Channel 3 frame interrupt is disabled.
		1	Channel 3 frame interrupt is enabled.
2	INTEN_FRAME_CH2		Channel 2 frame interrupt enable. Controls frame level interrupt (1 pulse per 1 frame) from the VPIF to ARM processor. To activate asserting this interrupt to ARM, configure this bit to 1, and then configure the INTEN_FRAME_CH2_SET bit in INTENSET to 1.
		0	Channel 2 frame interrupt is disabled.
		1	Channel 2 frame interrupt is enabled.
1	INTEN_FRAME_CH1		Channel 1 frame interrupt enable. Controls frame level interrupt (1 pulse per 1 frame) from the VPIF to ARM processor. To activate asserting this interrupt to ARM, configure this bit to 1, and then configure the INTEN_FRAME_CH1_SET bit in INTENSET to 1. In raw capture mode, this bit controls the line-level interrupt enable. It depends on the value of the CH0_FORMAT bit in CH0_CTRL, if CH0_FORMAT = 3h, this bit is prepared for line-level interrupt control, if CH0_FORMAT = 0, this bit is prepared for frame level interrupt.
		0	Channel 1 frame interrupt is disabled.
		1	Channel 1 frame interrupt is enabled.
0	INTEN_FRAME_CH0		Channel 0 frame interrupt enable. Controls frame level interrupt (1 pulse per 1 frame) from the VPIF to ARM processor. To activate asserting this interrupt to ARM, configure this bit to 1, and then configure the INTEN_FRAME_CH0_SET bit in INTENSET to 1.
		0	Channel 0 frame interrupt is disabled.
		1	Channel 0 frame interrupt is enabled.

3.7 Interrupt Enable Set Register (INTENSET)

The interrupt enable set register (INTENSET) is shown in Figure 31 and described in Table 18.

Figure 31. Interrupt Enable Set Register (INTENSET)

31	16
Reserved	
R-0	

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved	INTEN_ERROR_SET	INTEN_FRAME_CH3_SET	INTEN_FRAME_CH2_SET	INTEN_FRAME_CH1_SET	INTEN_FRAME_CH0_SET
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Interrupt Enable Set Register (INTENSET) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	INTEN_ERROR_SET		Error interrupt enable set. To activate the error interrupt, configure the INTEN_ERROR bit in INTEN to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_ERROR bit is activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. If you write 1 to the INTEN_ERROR_CLR bit in INTENCLR during this bit being activated, this bit is internally cleared to 0.
		0	Interrupt on INTEN_ERROR is inactivated (cannot write 0).
		1	Interrupt on INTEN_ERROR is activated.
3	INTEN_FRAME_CH3_SET		Channel 3 frame interrupt enable set. To activate the channel 3 frame interrupt, configure the INTEN_FRAME_CH3 bit in INTEN to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_FRAME_CH3 bit is activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. If you write 1 to the INTEN_FRAME_CH3_CLR bit in INTENCLR during this bit being activated, this bit is internally cleared to 0.
		0	Interrupt on INTEN_FRAME_CH3 is inactivated (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH3 is activated.
2	INTEN_FRAME_CH2_SET		Channel 2 frame interrupt enable set. To activate the channel 2 frame interrupt, configure the INTEN_FRAME_CH2 bit in INTEN to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_FRAME_CH2 bit is activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. If you write 1 to the INTEN_FRAME_CH2_CLR bit in INTENCLR during this bit being activated, this bit is internally cleared to 0.
		0	Interrupt on INTEN_FRAME_CH2 is inactivated (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH2 is activated.

Table 18. Interrupt Enable Set Register (INTENSET) Field Descriptions (continued)

Bit	Field	Value	Description
1	INTEN_FRAME_CH1_SET		Channel 1 frame interrupt enable set. To activate the channel 1 frame interrupt, configure the INTEN_FRAME_CH1 bit in INTEN to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_FRAME_CH1 bit is activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. If you write 1 to the INTEN_FRAME_CH1_CLR bit in INTENCLR during this bit being activated, this bit is internally cleared to 0. In raw capture mode, this bit controls the line-level interrupt enable. It depends on the value of the CH0_FORMAT bit in CH0_CTRL, if CH0_FORMAT = 3h, this bit is prepared for line-level interrupt control, if CH0_FORMAT = 0, this bit is prepared for frame level interrupt.
		0	Interrupt on INTEN_FRAME_CH1 is inactivated (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH1 is activated.
0	INTEN_FRAME_CH0_SET		Channel 0 frame interrupt enable set. To activate the channel 0 frame interrupt, configure the INTEN_FRAME_CH0 bit in INTEN to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_FRAME_CH0 bit is activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. If you write 1 to the INTEN_FRAME_CH0_CLR bit in INTENCLR during this bit being activated, this bit is internally cleared to 0.
		0	Interrupt on INTEN_FRAME_CH0 is inactivated (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH0 is activated.

3.8 Interrupt Enable Clear Register (INTENCLR)

The interrupt enable clear register (INTENCLR) is shown in Figure 32 and described in Table 19.

Figure 32. Interrupt Enable Clear Register (INTENCLR)

31	16
Reserved	
R-0	

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved	INTEN_ERROR_CLR	INTEN_FRAME_CH3_CLR	INTEN_FRAME_CH2_CLR	INTEN_FRAME_CH1_CLR	INTEN_FRAME_CH0_CLR
R-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R = Read only; W = Write only; -*n* = value after reset

Table 19. Interrupt Enable Clear Register (INTENCLR) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	INTEN_ERROR_CLR		Error interrupt enable clear. To inactivate the error interrupt, configure the INTEN_ERROR bit in INTEN and the INTEN_ERROR_SET bit in INTENSET to 1, and then configure this bit to 1. While activated, this bit value remains set to 1. Note that this bit is effective only when the INTEN_ERROR and the INTEN_ERROR_SET bits are activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit.
		0	No change (cannot write 0).
		1	Interrupt on INTEN_ERROR inactivated (cannot be read by ARM).
3	INTEN_FRAME_CH3_CLR		Channel 3 frame interrupt enable clear. To inactivate the channel 3 frame interrupt, configure the INTEN_FRAME_CH3 bit in INTEN and the INTEN_FRAME_CH3_SET bit in INTENSET to 1, and then configure this bit to 1. Note that this bit is effective only when the INTEN_FRAME_CH3 and the INTEN_FRAME_CH3_SET bits are activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit.
		0	No change (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH3 is inactivated (cannot be read by ARM).
2	INTEN_FRAME_CH2_CLR		Channel 2 frame interrupt enable clear. To inactivate the channel 2 frame interrupt, configure the INTEN_FRAME_CH2 bit in INTEN and the INTEN_FRAME_CH2_SET bit in INTENSET to 1, and then configure this bit to 1. Note that this bit is effective only when the INTEN_FRAME_CH2 and the INTEN_FRAME_CH2_SET bits are activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit.
		0	No change (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH2 is inactivated (cannot be read by ARM).
1	INTEN_FRAME_CH1_CLR		Channel 1 frame interrupt enable clear. To inactivate the channel 1 frame interrupt, configure the INTEN_FRAME_CH1 bit in INTEN and the INTEN_FRAME_CH1_SET bit in INTENSET to 1, and then configure this bit to 1. Note that this bit is effective only when the INTEN_FRAME_CH1 and the INTEN_FRAME_CH1_SET bits are activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit. In raw capture mode, this bit controls the line-level interrupt enable. It depends on the value of the CH0_FORMAT bit in CH0_CTRL, if CH0_FORMAT = 3h, this bit is prepared for line-level interrupt control, if CH0_FORMAT = 0, this bit is prepared for frame level interrupt.
		0	No change (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH1 is inactivated (cannot be read by ARM).

Table 19. Interrupt Enable Clear Register (INTENCLR) Field Descriptions (continued)

Bit	Field	Value	Description
0	INTEN_FRAME_CH0_CLR		Channel 0 frame interrupt enable clear. To inactivate the channel 0 frame interrupt, configure the INTEN_FRAME_CH0 bit in INTEN and the INTEN_FRAME_CH0_SET bit in INTENSET to 1, and then configure this bit to 1. Note that this bit is effective only when the INTEN_FRAME_CH0 and the INTEN_FRAME_CH0_SET bits are activated; otherwise, any configured value to this bit is ignored and the bit value remains cleared to 0. You can only write 1 to this bit.
		0	No change (cannot write 0).
		1	Interrupt on INTEN_FRAME_CH0 is inactivated (cannot be read by ARM).

3.9 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 33 and described in Table 20.

Figure 33. Interrupt Status Register (INTSTAT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved			STATUS_ERROR	STATUS_FRAME_CH3	STATUS_FRAME_CH2	STATUS_FRAME_CH1	STATUS_FRAME_CH0
R-0			R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 20. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	STATUS_ERROR		Error interrupt status. This bit is effective even if the INTEN_ERROR bit in INTEN is disabled. Note that this bit is read only. To clear this bit, set the STATUS_CLR_ERROR bit in INTSTATCLR to 1.
		0	Error is not detected.
		1	Error is detected, and not checked yet.
3	STATUS_FRAME_CH3		Channel 3 frame interrupt status. This bit is effective even if the INTEN_FRAME_CH3 bit in INTEN is disabled. Note that this bit is read only. To clear this bit, set the STATUS_CLR_FRAME_CH3 bit in INTSTATCLR to 1.
		0	Frame sync on channel 3 is not detected.
		1	Frame sync on channel 3 is detected, and not checked yet.
2	STATUS_FRAME_CH2		Channel 2 frame interrupt status. This bit is effective even if the INTEN_FRAME_CH2 bit in INTEN is disabled. Note that this bit is read only. To clear this bit, set the STATUS_CLR_FRAME_CH2 bit in INTSTATCLR to 1.
		0	Frame sync on channel 2 is not detected.
		1	Frame sync on channel 2 is detected, and not checked yet.
1	STATUS_FRAME_CH1		Channel 1 frame interrupt status. This bit is effective even if the INTEN_FRAME_CH1 bit in INTEN is disabled. Note that this bit is read only. To clear this bit, set the STATUS_CLR_FRAME_CH1 bit in INTSTATCLR to 1. In raw capture mode, this bit controls the line-level interrupt enable. It depends on the value of the CH0_FORMAT bit in CH0_CTRL, if CH0_FORMAT = 3h, this bit is prepared for line-level interrupt control, if CH0_FORMAT = 0, this bit is prepared for frame level interrupt.
		0	Frame sync on channel 1 is not detected.
		1	Frame sync on channel 1 is detected, and not checked yet.
0	STATUS_FRAME_CH0		Channel 0 frame interrupt status. This bit is effective even if the INTEN_FRAME_CH0 bit in INTEN is disabled. Note that this bit is read only. To clear this bit, set the STATUS_CLR_FRAME_CH0 bit in INTSTATCLR to 1.
		0	Frame sync on channel 0 is not detected.
		1	Frame sync on channel 0 is detected, and not checked yet.

3.10 Interrupt Status Clear Register (INTSTATCLR)

The interrupt status clear register (INTSTATCLR) is shown in Figure 34 and described in Table 21.

Figure 34. Interrupt Status Clear Register (INTSTATCLR)

31					16
Reserved					
R-0					

15					8
Reserved					
R-0					

7	4	3	2	1	0
Reserved	STATUS_CLR_ERROR	STATUS_CLR_FRAME_CH3	STATUS_CLR_FRAME_CH2	STATUS_CLR_FRAME_CH1	STATUS_CLR_FRAME_CH0
R-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R = Read only; W = Write only; -*n* = value after reset

Table 21. Interrupt Status Clear Register (INTSTATCLR) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	STATUS_CLR_ERROR		Error interrupt status clear. To clear the STATUS_ERROR bit in INTSTAT, set this bit to 1. Note that this bit is write-only and the written value cannot be read by the ARM.
		0	No change
		1	STATUS_ERROR bit in INTSTAT is cleared.
3	STATUS_CLR_FRAME_CH3		Channel 3 frame interrupt status clear. To clear the STATUS_FRAME_CH3 bit in INTSTAT, set this bit to 1. Note that this bit is write-only and the written value cannot be read by the ARM.
		0	No change
		1	STATUS_FRAME_CH3 bit in INTSTAT is cleared.
2	STATUS_CLR_FRAME_CH2		Channel 2 frame interrupt status clear. To clear the STATUS_FRAME_CH2 bit in INTSTAT, set this bit to 1. Note that this bit is write-only and the written value cannot be read by the ARM.
		0	No change
		1	STATUS_FRAME_CH2 bit in INTSTAT is cleared.
1	STATUS_CLR_FRAME_CH1		Channel 1 frame interrupt status clear. To clear the STATUS_FRAME_CH1 bit in INTSTAT, set this bit to 1. Note that this bit is write-only and the written value cannot be read by the ARM. In raw capture mode, this bit controls the line-level interrupt enable. It depends on the value of the CH0_FORMAT bit in CH0_CTRL, if CH0_FORMAT = 3h, this bit is prepared for line-level interrupt control, if CH0_FORMAT = 0, this bit is prepared for frame level interrupt.
		0	No change
		1	STATUS_FRAME_CH1 bit in INTSTAT is cleared.
0	STATUS_CLR_FRAME_CH0		Channel 0 frame interrupt status clear. To clear the STATUS_FRAME_CH0 bit in INTSTAT, set this bit to 1. Note that this bit is write-only and the written value cannot be read by the ARM.
		0	No change
		1	STATUS_FRAME_CH0 bit in INTSTAT is cleared.

3.11 Emulation Suspend Control Register (EMU_CTRL)

The emulation suspend control register (EMU_CTRL) is shown in Figure 35 and described in Table 22.

Figure 35. Emulation Suspend Control Register (EMU_CTRL)

31	16
Reserved	
R-0	

15	1	0
Reserved		EMULSUSP_FREE
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

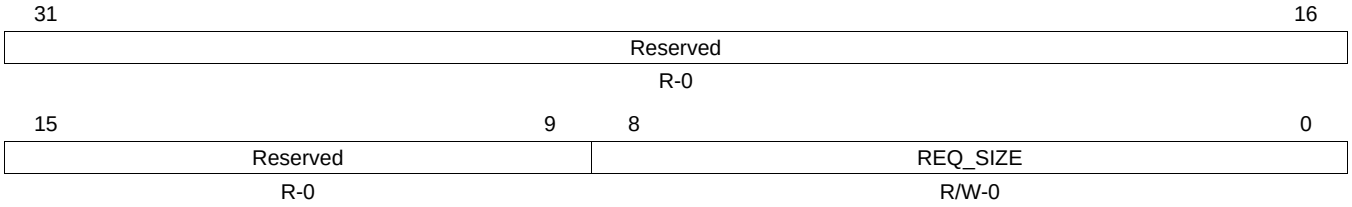
Table 22. Emulation Suspend Control Register (EMU_CTRL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	EMULSUSP_FREE		Controls whether the peripheral responds to the emulation suspend signal that it has been programmed to monitor.
		0	Activating monitoring emulation suspend signal.
		1	Ignores any emulation suspend signal (non-stop).

3.12 DMA Size Control Register (DMA_SIZE)

The DMA size control register (DMA_SIZE) is shown in Figure 36 and described in Table 23.

Figure 36. DMA Size Control Register (DMA_SIZE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23. DMA Size Control Register (DMA_SIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	REQ_SIZE	0-1FF	Defines request unit size for DMA data transfer from/to SDRAM. The VPIF has 64 bits × 64 words ping-pong buffer for each channel and the VPIF asserts the DMA data request to SDRAM in the following case: Mass of stored bytes in the ping-pong buffer reaches configured value. Mass of transmitted bytes from the ping-pong buffer reaches configured value.
		0-1Fh	Reserved
		20h	32 byte. Data size is either luminance or chrominance.
		21h-3Fh	Reserved
		40h	64 byte. Data size is either luminance or chrominance.
		41h-7Fh	Reserved
		80h	128 byte. Data size is either luminance or chrominance.
		81h-1FFh	Reserved

3.13 Channel *n* Top Field Luminance Buffer Start Address Register (CH0_TY_STRTADR and CH1_TY_STRTADR)

The registers in the following description are prepared for SDRAM address configuration where the input and output data is stored. The image of each register is shown in Figure 37 (sub-picture format) and in Figure 38 (raster scanning format).

Figure 37. Image of Storage Format on SDRAM in Sub-Picture Format

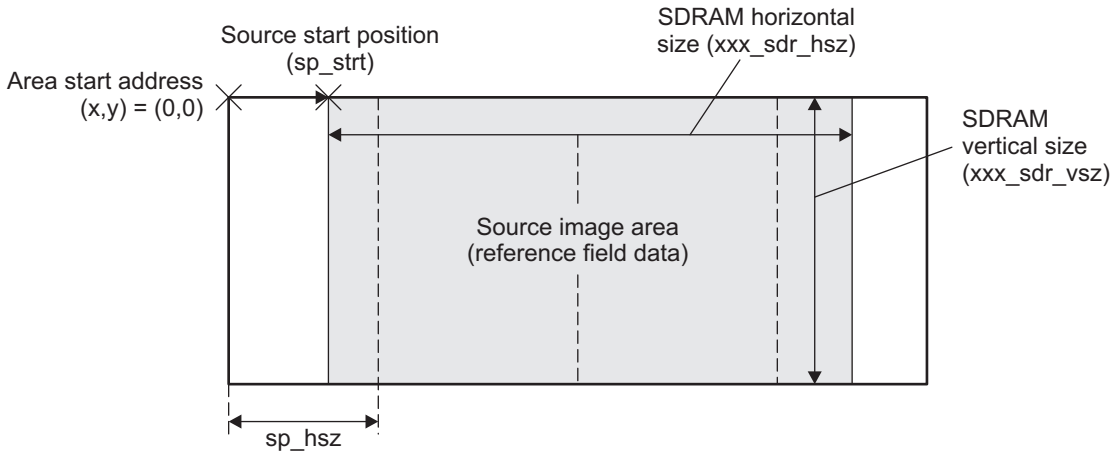
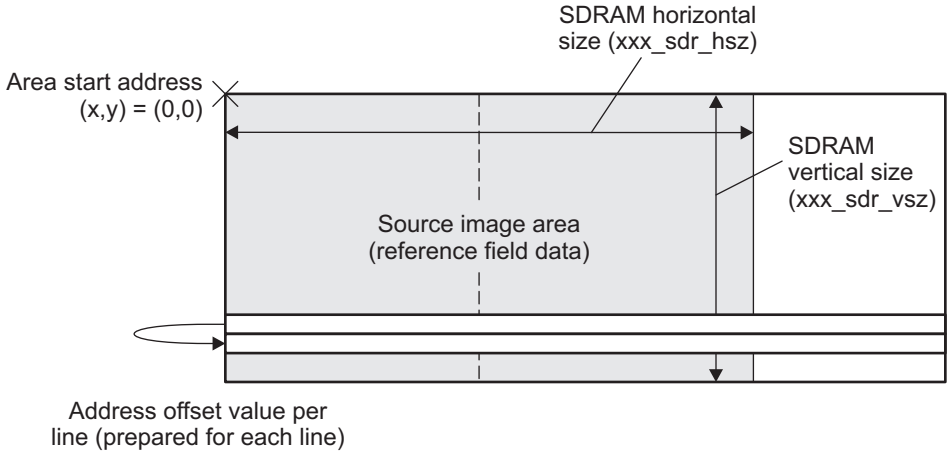


Figure 38. Image of Storage Format on SDRAM in Raster Scanning Format



In sub-picture addressing mode, the source start position is equal to the start position of the active video area (just after the SAV code in the first valid line of the video data in the top/bottom field). This definition is common in both the receiver and transmitter functions of the VPIF.

The CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG) defines the horizontal sub-picture size as shown in Figure 37. The sub-picture size is defined from the following:

- CH*n*_SP_HSZ = 10h (16 byte)
- CH*n*_SP_HSZ = 20h (32 byte)
- CH*n*_SP_HSZ = 40h (64 byte)
- CH*n*_SP_HSZ = 80h (128 byte)
- CH*n*_SP_HSZ = 100h (256 byte)

Taking the fundamental objective of the sub-picture mode into consideration, you have to restrict the value of the area start address to be a multiple of the configured sub-picture size in the sub-picture addressing mode. This means that you have to keep a value of 0 for the following bits of the area start address value:

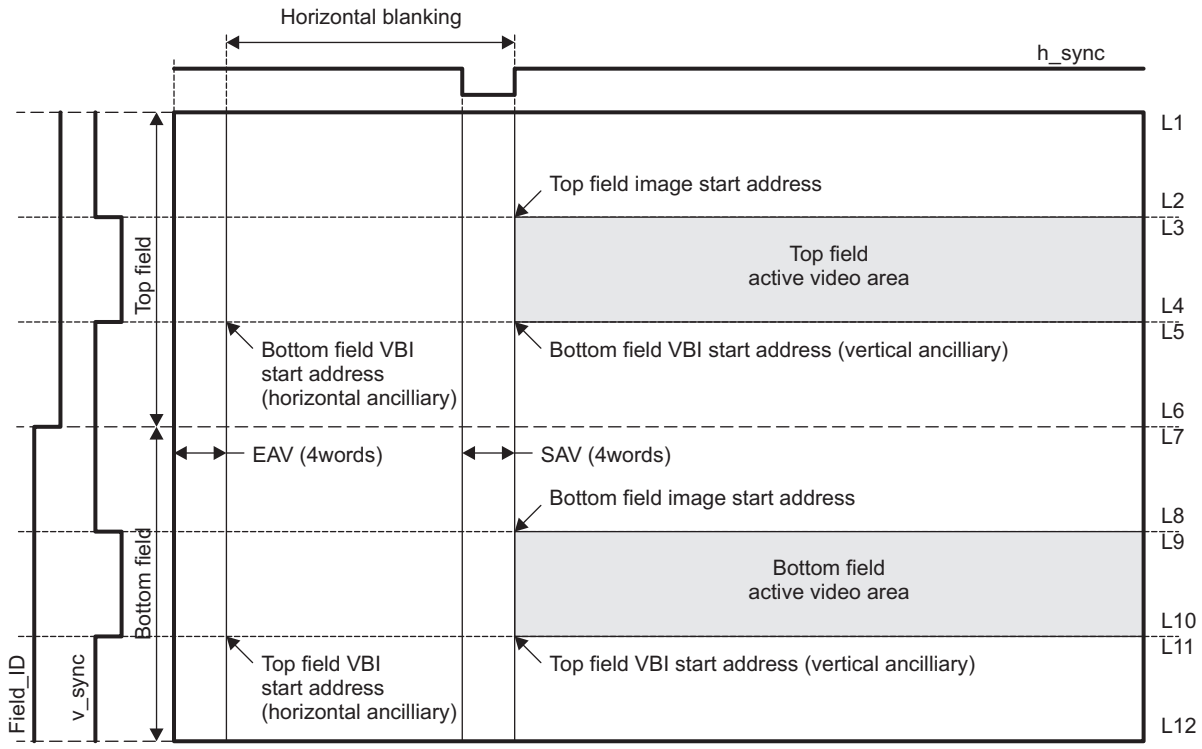
- sub-picture size = 16 bytes: area start address[3:0] = 0000
- sub-picture size = 32 bytes: area start address[4:0] = 00000
- sub-picture size = 64 bytes: area start address[5:0] = 000000
- sub-picture size = 128 bytes: area start address[6:0] = 0000000
- sub-picture size = 256 bytes: area start address[7:0] = 00000000

This rule is effective only in the sub-picture addressing mode.

In raster scanning addressing mode, the area start address is equal to the start position of the active video area (just after the SAV code in the first valid line of the video data in the top/bottom field). This definition is common in both the receiver and transmitter functions of the VPIF when the VPIF processes the video image data in the raster scanning mode. The register value of the area start address must be a multiple of 8.

For VBI data for vertical ancillary data, the area start address is equal to the start position of the active video area (just after the SAV code in the first vertical blanking line on each field), as shown in Figure 39.

Figure 39. Relationship Between SDRAM Start Address and Sync Position



The channel *n* top field luminance buffer start address register (CH*n*_TY_STRTADR) is shown in Figure 40 and described in Table 24.

NOTE: CH1_TY_STRTADR is available in Y/C multiplexed format case in channel 1; otherwise, any configuration on CH1_TY_STRTADR is ignored.

Figure 40. Channel *n* Top Field Luminance Buffer Start Address Register (CH*n*_TY_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_LUMA	
R/W-0	

15	15
CH*n*_TOP_STRT_ADD_LUMA	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 24. Channel *n* Top Field Luminance Buffer Start Address Register (CH*n*_TY_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_LUMA	0-FFFF FFFFh	Configures access start address of SDRAM for luminance data in top field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. This address is used for the SDRAM start address of the top field in raw data capture mode. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.14 Channel *n* Bottom Field Luminance Buffer Start Address Register (CH0_BY_STRTADR and CH1_BY_STRTADR)

The channel *n* bottom field luminance buffer start address register (CH*n*_BY_STRTADR) is shown in Figure 41 and described in Table 25.

NOTE: CH1_BY_STRTADR is available in Y/C multiplexed format case in channel 1; otherwise, any configuration on CH1_BY_STRTADR is ignored.

Figure 41. Channel *n* Bottom Field Luminance Buffer Start Address Register (CH*n*_BY_STRTADR)

31															16
CH*n*_BTM_STRT_ADD_LUMA															
R/W-0															
15															0
CH*n*_BTM_STRT_ADD_LUMA															
R/W-0															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 25. Channel *n* Bottom Field Luminance Buffer Start Address Register (CH*n*_BY_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_LUMA	0-FFFF FFFFh	Configures access start address of SDRAM for luminance data in bottom field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. This address is used for the SDRAM start address of the bottom field in raw data capture mode. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.15 Channel *n* Top Field Chrominance Buffer Start Address Register (CH0_TC_STRTADR and CH1_TC_STRTADR)

The channel *n* top field chrominance buffer start address register (CH*n*_TC_STRTADR) is shown in Figure 42 and described in Table 26.

NOTE: CH0_TC_STRTADR is available in Y/C multiplexed format case in channel 0; otherwise, any configuration on CH0_TC_STRTADR is ignored.

Figure 42. Channel *n* Top Field Chrominance Buffer Start Address Register (CH*n*_TC_STRTADR)

31		16
	CH*n*_TOP_STRT_ADD_CHROMA	
	R/W-0	

15		0
	CH*n*_TOP_STRT_ADD_CHROMA	
	R/W-0	

LEGEND: R = Read only; -*n* = value after reset

Table 26. Channel *n* Top Field Chrominance Buffer Start Address Register (CH*n*_TC_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_CHROMA	0-FFFF FFFFh	Configures access start address of SDRAM for chrominance data in top field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). On raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.16 Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH0_BC_STRTADR and CH1_BC_STRTADR)

The channel *n* bottom field chrominance buffer start address register (CH*n*_BC_STRTADR) is shown in Figure 43 and described in Table 27.

NOTE: CH0_BC_STRTADR is available in Y/C multiplexed format case in channel 0; otherwise, any configuration on CH0_BC_STRTADR is ignored.

Figure 43. Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH*n*_BC_STRTADR)

31		16
	CH*n*_BTM_STRT_ADD_CHROMA	
	R/W-0	

15		0
	CH*n*_BTM_STRT_ADD_CHROMA	
	R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 27. Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH*n*_BC_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_CHROMA	0-FFFF FFFFh	Configures access start address of SDRAM for chrominance data in bottom field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following regulations: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.17 Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH0_THA_STRTADR and CH1_THA_STRTADR)

The channel *n* top field horizontal ancillary data buffer start address register (CH*n*_THA_STRTADR) is shown in Figure 44 and described in Table 28.

Figure 44. Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_THA_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_HANC	
R/W-0	

15	0
CH*n*_TOP_STRT_ADD_HANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 28. Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_THA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_HANC	0-FFFF FFFFh	Configures access start address of SDRAM for horizontal ancillary data in top field on channel *n*. This address is the Area Start address in Figure 38 . The input data starts to be stored into SDRAM from this address. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.18 Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH0_BHA_STRTADR and CH1_BHA_STRTADR)

The channel *n* bottom field horizontal ancillary data buffer start address register (CH*n*_BHA_STRTADR) is shown in Figure 45 and described in Table 29.

Figure 45. Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_BHA_STRTADR)

31	16
CH*n*_BTM_STRT_ADD_HANC	
R/W-0	

15	0
CH*n*_BTM_STRT_ADD_HANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 29. Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_BHA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_HANC	0-FFFF FFFFh	Configures access start address of SDRAM for horizontal ancillary data in bottom field on channel *n*. This address is the Area Start address in Figure 38. The input data starts to be stored into SDRAM from this address. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.19 Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH0_TVA_STRTADR and CH1_TVA_STRTADR)

The channel *n* top field vertical ancillary data buffer start address register (CH*n*_TVA_STRTADR) is shown in Figure 46 and described in Table 30.

Figure 46. Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_TVA_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_VANC	
R/W-0	

15	0
CH*n*_TOP_STRT_ADD_VANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 30. Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_TVA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_VANC	0-FFFF FFFFh	Configures access start address of SDRAM for vertical ancillary data in top field on channel *n*. This address is the Area Start address in Figure 38. The input data starts to be stored into SDRAM from this address. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.20 Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH0_BVA_STRTADR and CH1_BVA_STRTADR)

The channel *n* bottom field vertical ancillary data buffer start address register (CH*n*_BVA_STRTADR) is shown in Figure 47 and described in Table 31.

NOTE: Even in progressive mode, the configured value to CH*n*_BVA_STRTADR is effective.

Figure 47. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_BVA_STRTADR)

31		16
CH*n*_BTM_STRT_ADD_VANC		
R/W-0		

15		0
CH*n*_BTM_STRT_ADD_VANC		
R/W-0		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 31. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_BVA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_VANC	0-FFFF FFFFh	Configures access start address of SDRAM for vertical ancillary data in bottom field on channel *n*. This address is the Area Start address in Figure 38. The input data starts to be stored into SDRAM from this address. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.21 Channel *n* Sub-Picture Configuration Register (CH0_SUBPIC_CFG and CH1_SUBPIC_CFG)

The channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG) is shown in Figure 48 and described in Table 32.

Figure 48. Channel *n* Sub-Picture Configuration Register (CH*n*_SUBPIC_CFG)

31	24	23	16
Reserved		CH*n*_SP_STRT	
R-0		R/W-0	

15	9	8	0
Reserved		CH*n*_SP_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 32. Channel *n* Sub-Picture Configuration Register (CH*n*_SUBPIC_CFG) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	CH*n*_SP_STRT	0-FFh	Configures horizontal start position from which the input image data is stored into SDRAM. The horizontal start position defines the bytes of displacement from the Area Start address (configured in CH*n*_TY_STRTADR, CH*n*_BY_STRTADR, CH*n*_TC_STRTADR, and CH*n*_BC_STRTADR). This value must be less than the horizontal sub-picture size configured in CH*n*_SP_HSZ bit. Also, the configured value should be a multiple of 8.
15-9	Reserved	0	Reserved
8-0	CH*n*_SP_HSZ	0-1FFh	Configures horizontal size of sub-picture for VPIF channel *n* input image data (only for Y/C format) that is used, if you select the sub-picture mode for the storage format of SDRAM. This value is used for channel *n* luminance and chrominance data for both the top and bottom fields. Sub-picture allocation is started from the Area Start address (configured in CH*n*_TY_STRTADR, CH*n*_BY_STRTADR, CH*n*_TC_STRTADR, and CH*n*_BC_STRTADR). Also, the configured value should be a power of 2.
		0-Fh	Reserved
		10h	16 byte
		11h-1Fh	Reserved
		20h	32 byte
		21h-3Fh	Reserved
		40h	64 byte
		41h-7Fh	Reserved
		80h	128 byte
		81h-FFh	Reserved
		100h	256 byte
		101h-1FFh	Reserved

3.22 Channel *n* Image Data Address Offset Register (CH0_IMG_ADD_OFST and CH1_IMG_ADD_OFST)

NOTE: CH0_IMG_ADD_OFST is also used for the line address offset value for stored image data in raw data capture mode.

The channel *n* image data address offset register (CH*n*_IMG_ADD_OFST) is shown in Figure 49 and described in Table 33.

Figure 49. Channel *n* Image Data Address Offset Register (CH*n*_IMG_ADD_OFST)

31	16
CH*n*_IMG_ADD_OFST	
R/W-0	

15	0
CH*n*_IMG_ADD_OFST	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 33. Channel *n* Image Data Address Offset Register (CH*n*_IMG_ADD_OFST) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_IMG_ADD_OFST	0-FFFF FFFFh	Configures address offset value of each line for raster store format in the image data and vertical ancillary data on VPIF channel *n*. Value is given in bytes, note that the 3 LSBs must be 0. Address calculation method on line[x] is written in the following equation: Address = CH*n*_IMG_STRT_ADD + CH*n*_IMG_ADD_OFST × line[x] line[x] = current_line – L3: top field or L9: bottom field Note that this value is valid only if SDRAM storage mode is raster scanning format. In sub-picture mode, this value is ignored. For vertical ancillary data, the address line offset value is automatically calculated by hardware with the configuration of the CH*n*_YC_MUX bit in CH*n*_CTRL. In Y/C mux mode, the actual address offset is CH*n*_IMG_ADD_OFST × 2. In Y/C separate mode, the actual address offset is CH*n*_IMG_ADD_OFST.

3.23 Channel *n* Horizontal Ancillary Data Address Offset Register (CH0_HA_ADD_OFST and CH1_HA_ADD_OFST)

The channel *n* horizontal ancillary data address offset register (CH*n*_HA_ADD_OFST) is shown in Figure 50 and described in Table 34.

Figure 50. Channel *n* Horizontal Ancillary Data Address Offset Register (CH*n*_HA_ADD_OFST)

31	16
CH*n*_HANC_ADD_OFST	
R/W-0	

15	0
CH*n*_HANC_ADD_OFST	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 34. Channel *n* Horizontal Ancillary Data Address Offset Register (CH*n*_HA_ADD_OFST) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_HANC_ADD_OFST	0-FFFF FFFFh	Configures address offset value of each line for raster store format in the horizontal ancillary data on VPIF channel *n*. Value is given in bytes, note that the 3 LSBs must be 0. Address calculation method on line[x] is written in the following equation: Address = CH*n*_HANC_STRT_ADD + CH*n*_HANC_ADD_OFST × line[x] line[x] = current_line – L1: top field or L7: bottom field Note that this value is valid only if SDRAM storage mode is raster scanning format. In sub-picture mode, this value is ignored.

3.24 Channel *n* Horizontal Data Size Configuration Register (CH0_HSIZE_CFG and CH1_HSIZE_CFG)

The register image of the CH*n*_EAV2SAV and CH*n*_SAV2EAV bits in the Y/C data processing mode are shown in Figure 51 and in the CCD/CMOS data processing mode is shown in Figure 52.

In the Y/C data processing mode, the CH*n*_EAV2SAV and CH*n*_SAV2EAV bits do not include the 4-byte code of EAV and SAV. In the CCD/CMOS data processing mode, the CH*n*_EAV2SAV and CH*n*_SAV2EAV bits indicate the blanking interval and the picture area directly because the incoming data does not have any timing reference code representative for SAV and EAV.

The channel *n* horizontal data size configuration register (CH*n*_HSIZE_CFG) is shown in Figure 53 and described in Table 35.

Figure 51. Image of Horizontal Distance in Y/C Mode

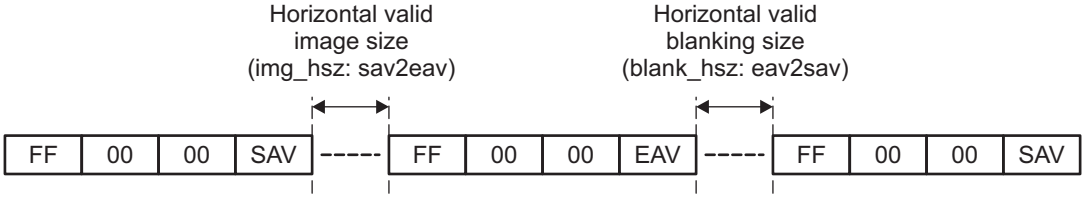


Figure 52. Image of Horizontal Distance in CCD/CMOS Mode

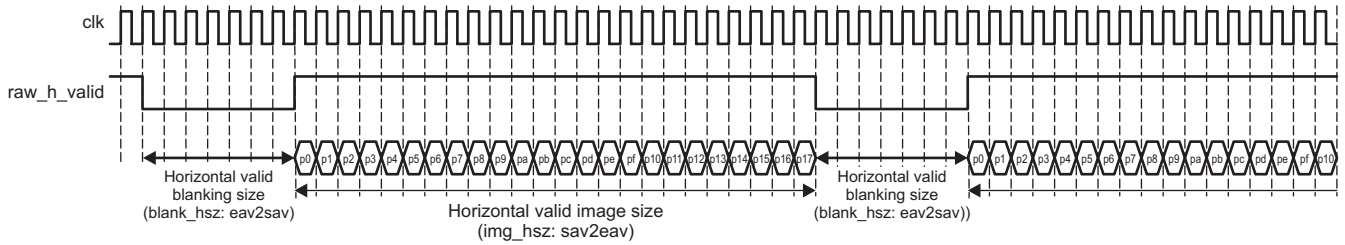


Figure 53. Channel *n* Horizontal Data Size Configuration Register (CH*n*_HSIZE_CFG)

31 29	28 16
Reserved	CH*n*_EAV2SAV
R-0	R/W-0

15 13	12 0
Reserved	CH*n*_SAV2EAV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35. Channel *n* Horizontal Data Size Configuration Register (CH*n*_HSIZE_CFG) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Reserved
28-16	CH*n*_EAV2SAV	0-1FFFh	In Y/C data processing mode (CH*n*_FORMAT bit in CH*n*_CTRL is cleared to 0), indicates the horizontal distance between the EAV code and SAV code on the input data (unit size = byte) for Y/C multiplexed mode and for Y/C demultiplexed mode. See Figure 51. In CCD/CMOS input processing mode (CH*n*_FORMAT bit in CH*n*_CTRL is set to 2h or 3h), indicates the length of the horizontal blanking interval (unit size = byte). See Figure 52. Value should be an even number (bit 16 = 0).
15-13	Reserved	0	Reserved
12-0	CH*n*_SAV2EAV	0-1FFFh	In Y/C data processing mode (CH*n*_FORMAT bit in CH*n*_CTRL is cleared to 0), indicates the horizontal distance between the SAV code and EAV code on the input data (unit size = byte) for Y/C multiplexed mode and for Y/C demultiplexed mode. See Figure 51. In CCD/CMOS input processing mode (CH*n*_FORMAT bit in CH*n*_CTRL is set to 2h or 3h), indicates the horizontal size of the processed picture (unit size = byte). See Figure 52. Value should be an even number (bit 0 = 0).

3.25 Channel *n* Vertical Data Size Configuration 0 Register (CH0_VSIZE_CFG0 and CH1_VSIZE_CFG0)

NOTE: Configured values on the channel *n* vertical data size configuration 0 registers (CH*n*_VSIZE_CFG0) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 0 register (CH*n*_VSIZE_CFG0) is shown in Figure 54 and described in Table 36.

Figure 54. Channel *n* Vertical Data Size Configuration 0 Register (CH*n*_VSIZE_CFG0)

31	28	27	16
Reserved		CH*n*_L1	
R-0		R/W-0	

15	12	11	0
Reserved		CH*n*_L3	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 36. Channel *n* Vertical Data Size Configuration 0 Register (CH*n*_VSIZE_CFG0) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	CH*n*_L1	0-FFFh	Configures L1 position on Figure 39.
15-12	Reserved	0	Reserved
11-0	CH*n*_L3	0-FFFh	Configures L3 position on Figure 39.

3.26 Channel *n* Vertical Data Size Configuration 1 Register (CH0_VSIZE_CFG_1 and CH1_VSIZE_CFG1)

NOTE: Configured values on the channel *n* vertical data size configuration 1 registers (CH*n*_VSIZE_CFG1) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 1 register (CH*n*_VSIZE_CFG1) is shown in Figure 55 and described in Table 37.

Figure 55. Channel *n* Vertical Data Size Configuration 1 Register (CH*n*_VSIZE_CFG1)

31	28	27	16
Reserved		CH*n*_L5	
R-0		R/W-0	

15	12	11	0
Reserved		CH*n*_L7	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 37. Channel *n* Vertical Data Size Configuration 1 Register (CH*n*_VSIZE_CFG1) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	CH*n*_L5	0-FFFh	Configures L5 position on Figure 39.
15-12	Reserved	0	Reserved
11-0	CH*n*_L7	0-FFFh	Configures L7 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.

3.27 Channel *n* Vertical Data Size Configuration 2 Register (CH0_VSIZE_CFG2 and CH1_VSIZE_CFG2)

NOTE: Configured values on the channel *n* vertical data size configuration 2 registers (CH*n*_VSIZE_CFG2) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 2 register (CH*n*_VSIZE_CFG2) is shown in Figure 56 and described in Table 38.

Figure 56. Channel *n* Vertical Data Size Configuration 2 Register (CH*n*_VSIZE_CFG2)

31	28	27	16
Reserved		CH*n*_L9	
R-0		R/W-0	

15	12	11	0
Reserved		CH*n*_L11	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 38. Channel *n* Vertical Data Size Configuration 2 Register (CH*n*_VSIZE_CFG2) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	CH*n*_L9	0-FFFh	Configures L9 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.
15-12	Reserved	0	Reserved
11-0	CH*n*_L11	0-FFFh	Configures L11 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.

3.28 Channel *n* Vertical Image Size Register (CH0_VSIZE and CH1_VSIZE)

The channel *n* vertical image size register (CH*n*_VSIZE) is shown in Figure 57 and described in Table 39.

Figure 57. Channel *n* Vertical Image Size Register (CH*n*_VSIZE)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		CH*n*_VSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 39. Channel *n* Vertical Image Size Register (CH*n*_VSIZE) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	CH*n*_VSZ	0-FFFh	Defines vertical image size of incoming video data in channel *n*. Format of value should be based on frame format.

3.29 Channel *n* Top Field Luminance Buffer Start Address Register (CH2_TY_STRTADR and CH3_TY_STRTADR)

The registers in the following description are prepared for SDRAM address configuration where the input and output data is stored. The image of each register is shown in Figure 37 (sub-picture format) and in Figure 38 (raster scanning format).

The channel *n* top field luminance buffer start address register (CH*n*_TY_STRTADR) is shown in Figure 58 and described in Table 40.

NOTE: CH3_TY_STRTADR is available in Y/C multiplexed format case in channel 3; otherwise, any configuration on CH3_TY_STRTADR is ignored.

Figure 58. Channel *n* Top Field Luminance Buffer Start Address Register (CH*n*_TY_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_LUMA	
R/W-0	

15	15
CH*n*_TOP_STRT_ADD_LUMA	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 40. Channel *n* Top Field Luminance Buffer Start Address Register (CH*n*_TY_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_LUMA	0-FFFF FFFFh	Configures access start address of SDRAM for luminance data in top field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0 on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.30 Channel *n* Bottom Field Luminance Buffer Start Address Register (CH2_BY_STRTADR and CH3_BY_STRTADR)

The channel *n* bottom field luminance buffer start address register (CH*n*_BY_STRTADR) is shown in Figure 59 and described in Table 41.

NOTE: CH3_BY_STRTADR is available in Y/C multiplexed format case in channel 3; otherwise, any configuration on CH3_BY_STRTADR is ignored.

Figure 59. Channel *n* Bottom Field Luminance Buffer Start Address Register (CH*n*_BY_STRTADR)

31															16
CH*n*_BTM_STRT_ADD_LUMA															
R/W-0															

L

15															0
CH*n*_BTM_STRT_ADD_LUMA															
R/W-0															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 41. Channel *n* Bottom Field Luminance Buffer Start Address Register (CH*n*_BY_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_LUMA	0-FFFF FFFFh	Configures access start address of SDRAM for luminance data in bottom field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.31 Channel *n* Top Field Chrominance Buffer Start Address Register (CH2_TC_STRTADR and CH3_TC_STRTADR)

The channel *n* top field chrominance buffer start address register (CH*n*_TC_STRTADR) is shown in Figure 60 and described in Table 42.

NOTE: CH2_TC_STRTADR is available in Y/C multiplexed format case in channel 0; otherwise, any configuration on CH2_TC_STRTADR is ignored.

Figure 60. Channel *n* Top Field Chrominance Buffer Start Address Register (CH*n*_TC_STRTADR)

31		16
	CH*n*_TOP_STRT_ADD_CHROMA	
	R/W-0	

15		0
	CH*n*_TOP_STRT_ADD_CHROMA	
	R/W-0	

LEGEND: R = Read only; -*n* = value after reset

Table 42. Channel *n* Top Field Chrominance Buffer Start Address Register (CH*n*_TC_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_CHROMA	0-FFFF FFFFh	Configures access start address of SDRAM for chrominance data in top field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). On raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.32 Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH2_BC_STRTADR and CH3_BC_STRTADR)

The channel *n* bottom field chrominance buffer start address register (CH*n*_BC_STRTADR) is shown in Figure 61 and described in Table 43.

NOTE: CH2_BC_STRTADR is available in Y/C multiplexed format case in channel 0; otherwise, any configuration on CH2_BC_STRTADR is ignored.

Figure 61. Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH*n*_BC_STRTADR)

31		16
CH*n*_BTM_STRT_ADD_CHROMA		
R/W-0		

15		0
CH*n*_BTM_STRT_ADD_CHROMA		
R/W-0		

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 43. Channel *n* Bottom Field Chrominance Buffer Start Address Register (CH*n*_BC_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_CHROMA	0-FFFF FFFFh	Configures access start address of SDRAM for chrominance data in bottom field on channel *n*. This address is the Area Start address in Figure 37 (sub-picture mode) and in Figure 38 (raster scanning mode). In raster scanning mode, the input data starts to be stored into SDRAM from this address. In order to configure this address, note the following regulations: In sub-picture mode, the start address should be aligned to the horizontal start of the sub-picture (LSB side N bits of this register must be 0 and N value is provided by number of 0s on the CH*n*_SP_HSZ bit in the channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG). In raster scanning mode, the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.33 Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH2_THA_STRTADR and CH3_THA_STRTADR)

The channel *n* top field horizontal ancillary data buffer start address register (CH*n*_THA_STRTADR) is shown in Figure 62 and described in Table 44.

Figure 62. Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_THA_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_HANC	
R/W-0	

15	0
CH*n*_TOP_STRT_ADD_HANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 44. Channel *n* Top Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_THA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_HANC	0-FFFF FFFFh	Configures access start address of SDRAM for horizontal ancillary data in top field on channel *n*. The output data starts to be read from this address in SDRAM (Figure 38). Data size to be read from SDRAM and displaying position is configured in other registers. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.34 Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH2_BHA_STRTADR and CH3_BHA_STRTADR)

The channel *n* bottom field horizontal ancillary data buffer start address register (CH*n*_BHA_STRTADR) is shown in Figure 63 and described in Table 45.

Figure 63. Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_BHA_STRTADR)

31	16
CH*n*_BTM_STRT_ADD_HANC	
R/W-0	

15	0
CH*n*_BTM_STRT_ADD_HANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 45. Channel *n* Bottom Field Horizontal Ancillary Data Buffer Start Address Register (CH*n*_BHA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_HANC	0-FFFF FFFFh	Configures access start address of SDRAM for horizontal ancillary data in bottom field on channel *n*. The output data starts to be read from this address in SDRAM (Figure 38). Data size to be read from SDRAM and displaying position is configured in other registers. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.35 Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH2_TVA_STRTADR and CH3_TVA_STRTADR)

The channel *n* top field vertical ancillary data buffer start address register (CH2_TVA_STRTADR) is shown in Figure 64 and described in Table 46.

Figure 64. Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_TVA_STRTADR)

31	16
CH*n*_TOP_STRT_ADD_VANC	
R/W-0	

15	0
CH*n*_TOP_STRT_ADD_VANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 46. Channel *n* Top Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_TVA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_TOP_STRT_ADD_VANC	0-FFFF FFFFh	Configures access start address of SDRAM for vertical ancillary data in top field on channel *n*. The output data starts to be read from this address in SDRAM (Figure 38). Data size to be read from SDRAM and displaying position is configured in other registers. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0).

3.36 Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH2_BVA_STRTADR and CH3_BVA_STRTADR)

The channel *n* bottom field vertical ancillary data buffer start address register (CH2_BVA_STRTADR) is shown in Figure 65 and described in Table 47.

Figure 65. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_BVA_STRTADR)

31	16
CH*n*_BTM_STRT_ADD_VANC	
R/W-0	

15	0
CH*n*_BTM_STRT_ADD_VANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 47. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (CH*n*_BVA_STRTADR) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_BTM_STRT_ADD_VANC	0-FFFF FFFFh	Configures access start address of SDRAM for vertical ancillary data in bottom field on channel *n*. The output data starts to be read from this address in SDRAM (Figure 38). Data size to be read from SDRAM and displaying position is configured in other registers. In order to configure this address, note that the start address should be aligned to 8-byte unit (3 LSBs must be 0). Even in progressive mode, the configured value in this register is effective.

3.37 Channel *n* Sub-Picture Configuration Register (CH2_SUBPIC_CFG and CH3_SUBPIC_CFG)

The channel *n* sub-picture configuration register (CH*n*_SUBPIC_CFG) is shown in Figure 66 and described in Table 48.

Figure 66. Channel *n* Sub-Picture Configuration Register (CH*n*_SUBPIC_CFG)

31	24	23	16
Reserved		CH*n*_SP_STRT	
R-0		R/W-0	

15-9	9	8	0
Reserved		CH*n*_SP_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

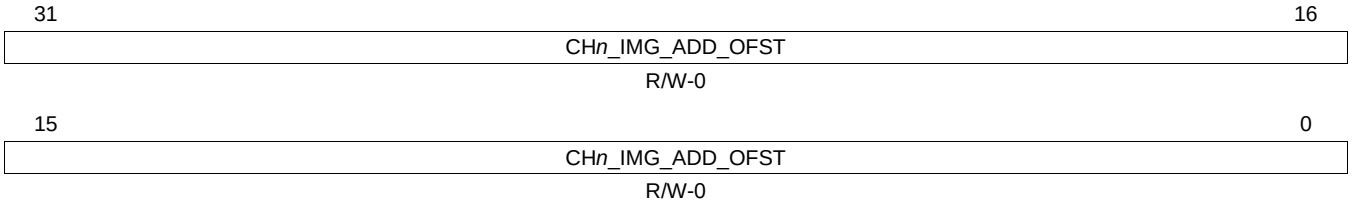
Table 48. Channel *n* Sub-Picture Configuration Register (CH*n*_SUBPIC_CFG) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	CH*n*_SP_STRT	0-FFh	Configures horizontal start position from which the input image data is stored into SDRAM. The horizontal start position defines the bytes of displacement from the Area Start address (configured in CH*n*_TY_STRTADR, CH*n*_BY_STRTADR, CH*n*_TC_STRTADR, and CH*n*_BC_STRTADR). This value must be less than the horizontal sub-picture size configured by CH*n*_SP_HSZ bit.
15-9	Reserved	0	Reserved
8-0	CH*n*_SP_HSZ	0-1FFh	Configures horizontal size of sub-picture for VPIF channel *n* output image data (only for Y/C format) that is used, if you select the sub-picture mode for the storage format of SDRAM. This value is used for channel *n* luminance and chrominance data for both the top and bottom fields. Sub-picture allocation is started from the Area Start address (configured in CH*n*_TY_STRTADR, CH*n*_BY_STRTADR, CH*n*_TC_STRTADR, and CH*n*_BC_STRTADR). Also, the configured value should be a power of 2.
		0-Fh	Reserved
		10h	16 byte
		11h-1Fh	Reserved
		20h	32 byte
		21h-3Fh	Reserved
		40h	64 byte
		41h-7Fh	Reserved
		80h	128 byte
		81h-FFh	Reserved
		100h	256 byte
		101h-1FFh	Reserved

3.38 Channel *n* Image Data Address Offset Register (CH2_IMG_ADD_OFST and CH3_IMG_ADD_OFST)

The channel *n* image data address offset register (CH*n*_IMG_ADD_OFST) is shown in Figure 67 and described in Table 49.

Figure 67. Channel *n* Image Data Address Offset Register (CH*n*_IMG_ADD_OFST)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 49. Channel *n* Image Data Address Offset Register (CH*n*_IMG_ADD_OFST) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_IMG_ADD_OFST	0-FFFF FFFFh	Configures address offset value of each line for raster store format in the image data and vertical ancillary data on VPIF channel *n*. Value is given in bytes, note that the 3 LSBs must be 0. Address calculation method on line[x] is written in the following equation: Address = CH*n*_IMG_STRT_ADD + CH*n*_IMG_ADD_OFST × line[x] line[x] = current_line – L3: top field or L9: bottom field Note that this value is valid only if SDRAM storage mode is raster scanning format. In sub-picture mode, this value is ignored.

3.39 Channel *n* Horizontal Ancillary Data Address Offset Register (CH2_HA_ADD_OFST and CH3_HA_ADD_OFST)

The channel *n* horizontal ancillary data address offset register (CH*n*_HA_ADD_OFST) is shown in Figure 68 and described in Table 50.

Figure 68. Channel *n* Horizontal Ancillary Data Address Offset Register (CH*n*_HA_ADD_OFST)

31	16
CH*n*_HANC_ADD_OFST	
R/W-0	

15	0
CH*n*_HANC_ADD_OFST	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 50. Channel *n* Horizontal Ancillary Data Address Offset Register (CH*n*_HA_ADD_OFST) Field Descriptions

Bit	Field	Value	Description
31-0	CH*n*_HANC_ADD_OFST	0-FFFF FFFFh	Configures address offset value of each line for raster store format in the horizontal ancillary data on VPIF channel *n*. Value is given in bytes, note that the 3 LSBs must be 0. Address calculation method on line[x] is written in following equation: Address = CH*n*_HANC_STRT_ADD + CH*n*_HANC_ADD_OFST × line[x] line[x] = current_line – L1: top field or L7: bottom field Note that this value is valid only if SDRAM storage mode is raster scanning format. In sub-picture mode, this value is ignored.

3.40 Channel *n* Horizontal Data Size Configuration Register (CH2_HSIZE_CFG and CH3_HSIZE_CFG)

The register image of the CH*n*_EAV2SAV and CH*n*_SAV2EAV bits is shown in Figure 51. The CH*n*_EAV2SAV and CH*n*_SAV2EAV bits do not include the 4-byte code of EAV and SAV. The channel *n* horizontal data size configuration register (CH*n*_HSIZE_CFG) is shown in Figure 69 and described in Table 51.

Figure 69. Channel *n* Horizontal Data Size Configuration Register (CH*n*_HSIZE_CFG)

31	27	26	16
Reserved		CH*n*_EAV2SAV	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_SAV2EAV	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 51. Channel *n* Horizontal Data Size Configuration Register (CH*n*_HSIZE_CFG) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_EAV2SAV	0-7FFh	Configures the horizontal distance between the EAV code and SAV code on the input data (unit size = byte) on channel *n* output. Value should be an even number (bit 16 = 0).
15-11	Reserved	0	Reserved
10-0	CH*n*_SAV2EAV	0-7FFh	Configures the horizontal distance between the SAV code and EAV code on the input data (unit size = byte) on channel *n* output. Value should be an even number (bit 0 = 0).

3.41 Channel *n* Vertical Data Size Configuration 0 Register (CH2_VSIZE_CFG0 and CH3_VSIZE_CFG0)

NOTE: Configured values on the channel *n* vertical data size configuration 0 register (CH*n*_VSIZE_CFG0) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 0 register (CH*n*_VSIZE_CFG0) is shown in Figure 70 and described in Table 52.

Figure 70. Channel *n* Vertical Data Size Configuration 0 Register (CH*n*_VSIZE_CFG0)

31	27	26	16
Reserved		CH*n*_L1	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_L3	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 52. Channel *n* Vertical Data Size Configuration 0 Register (CH*n*_VSIZE_CFG0) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_L1	0-7FFh	Configures L1 position on Figure 39.
15-11	Reserved	0	Reserved
10-0	CH*n*_L3	0-7FFh	Configures L3 position on Figure 39.

3.42 Channel *n* Vertical Data Size Configuration 1 Register (CH2_VSIZE_CFG1 and CH3_VSIZE_CFG1)

NOTE: Configured values on the channel *n* vertical data size configuration 1 register (CH*n*_VSIZE_CFG1) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 1 register (CH*n*_VSIZE_CFG1) is shown in Figure 71 and described in Table 53.

Figure 71. Channel *n* Vertical Data Size Configuration 1 Register (CH*n*_VSIZE_CFG1)

31	27	26	16
Reserved		CH*n*_L5	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_L7	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 53. Channel *n* Vertical Data Size Configuration 1 Register (CH*n*_VSIZE_CFG1) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_L5	0-7FFh	Configures L5 position on Figure 39.
15-11	Reserved	0	Reserved
10-0	CH*n*_L7	0-7FFh	Configures L7 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.

3.43 Channel *n* Vertical Data Size Configuration 2 Register (CH2_VSIZE_CFG2 and CH3_VSIZE_CFG2)

NOTE: Configured values on the channel *n* vertical data size configuration 2 register (CH*n*_VSIZE_CFG2) are reflected directly onto the hardware circuit. The hardware vertical line counter should be started from 1, not 0.

The channel *n* vertical data size configuration 2 register (CH*n*_VSIZE_CFG2) is shown in Figure 72 and described in Table 54.

Figure 72. Channel *n* Vertical Data Size Configuration 2 Register (CH*n*_VSIZE_CFG2)

31	27	26	16
Reserved		CH*n*_L9	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_L11	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 54. Channel *n* Vertical Data Size Configuration 2 Register (CH*n*_VSIZE_CFG2) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_L9	0-7FFh	Configures L9 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.
15-11	Reserved	0	Reserved
10-0	CH*n*_L11	0-7FFh	Configures L11 position on Figure 39. Note that this value is effective only when channel *n* is in the mode for receiving an interlaced picture (CH*n*_NIP bit in CH*n*_CTRL is set to 1); otherwise, this value is ignored.

3.44 Channel *n* Vertical Image Size Register (CH2_VSIZE and CH3_VSIZE)

The channel *n* vertical image size register (CH*n*_VSIZE) is shown in Figure 73 and described in Table 55.

Figure 73. Channel *n* Vertical Image Size Register (CH*n*_VSIZE)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		CH*n*_VSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 55. Channel *n* Vertical Image Size Register (CH*n*_VSIZE) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	CH*n*_VSZ	0-7FFh	Defines vertical image size of incoming video data in channel *n*. Format of value should be based on frame format.

3.45 Channel *n* Top Field Horizontal Ancillary Data Insertion Start Position Register (CH2_THA_STRTPOS and CH3_THA_STRTPOS)

The channel *n* top field horizontal ancillary data insertion start position register (CH*n*_THA_STRTPOS) is shown in Figure 74 and described in Table 56.

Figure 74. Channel *n* Top Field Horizontal Ancillary Data Insertion Start Position Register (CH*n*_THA_STRTPOS)

31	27	26	16
Reserved		CH*n*_HANC0_VPS	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_HANC0_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 56. Channel *n* Top Field Horizontal Ancillary Data Insertion Start Position Register (CH*n*_THA_STRTPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_HANC0_VPS	0-7FFh	Configures vertical start position of inserting the horizontal ancillary data in the output byte stream data. Register configuration is shown in Figure 4, Figure 5, and Figure 8. Configured value is referred to the internal line counter whose reset value is 1.
15-11	Reserved	0	Reserved
10-0	CH*n*_HANC0_HPS	0-7FFh	Configures horizontal start position of inserting the horizontal ancillary data in the output byte stream data. Register configuration is shown in Figure 8. Configured value is referred to the internal pixel counter whose reset value is 0. The configured value should be a multiple of 8.

3.46 Channel *n* Top Field Horizontal Ancillary Data Size Register (CH2_THA_SIZE and CH3_THA_SIZE)

The channel *n* top field horizontal ancillary data size register (CH*n*_THA_SIZE) is shown in Figure 75 and described in Table 57.

Figure 75. Channel *n* Top Field Horizontal Ancillary Data Size Register (CH*n*_THA_SIZE)

31	27	26	16
Reserved		CH*n*_HANC0_VSZ	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_HANC0_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 57. Channel *n* Top Field Horizontal Ancillary Data Size Register (CH*n*_THA_SIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_HANC0_VSZ	0-7FFh	Configures vertical size of horizontal ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8.
15-11	Reserved	0	Reserved
10-0	CH*n*_HANC0_HSZ	0-7FFh	Configures horizontal size of horizontal ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8. The configured value should be a multiple of 8.

3.47 Channel *n* Bottom Field Horizontal Ancillary Data Insertion Start Position Register (CH2_BHA_STRTPOS and CH3_BHA_STRTPOS)

The channel *n* bottom field horizontal ancillary data insertion start position register (CH*n*_BHA_STRTPOS) is shown in Figure 76 and described in Table 58.

Figure 76. Channel *n* Bottom Field Horizontal Ancillary Data Insertion Start Position Register (CH*n*_BHA_STRTPOS)

31	27	26	16
Reserved		CH*n*_HANC1_VPS	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_HANC1_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 58. Channel *n* Bottom Field Horizontal Ancillary Data Insertion Start Position Register (CH*n*_BHA_STRTPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_HANC1_VPS	0-7FFh	Configures vertical start position of inserting horizontal ancillary data in the output byte stream data. Register configuration is shown in Figure 4, Figure 5, and Figure 8. Configured value is referred to the internal line counter whose reset value is 1.
15-11	Reserved	0	Reserved
10-0	CH*n*_HANC1_HPS	0-7FFh	Configures horizontal start position of inserting horizontal ancillary data in the output byte stream data. Register configuration is shown in Figure 8. Configured value is referred to the internal pixel counter whose reset value is 0. The configured value should be a multiple of 8.

3.48 Channel *n* Bottom Field Horizontal Ancillary Data Size Register (CH2_BHA_SIZE and CH3_BHA_SIZE)

The channel *n* bottom field horizontal ancillary data size register (CH*n*_BHA_SIZE) is shown in Figure 77 and described in Table 59.

Figure 77. Channel *n* Bottom Field Horizontal Ancillary Data Size Register (CH*n*_BHA_SIZE)

31	27	26	16
Reserved		CH*n*_HANC1_VSZ	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_HANC1_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 59. Channel *n* Bottom Field Horizontal Ancillary Data Size Register (CH*n*_BHA_SIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_HANC1_VSZ	0-7FFh	Configures vertical size of horizontal ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8.
15-11	Reserved	0	Reserved
10-0	CH*n*_HANC1_HSZ	0-7FFh	Configures horizontal size of horizontal ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8. The configured value should be a multiple of 8.

3.49 Channel *n* Top Field Vertical Ancillary Data Insertion Start Position Register (CH2_TVA_STRTPOS and CH3_TVA_STRTPOS)

The channel *n* top field vertical ancillary data insertion start position register (CH*n*_TVA_STRTPOS) is shown in Figure 78 and described in Table 60.

Figure 78. Channel *n* Top Field Vertical Ancillary Data Insertion Start Position Register (CH*n*_TVA_STRTPOS)

31	27	26	16
Reserved		CH*n*_VANC0_VPS	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_VANC0_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 60. Channel *n* Top Field Vertical Ancillary Data Insertion Start Position Register (CH*n*_TVA_STRTPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_VANC0_VPS	0-7FFh	Configures vertical start position of inserting vertical ancillary data in the output byte stream data. Register configuration is shown in Figure 4, Figure 5, and Figure 8. Configured value is referred to internal line counter whose reset value is 1.
15-11	Reserved	0	Reserved
10-0	CH*n*_VANC0_HPS	0-7FFh	Configures horizontal start position of inserting vertical ancillary data in the output byte stream data. Register configuration is shown in Figure 8. Configured value is referred to internal pixel counter whose reset value is 0. The configured value should be a multiple of 8.

3.50 Channel *n* Top Field Vertical Ancillary Data Size Register (CH2_TVA_SIZE and CH3_TVA_SIZE)

The channel *n* top field vertical ancillary data size register (CH*n*_TVA_SIZE) is shown in Figure 79 and described in Table 61.

Figure 79. Channel *n* Top Field Vertical Ancillary Data Size Register (CH*n*_TVA_SIZE)

31	27	26	16
Reserved		CH*n*_VANC0_VSZ	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_VANC0_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 61. Channel *n* Top Field Vertical Ancillary Data Size Register (CH*n*_TVA_SIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_VANC0_VSZ	0-7FFh	Configures vertical size of vertical ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8.
15-11	Reserved	0	Reserved
10-0	CH*n*_VANC0_HSZ	0-7FFh	Configures horizontal size of vertical ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8. The configured value should be a multiple of 8.

3.51 Channel *n* Bottom Field Vertical Ancillary Data Insertion Start Position Register (CH2_BVA_STRTPOS and CH3_BVA_STRTPOS)

The channel *n* bottom field vertical ancillary data insertion start position register (CH*n*_BVA_STRTPOS) is shown in Figure 80 and described in Table 62.

Figure 80. Channel *n* Bottom Field Vertical Ancillary Data Insertion Start Position Register (CH*n*_BVA_STRTPOS)

31	27	26	16
Reserved		CH*n*_VANC1_VPS	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_VANC1_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 62. Channel *n* Bottom Field Vertical Ancillary Data Insertion Start Position Register (CH*n*_BVA_STRTPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_VANC1_VPS	0-7FFh	Configures vertical start position of inserting vertical ancillary data in the output byte stream data. Register configuration is shown in Figure 4, Figure 5, and Figure 8. Configured value is referred to internal line counter whose reset value is 1.
15-11	Reserved	0	Reserved
10-0	CH*n*_VANC1_HPS	0-7FFh	Configures horizontal start position of inserting vertical ancillary data in the output byte stream data. Register configuration is shown in Figure 8. Configured value is referred to internal pixel counter whose reset value is 0. The configured value should be a multiple of 8.

3.52 Channel *n* Bottom Field Vertical Ancillary Data Size Register (CH2_BVA_SIZE and CH3_BVA_SIZE)

The channel *n* bottom field vertical ancillary data size register (CH*n*_BVA_SIZE) is shown in Figure 81 and described in Table 63.

Figure 81. Channel *n* Bottom Field Vertical Ancillary Data Size Register (CH*n*_BVA_SIZE)

31	27	26	16
Reserved		CH*n*_VANC1_VSZ	
R-0		R/W-0	

15	11	10	0
Reserved		CH*n*_VANC1_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 63. Channel *n* Bottom Field Vertical Ancillary Data Size Register (CH*n*_BVA_SIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	CH*n*_VANC1_VSZ	0-7FFh	Configures vertical size of vertical ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8.
15-11	Reserved	0	Reserved
10-0	CH*n*_VANC1_HSZ	0-7FFh	Configures horizontal size of vertical ancillary data to be inserted in the output byte stream data. Register configuration is shown in Figure 8. The configured value should be a multiple of 8.

Appendix A Revision History

Table 64 lists the changes made since the previous version of this document.

Table 64. Document Revision History

Reference	Additions/Modifications/Deletions
Section 1.1	Changed first paragraph.
Section 1.2	Changed paragraph.
Table 1	Changed HDTV value for Square pixel common image format.
	Added footnote.
Figure 5	Changed figure.
Section 2.4.7	Deleted last bullet in first paragraph.
Table 17	Changed Description of INTEN_ERROR bit.

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