TI Designs – Precision: Verified Design Digitally Tunable MDAC-Based State Variable Filter Reference Design

V Texas Instruments

accurate digital tuning of gain, center/cut off

This MDAC based state variable filter offers highly

frequency, and quality factor. This circuit provides

three separate filter outputs: low pass, band pass,

and high pass that can be accessed simultaneously.

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Circuit Description

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Design Resources





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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V
- AC Input: 1 V_{PP}
- Output: Low pass, Band pass, High pass
- Tunability: Gain, Center/Cut off Frequency, and Quality Factor

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1	Comparison	of Design	Goals Simulation	and Measured	Performance
Table I.	Comparison	or Design	Goals, Simulation,	anu measureu	renormance

	Goal	Simulated	Measured	
Cut Off Frequency	10 Hz to 30kHz	2.11 Hz to 27.98 kHz	1.99 Hz to 28.76 kHz	
Range (3dB)	DAC Code Range: 0x0004 to 0xFFFF			
Coin Dongo	0 dB to 6dB	-54.13 dB to 6.02 dB	-53.31 dB to 6.01 dB	
Gain Range	DAC Code Range: 0x0040 to 0xFFFF			
Quality Easter Bange	0 dB to 6dB	0.47 to 2.15	0.46 to 2.14	
Quality Factor Range	DAC Code Range: 0xFFFF to 0x4000			



Figure 1: Measured Transfer Function



2 Theory of Operation



An implementation of a state variable filter using discrete resistors is shown in Figure 2



In Figure 2, amplifier A1 and A2 form summing and inverting stages followed by two op amp integrators, A3 and A4 which act as single pole low pass filters. Amplifiers A3 and A4 are cascaded to form a second-order filter. This configuration provides 3 filter outputs: low pass (LP), band pass (BP) and high pass (HP). The center frequency (in the case of the band pass) or cut off frequency (in the case of the high pass and low pass) is set by theRC circuits on both integrators. For simplicity, this RC combination is typically made equal i.e. R3 = R4 and C1 = C2.

In order to analyze this circuit, nodal equations for each node in the circuit must be solved. The resulting transfer function is shown in Equations 1, 2 & 3.

$$\frac{LP}{IN} = \frac{\frac{R_5 \cdot R_8}{C_1 \cdot C_2 \cdot R_1 \cdot R_3 \cdot R_4 \cdot R_6}}{s^2 + \frac{R_5 \cdot R_8}{C_1 \cdot R_2 \cdot R_3 \cdot R_6} \cdot s + \frac{R_8}{C_1 \cdot C_2 \cdot R_3 \cdot R_4 \cdot R_7}}$$
(1)

$$\frac{BP}{IN} = \frac{-\frac{R_5 \cdot R_8}{C_1 \cdot R_1 \cdot R_3 \cdot R_6} \cdot s}{s^2 + \frac{R_5 \cdot R_8}{C_1 \cdot R_2 \cdot R_3 \cdot R_6} \cdot s + \frac{R_8}{C_1 \cdot C_2 \cdot R_3 \cdot R_4 \cdot R_7}}$$
(2)

$$\frac{HP}{IN} = \frac{\frac{R_5 \cdot R_8}{C_1 \cdot R_1 \cdot R_3 \cdot R_6} \cdot s^2}{s^2 + \frac{R_5 \cdot R_8}{C_1 \cdot R_2 \cdot R_3 \cdot R_6} \cdot s + \frac{R_8}{C_1 \cdot C_2 \cdot R_3 \cdot R_4 \cdot R_7}}$$

$$C_1 = C_2, \quad R_3 = R_4, \quad R_7 = R_8$$
(3)

3



Equations 1, 2 & 3 are simplified by making the assumptions in Equation 4. Comparing the resulting equations with the standard equation for a band pass filter (Equation 5), yields expressions for gain (A_0), center/cut off frequency (ω), and quality factor (Q) (Equations 6, 7 & 8).

$$\frac{BP}{IN} = \frac{-\frac{A_0 \cdot \omega}{Q} \cdot s}{s^2 + \frac{\omega}{Q} \cdot s + \omega^2}$$
(5)

$$A_0 = \frac{-R_2}{R_1} \tag{6}$$

$$\omega = \frac{1}{C_1 \cdot R_3} \tag{7}$$

$$Q = \frac{R_2 \cdot R_6}{R_5 \cdot R_8} \tag{8}$$

3 Component Selection

3.1 DAC Selection

To realize eight discrete resistors a minimum of six MDACs ladders must be used. By using three dual channel MDACs with only six MDAC ladders, resistors R5 and R7 are realized by using the fixed values of two MDAC feedback resistors.

The DAC8812 is a great option for this design. It is a dual channel MDAC with strong linearity and large multiplying bandwidth which makes it ideal for this application.

Generally, MDACs are used in high performance applications that take full advantage of their strong dc specifications. MDACs have a current output and are used in conjunction with an external I-V operational amplifier. However, this design leverages the unique software-controlled output impedance property of MDACs. An important property of MDACs for this application is their reference multiplying bandwidth. The reference multiplying bandwidth changes with the programed DAC code and the bandwidth is decreased at lower codes when the reference input is highly attenuated as shown in Figure 3. Plots such as these can be found in the datasheet of any MDAC.



Figure 3: DAC8812 Reference multiplying bandwidth





Figure 4: MDAC equivalent circuit

The resistors in Figure 2 are replaced by MDACs. The circuit equivalents of an MDAC are shown in Figure 4. Resistor R5 and R7 are realized using feedback resistors integrated in the multiplying DACs. The values of these resistors are fixed and cannot be changed by writing to the MDAC. The remaining resistors are realized by the programmable ladder impedance of the MDAC. Table 2 shows the maximum and minimum values for the tunable resistors. Note that resistors R3/R4 and resistors R7/R8 are implemented such that their values are tuned simultaneously (refer to Equation 4). To realize all the resistors in this filter a minimum of six MDACs are required. Therefore three DAC8812, a 16-Bit, dual channel serial input multiplying DAC, are used in this design. The tunable resistor range for the DAC8812 is shown in Table 2. Keep in mind that the resistor ladders in the DAC8812 can vary by ±20 percent.

Resistors	MDAC	Minimum Value (0xFFFF Code)	Maximum Value (0x0001 Code)
R1	U4 A	5.02 kΩ	33.00 kΩ
R2	U4 B	5.02 kΩ	25.57 kΩ
R3	U2 A	5.00 kΩ	26.91 kΩ
R4	U2 B	5.00 kΩ	22.86 kΩ
R5	U4 B RFB	5.18 kΩ	5.18 kΩ
R6	U1 B RFB	4.96 kΩ	4.96 kΩ
R7	U1 B	4.81 kΩ	22.55 kΩ
R8	U1 A	4.81 kΩ	22.48 kΩ

Table 2. Measured resistor values tunable range with MDAC DAC8812

3.2 Amplifier Selection

This design requires four operational amplifiers. For all of these amplifiers, low input bias current is desired so that the critical parameters of the filter have exclusive tunability via the MDAC based resistors and their matching. The center/cut off frequency range for this design ranges from dc to 30 kHz, therefore high speed/high unity gain bandwidth amplifiers are not required.

The OPA277 was selected for this design because it features a sufficiently low input bias current of 1 nA.

3.3 Passive Component Selection

The high side cut off frequency is determined by the combination of capacitors C1 & C2 and the multiplying bandwidth of the MDAC with the lowest input code. The size of C1 is determined by Equation 7. The desired frequency bandwidth of the filters is 30 kHz. The DAC8812 reference input impedance is 5 k Ω paired with a 1 nF standard value for C1 will result in 32 kHz. In order to comply with Equation 4, both C1 and C2 must be the same value for the equations to be valid.



4 Simulation

The proposed circuit was simulated in TINA-TI[™] using SPICE models of both the DAC8822 and OPA277. The choice of using the DAC8822 as a simulation model was based on the core similarity with the DAC8812 and the current lack of availability of a DAC8812 model. The DAC8822 and DAC8812 are very similar devices with the minor functional difference that the DAC8822 has more feedback resistor options. The simulation suite consists of an ac simulation test bench that included center/cut off frequency, gain and quality factor for high pass, low pass and band pass outputs.

Figure 5 shows the realization of the resistors in this circuit using MDAC DAC8822.



Figure 5: State Variable Filter using DAC8822

4.1 Center/Cut Off Frequency Simulation

The center/cut off frequency simulations were carried out for all the outputs (low pass, band pass and high pass). The MDAC ladders U2A/B can be tuned, thereby changing the frequency from 2.11 Hz (code 0x0004) to 27.98 kHz (code 0xFFFF). See Equation (7). Note that 0x0000 is not used in this design because at this code all the ladder switches are open and the ladder resistance is Hi-Z.

Figure 6 shows center frequency simulations for the high pass output. For frequency simulation data for band pass and low pass filters refer to Appendix B.



Figure 6: Cut off frequency simulation – High pass output



4.2 Gain Simulation

The gain simulations were carried out for all the outputs (low pass, band pass and high pass). The MDAC ladder U4A can be tuned, thereby changing the gain from -54.13 dB (code 0x0040) to 6.02 dB (code 0xFFFF). See Equation 6.

Figure 7 shows gain simulations for the low pass output. For gain simulation data for band pass and high pass filters refer to Appendix B.



Figure 7: Gain simulation – Low pass output

4.3 Quality Factor Simulation

The quality factor simulations were carried out for all the outputs (low pass, band pass and high pass). The MDAC ladder U4B can be tuned, thereby changing the quality factor from 0.47 (code 0xFFFF) to 2.15 (code 0x4000). See Equation (8).



Figure 8 shows gain simulations for the band pass output.

Figure 8: Quality Factor simulation – Band pass output

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix A.

5.1 PCB Layout

General PCB layout best-practices should be followed for this design. Analog and digital lines must not be traced out parallel to each other in order to reduce the coupling of digital signals onto analog signal paths.



Figure 9: PCB Layout



6 Measurement

The circuit was tested using a bode plot analyzer that provided the input stimulus and measured the output response.

6.1 Center/Cut-off Frequency Measurement

The cut-off frequency setting is directly proportional to the DAC code of U2A/B. Each LSB change will adjust the frequency by approximately 0.5 Hz. For frequency measurement data for band pass and low pass filters refer to Appendix B.





Code	Simulated Freq.	Measured Freq.	Error
0x0004	2.1100 Hz	1.9900 Hz	-5.69 %
0x8000	14690 Hz	14962 Hz	-1.85 %
OxFFFF	27980 Hz	28757 Hz	-2.78 %

Table 3. high rass flequency results @ 2 kn	Table 3.	High	Pass	Frequency	/ Results	@ 2 kHz
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6.2 Gain Measurement

The gain setting is directly proportional to the DAC code of U4A. Each LSB change will adjust the gain by approximately 1 mdB. Measurements at very low codes are susceptible to noise. For gain measurement data for band pass and high pass filters refer to Appendix B.



Figure 11: Gain	measurement - L	_ow	pass	out	put
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Code	Simulated Gain	Measured Gain	Error
0x0040	-54.1276 dB	-53.3100 dB	-0.8176 dB
0x8000	0.0012 dB	0.0007 dB	0.0004 dB

6.0140 dB

0.0060 dB

Table 4. Low Pass Gain Results

6.0200 dB

OxFFFF



6.3 Quality Factor Measurement

The quality factor measurement is inversely proportional to the DAC code of U4B. Each LSB change will adjust the quality factor by approximately 52µ. The quality factor can be controlled independently of gain by using another MDAC to control resistors R5 & R6. For information about how to calculate quality factor, please refer to Appendix B.





Code	Simulated Q-Factor	Measured Q-Factor	Error
0x4000	2.1524	2.1424	-0.46 %
0x8000	0.9461	1.0077	6.52 %
OxFFFF	0.4691	0.4660	-0.65 %

Table 5. Band Pa	ss Quality	Factor Results
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7 Modifications

Depending on the design requirement other multiplying DACs can be used in this design. DAC8812 was selected for its serial interface, high resolution, and superior multiplying bandwidth. Table 6 shows other MDAC options for application that may not require high resolution or that may require a parallel interface. Table 7 shows alternative amplifiers that can be used in this design for larger bandwidth or minimal input bias current.

MDAC	Resolution	Channel Count	Interface	Reference multiplying bandwidth
DAC8812	16 bits	2	Serial	10 MHz
DAC8822	16 bits	2	Parallel	10 MHz
DAC8802	14 bits	2	Serial	10 MHz
DAC8805	14 bits	2	Parallel	10 MHz
DAC7822	12 bits	2	Parallel	10 MHz

Table 6. Alternative MDACs

Table 7. Alternative operational amplifiers

Amplifier	Supply	Bandwidth	Input bias current (Typ.)
OPA277	±18 V	1 MHz	±500 nA
OPA211	±18 V	80 MHz	±50 nA
OPA188	±18 V	2 MHz	±160 pA
OPA170	±18 V	1.2 MHz	±8 pA

8 About the Author

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9 Acknowledgements & References

- 1. Engineer It, What is a multiplying DAC (MDAC)? (Video)
- 2. Build a three phase sine wave generator with the UAF421 (SBFA013)
- 3. Design a 60 Hz notch filter with the UAF42 (SBFA012)
- 4. TLC7528, Digitally-controlled state-variable filter application information (SLAS062E)
- 5. TIPD137, ±10V 4-Quadrant Multiplying DAC (TIDU031)



Appendix A.

A.1 Electrical Schematic



Figure A-1: Electrical Schematic

A.2 Bill of Materials

B TI DESU TIPD'	TEXAS INSTRUM III Of IGNS 60: Digitally Tu	nable ME	aterials DAC based State Variable Filter			
Iten	n # Quantity	Value	Designator	Description	Manufacturer	PartNumber
1	14	1uF	C1, C2, C9, C10, C11, C12, C15, C17, C18, C20, C25, C26, C28, C30	CAP, CERM, 0.1uF, 25V, +/-10%, X5R, 0603	MuRata	GRM188R61E104KA01D
2	11	100pF	C3, C4, C7, C8, C13, C14, C16, C21, C22, C24, C31	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H101J
3	1		C5	Not Installed	MuRata	
4	2	1000pF	C6, C23	CAP, CERM, 1000pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H102KA01D
5	3	10uF	C19, C27, C29	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	MuRata	GRM31CR61E106KA12L
6	4		J1, J3, J4, JP8	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S
7	4		J2, J5, J6, J9	Connector, TH, SMA	Emerson Network Power	142-0701-201
8	1		J7	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
9	1		J8	Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
10	9	10.01	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP9, JP10	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec	TSW-103-07-G-S
11	1	49.9kΩ		RES, 49.9 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0749R9L
12	4		[1P1, 1P6, 1P10, 1P12	Lest Point, Miniature, Black, TH	Keystone	5001
13	8		[TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP11	Test Point, Miniature, Red, TH	Keystone	5000
14	3		101, 02, 04	Dual, Serial Input 16-Bit Multiplying Digital-to-Analog Converter, PW0016A	Lexas Instruments	DAC8812ICPW

Figure A-2: Bill of Materials



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NSTRUMENTS

Appendix B.



B.1 Center/Cut Off Frequency Simulation & Measurements





Figure B-2: Cut-off frequency measurement – Low pass output

Code	Simulated Freq.	Measured Freq.	Error
0x0004	2.2138 Hz	1.9387 Hz	-12.45 %
0x8000	17.1738 kHz	16.8585 kHz	-1.84 %
OxFFFF	36.81 kHz	35.6480 kHz	-3.16 %

Tahlo	8		Pass	Fred	uionc\	Rosulte
Iaple	о.	LOW	ra55	гіец	uency	/ Results







Figure B-4: Cut-off frequency measurement – Band pass output Table 9. Band Pass Frequency Results

Code	Simulated Freq.	Measured Freq.	Error
0x0004	2.2514 Hz	1.9387 Hz	-13.89 %
0x8000	17.7834 kHz	16.7400 kHz	-5.87 %
OxFFFF	35.4852 kHz	35.7890 kHz	0.86 %

EXAS







Figure B-5: Gain simulation – High pass output



Figure B-6: Gain measurement – High pass output

Code	Simulated Gain	Measured Gain	Error
0x0004	-52.8254 dB	-45.7880 dB	-7.04 dB
0x8000	1.2612 dB	1.1631	0.10 dB
OxFFFF	7.3731 dB	7.3293	0.04 dB

Table 10. High Pass Gain Results @ 50 kHz











Code	Simulated Gain	Measured Gain	Error
0x0004	3.7835 dB	3.5845 dB	0.20 dB
0x8000	-2.2214 dB	-2.4316 dB	0.21 dB
OxFFFF	-56.3345 dB	-53.9780 dB	-2.36 dB

	Tab	le 1	11.	Band	Pass	Gain	Results
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B.3 Quality Factor Simulation & Measurements

The quality factor is calculated using Equation (9), the center frequency (f_c) and the -3 dB bandwidth (Δf_{3dB}) of the bandpass filter.

$$Q = \frac{f_c}{\Delta f_{-3dB}} \tag{9}$$

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