TI Designs

Interfacing Current Output Hall Sensors and CTs With Pseudo-Differential ADC/MCU Reference Design

TI Designs

This design provides a reference solution for interfacing current output Hall sensors and current transformers to pseudo-differential ADC (standalone and integrated into MCU). Two variants of signal conditioning circuits are designed to measure motor current using bipolar and unipolar supply voltages respectively. Both signal conditioning circuits provide current measurement accuracy within ±0.5% for an operating temperature range from –25°C to 75°C.

Design Resources

TIDA-00316	Design Folder
TPS62150	Product Folder
TPS7A3001	Product Folder
TPS7A4901	Product Folder
OPA2192	Product Folder
OPA2322	Product Folder
TLV1702	Product Folder
LP2992A-5.0	Product Folder
REF2033	Product Folder
REF2025	Product Folder

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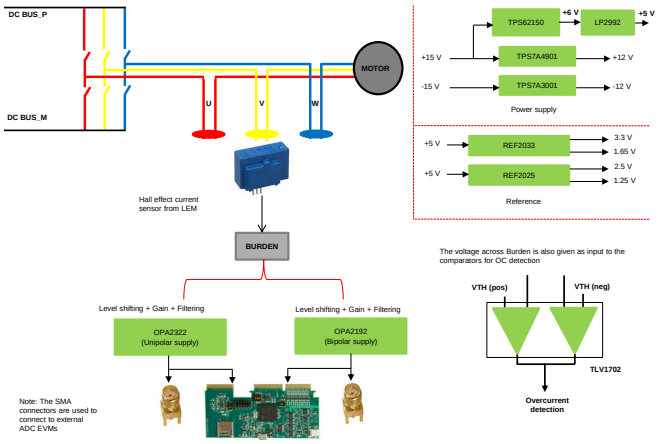
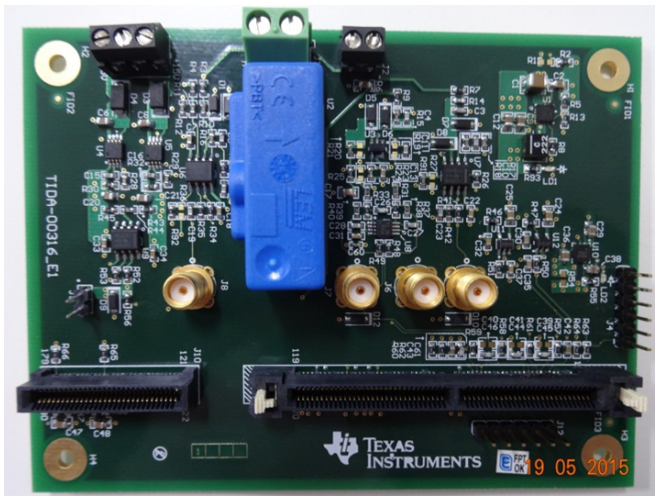
Design Features

- Onboard Current-Output Hall Sensor to Measure Nominal Current up to 25-A_{RMS}
- Current Measurement Accuracy of 0.5%
- Common Reference Solution for Interfacing Both CT and Current Output Hall Sensor With Pseudo-Differential ADC/MCU
- Two Different Variants to Work on Unipolar and Bipolar Supply Rails
- Designed to Evaluate With Delfino F2837x Control Card
- Designed to Evaluate With External ADC (ADS7253) for Interfacing With Motor Controller

Featured Applications

- AC Variable Speed Industrial Drives
- Servo Motor Drives
- UPS Systems
- Solar Inverters
- AC/DC and DC/DC Power Supplies





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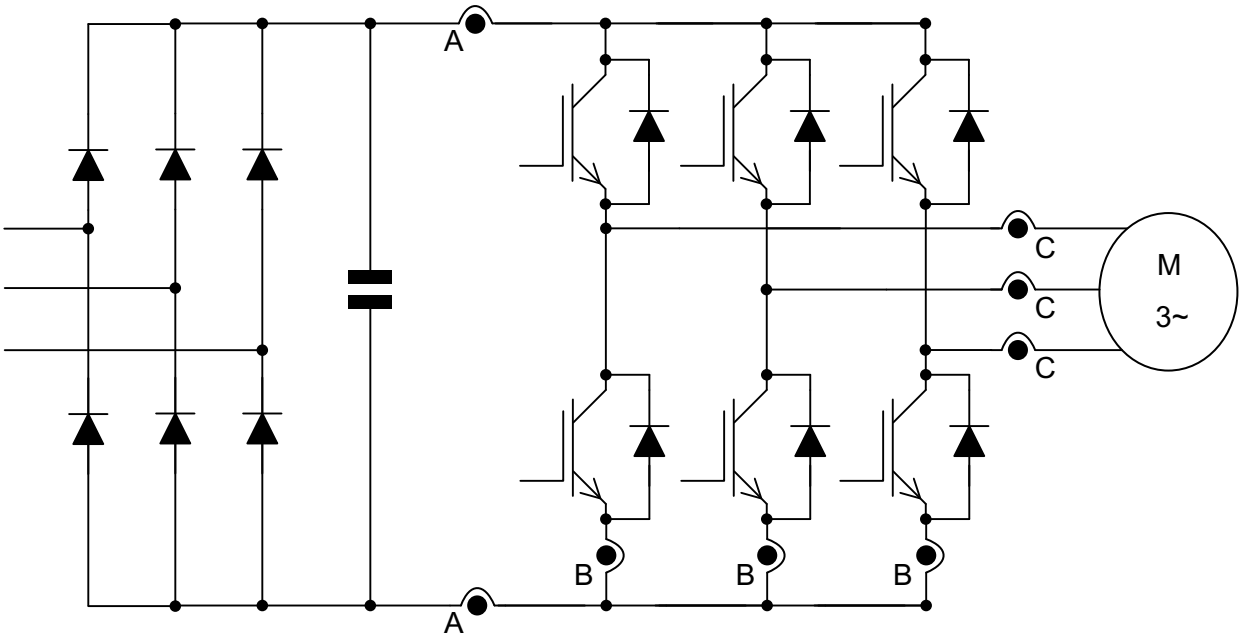
1 System Description

Current measurement is an inherent part of any inverter-driven application. One important reason for measuring the motor current is to perform a control algorithm. Vector control and direct torque control require current sensing for control purposes. Information of motor parameters is also important for several control schemes. Stator current measurement is used to estimate these parameters. Current measurement is also used for hardware overload and earth fault protection.

The inverter output rating needs to be derated while operating at higher temperature. The higher temperature could be due to increased ambient, a faulty fan, or obstructions in cooling path. In those scenarios, current measurement helps in derating the inverter current in order to keep the power devices within its permissible operating temperature.

The motor current can be measured at different locations in the inverter. Figure 1 shows the overview of usual measurement locations, considering a 3-phase inverter for a motor control application:



A) Current measurement in the DC- and DC+ link
B) Current measurement in the bottom side emitter path of each half-bridge
C) Current measurement in the output phases

Figure 1. Typical Measuring Locations for Current Measurement in Motor Drives

The cheapest variant of current measurement ("A") is often used for applications in the lower power range. Typically, the current measurement is done on DC minus bus; this may be the reference potential of the microcontroller and therefore is not necessary to isolate the signal. Another alternative location of current measurement, found particularly in the low to medium power range, is variant "B". In this case, the current is measured at the emitter of the bottom IGBT of each arm in a 3-phase inverter. It may also be possible to dispense with a third current measurement; this can be derived by calculation based on the measured two current signals. The advantage of this measurement method is similar to that of variant "A", in that the negative section of the DC-bus can be taken as the common reference potential. However, the disadvantage is the increased stray inductance. In high dynamic drives and high-power applications, current is usually measured in the output phases of the inverter (variant "C" in Figure 1). The third current sensor is not necessary in this case either.

The design TIDA-00316 is meant for current measurement (variant "C") using current-output Hall-effect sensors in AC and DC drives. The objective of this design is to provide a reference solution for pseudo-differential signal conditioning circuit to measure motor current using current-output Hall-effect sensors (typically available from companies like LEM Technologies www.lem.com and VACUUMSCHMELZE or VAC http://www.vacuumschmelze.com/) and current transformers (CTs). It is very common to use single-ended ADCs integrated into the controller for current measurement.

The signal conditioning circuit for Hall-effect sensors is required for the following reasons:

- Current output Hall sensors are typically powered from ±12 V or ±15 V leading to bipolar output signal swing. Interfacing this to an ADC with a 3.3-V reference would need amplifier plus level shifting.
- In industrial motor drives, it is pretty common to use the sensor up to 200% to 250% of its rating. It is important to detect over load condition and protect the drive.
- Higher input offset voltage, temperature drift, noise, and linearity leads to error in motor current measurement, thereby affecting control loop performance. Proper signal conditioning circuit makes sure to reduce the errors and noise from the sensors.
- If using ADC inside Delfino™ F2837x, the common-mode voltage needs to be shifted from 2.5 V to 1.65 V.

2 Block Diagram

The system block diagram for TIDA-00316 is shown in Figure 2. The design uses the Onboard Current-Output Hall-Effect Sensor to measure the motor current. Also, the design provides a connection to an external CT to the signal conditioning circuit for current measurement. For both the Hall-effect sensor and CT, the burden resistor is available on the board.

The voltage across the burden resistor is signal-conditioned in two different ways:

1. Pseudo-differential with unipolar supply – Using OPA2322
2. Pseudo-differential with bipolar supply – Using OPA2192

The outputs of the above signal conditioning circuits are connected to:

- 180-pin connector to interface with Internal ADC of Delfino F2837x.
- SMA Connectors to evaluate the performance of the signal conditioning circuit with external ADCs like ADS7253.

The Hall-effect sensor is powered using power supply of ±12 V, which is generated from ±15 V (using the TPS7A4901 and TPS7A3001). The signal conditioning circuit in unipolar section is powered using 5-V DC generated from a 15-V supply (using the TPS62150 and LP2992). The 5 V is used to power op-amp OPA2322. The bipolar op-amp OPA2192 is powered using ±12V generated out of ±15V supply. For both Pseudo-differential signal conditioning circuits, the output common-mode voltage (V_{OCM}) can be set at 2.5 V when used with external 5-V ADCs or 1.65 V when used with internal ADC of Delfino F2837x Controller. The REF2033 is used to generate reference voltage of 1.65 and 3.3 V. To protect against an overcurrent Fault condition, the sensed current is fed to two comparators, available in single device TLV1702 (one for detection of overcurrent in positive half-cycle and one for detection of overcurrent in negative half-cycle). Both the protection circuits have a response time of less than 500 ns.

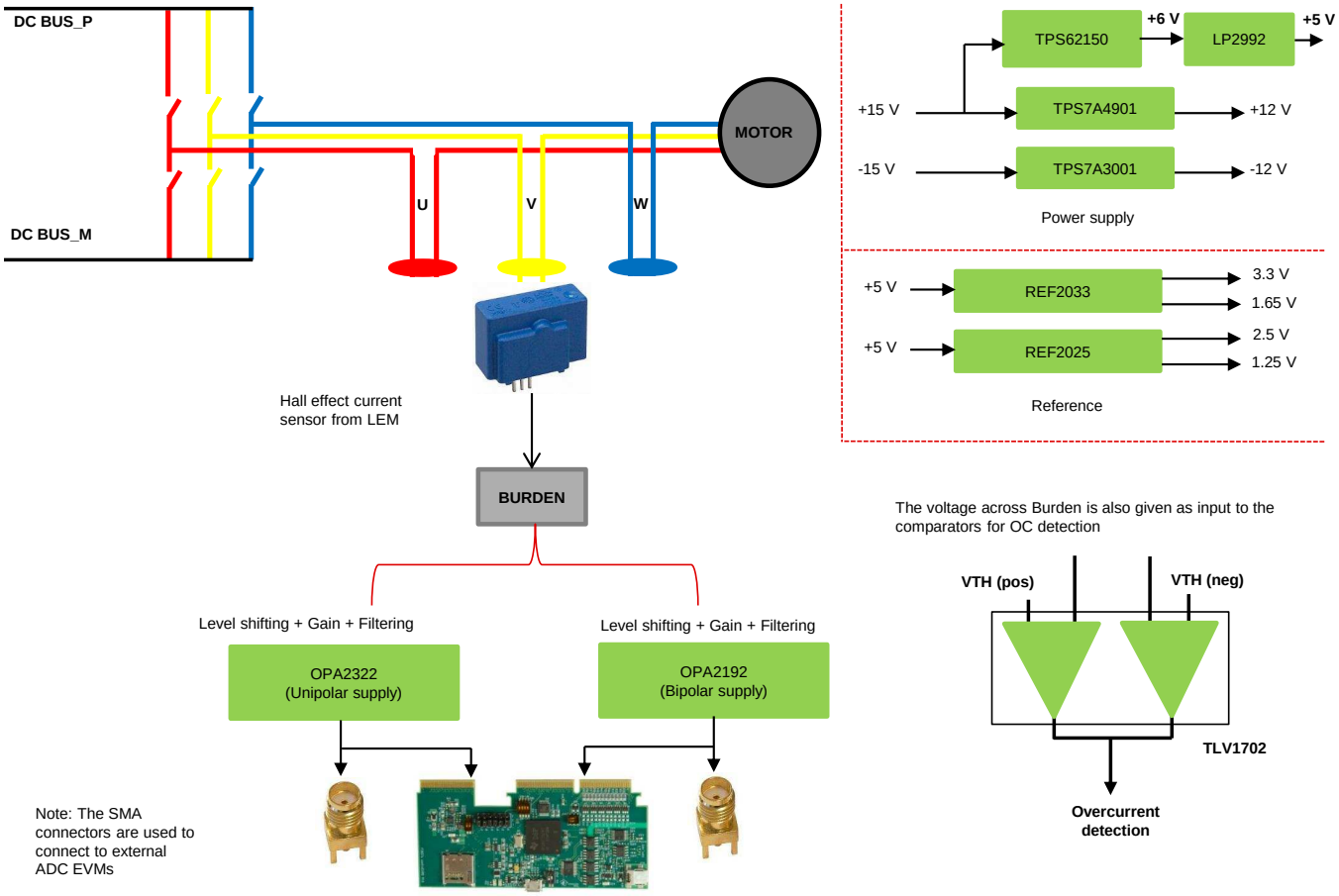


Figure 2. System Block Diagram

2.1 Highlighted Products

This reference design features the following devices from Texas Instruments:

- TPS62150: Buck step-down regulator with 3- to 17-V input and 0.9- to 6-V output, –40°C to 85°C, 16-pin QFN (RGT), green (RoHS and no Sb/Br)
- TPS7A3001: Single output, high PSRR LDO, 200 mA, adjustable –1.18- to –33-V output, –3- to –36-V input, with ultra-low noise, 8-pin MSOP (DGN), –40°C to 125°C, green (RoHS and no Sb/Br)
- TPS7A4901: Single output, high PSRR LDO, 150 mA, adjustable 1.2- to 33-V output, 3- to 36-V input, with ultra-low noise, 8-pin MSOP (DGN), –40°C to 125°C, green (RoHS and no Sb/Br)
- OPA2192: High voltage, rail-to-rail input/output, precision operational amplifiers, e-trim™ series, D0008A
- OPA2322A: 20 MHz, low noise, RRIO, CMOS operational amplifier, 1.8 to 5.5 V, –40°C to 125°C, 8-pin SOIC (D0008A), green (RoHS and no Sb/Br)
- TLV1702: Dual, 2.2-V to 36-V, micropower comparator
- LP2992AILD-5.0/NOPB: Micropower 250-mA low-noise ultra-low dropout regulator, 6-pin LLP, Pb free
- REF2033: Low-drift, low-power, dual-output, V_{REF} and V_{REF} / 2 voltage references, DDC0005A
- REF2025: Dual output voltage reference 2.5 V, DBV0005A

For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design (Design Resources).

3 Hall Sensors

3.1 Closed Loop Hall Sensor

Conductor carrying a current IP (Figure 3) generates a magnetic field, which is concentrated in a magnetic circuit. This field can be measured in an air gap by using a Hall element. The latter has the property of converting the magnetic flux into a voltage, when it is supplied with a constant current I_C. When applying the closed-loop principle, the Hall voltage is only used for balancing the primary and the secondary flux. The additional secondary coil, for example with 2,000 turns, carries a current I_S, which equals 1/2000 of the primary current in order to exactly compensate for the field of the primary conductor. The total flux then equals zero. Operating the Hall generator in a zero flux condition eliminates the drift of gain with temperature. When the magnetic flux is fully compensated (zero), the magnetic potential (ampere-turns) of the two coils is identical. Therefore:

$$N_P \times I_P = N_S \times I_S \text{ which can also be written as } I_S = I_P \times \frac{N_P}{N_S} \quad (1)$$

Consequently, the secondary current, I_S, is the exact image of the primary current, I_P, being measured. Inserting a "measurement resistor", R_M, in series with the secondary coil creates an output voltage that is an exact image of the measured current. To give an order of magnitude, the typical number of secondary turns is N_S = 1000 to 5000 and the secondary current is usually between I_S = 25 to 300 mA, although it could be as high as 2 A.

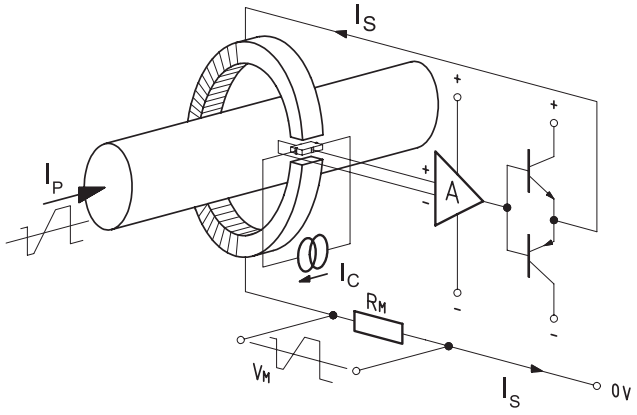


Figure 3. Operating Principle of Closed Loop Hall Transducer

3.2 Advantages and Limitations

Closed loop transducers are capable of measuring DC, AC, and complex current waveforms while ensuring galvanic isolation. The advantages of closed loop sensors include very good accuracy and linearity, low gain drift, wide bandwidth, and fast response time. Another advantage is the output current signal is easily scalable and well suited to high noise environments; nevertheless, closed loop transducers are available in voltage output configurations. Again, as with most magnetic-based measurement techniques, insertion losses are very low. The main limitations of the closed loop technology are the high current consumption from the secondary supply (which must provide the compensation as well as bias current), the larger dimensions (more noticeable on high current transducers), a more expensive construction compared with the simpler open loop designs, and a limited output voltage due to the internal voltage drops across the output stage and secondary coil resistance. Again, depending on the application requirements, the advantages often outweigh the limitations and the accuracy and response of a closed loop solution is desirable over other alternatives.

3.3 Hall Sensor "LAH 25-NP" From LEM Technologies

Selecting the right transducer is often a tradeoff between several parameters: operating current range, output signal type, accuracy, frequency response, dv/dt, temperature range, weight, size, costs, and so on. LAH 25-NP is closed-loop (compensated) multi-range current transducer using Hall effect from LEM Technologies. It is typically used to measure current (DC, AC, or pulsed) with galvanic separation between the primary and secondary circuit. The internal structure of LAH 25-NP is shown in Figure 4.

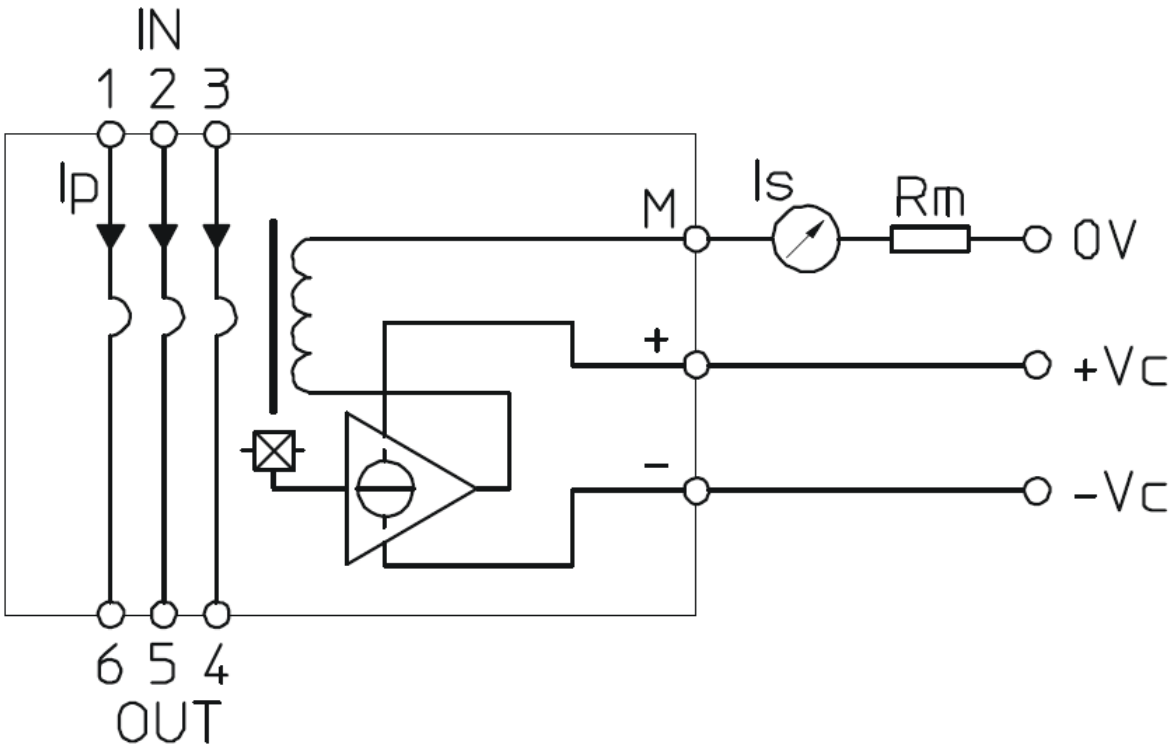


Figure 4. Internal Structure of LAH 25-NP

The LAH 25-NP takes dual power supply and provides current output from pin M. The output (or secondary) current is proportional to primary current and turns ratio.

Closed loop Hall sensors provide excellent accuracy at 25°C, in general below 1% of the nominal range, and a reduced error over the specified temperature range (–40°C to 105°C). Figure 5 shows the accuracy data for LAH 25-NP (taken from its datasheet).

Accuracy - Dynamic performance data			
X	Accuracy [5] @ I_{PN}, T_A = 25°C	± 0.3	%
ε_L	Linearity error	< 0.2	%

Figure 5. Accuracy of LAH 25-NP

4 Component Selection

4.1 Calculation of Burden Resistor for LAH 25-NP

The burden is calculated according to procedure given in the "Technical Manual" from LEM Technologies. The measuring voltage generated at the terminals of the burden resistor (V_M) depends on the amplitude of the primary current I_P, the turns ratio of the transducer K_N, and the measuring (or burden) resistor R_M. The nominal current I_{PN} determines the type of transducer and its turns ratio K_N. The voltage measured at a given primary peak current IP is thus determined by the choice of the resistor RM.

(a) Nominal current to be measured: 8 A

(b) Peak current → Overload condition: 225% of the nominal, which is 8 × 2.25 = 18 A

(c) Ambient temperature: 70°C

(d) Transducer supply voltage: ±12 V

(e) Referring to the datasheet of LAH 25-NP, the PCB connection should be as shown in third row in Figure 6. For that condition, the value of K_N is equal to 3:1000.

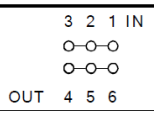
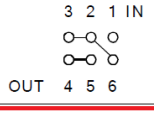
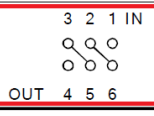
Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	
2	12	27	24	2 : 1000	0.81	0.054	
3	8	18	24	3 : 1000	1.62	0.110	

Figure 6. Recommended PCB Connections and Corresponding Parameter

4.1.1 Calculation of R_M for 5-V ADC System

For a 5-V ADC, the mid-voltage value is 2.5 V. Keeping a margin of 0.25 V, the range of input voltages for the 5-V ADC is 0.25 to 4.75 V. That means the voltage across the burden should be 2.25 V when primary current is at its peak value.

- For positive peak current through the primary of the Hall sensor → 2.5 V + 2.25 V = 4.75 V
- For negative peak current through the primary of the Hall sensor → 2.5 V – 2.25 V = 0.25 V

$$R_M = \frac{V_M}{I_P \times K_N} \quad (2)$$

Using Equation 2,

- V_M = 2.25 V
- I_P = 18 A
- K_N = 3:1000
- R_M = 41.67 Ω

The selected value of R_M is 42.2 Ω.

4.1.2 Calculation of R_M for 3.3-V ADC System

For a 3.3-V ADC, mid-voltage value is 1.65 V. Keeping a margin of 0.25 V, the range of input voltages for the 3.3-V ADC is 0.25 to 3.05 V. That means the voltage across the burden should be 1.4 V when primary current is at its peak value.

- For positive peak current through the primary of the Hall sensor → 1.65 V + 1.4 V = 3.05 V
- For negative peak current through the primary of the Hall sensor → 1.65 V – 1.4 V = 0.25 V

Using Equation 2,

- V_M = 1.4 V
- I_P = 18 A
- K_N = 3:1000
- R_M = 25.93 Ω

The selected value of R_M is 27 Ω.

4.2 Selection of Power Supply Components

The current sensor (LAH 25-NP) requires a bipolar supply rails of ±12 V and hence the board is designed to be powered from ±15 V (max).

From a ±15-V input, mainly there are two different voltages required:

1. 15 V to ±12 V for Hall sensor, bipolar-supply op-amp as well as comparator.
2. 15 V to 5 V for supplying unipolar-supply op-amp, onboard reference devices, Delfino Control Card.

For applications requiring positive as well as negative high-performance rails (to power precision signal chain components), the TPS7A49xx and TPS7A30xx devices are most suitable.

From 15-V to 5-V generation, linear regulator is not a good option as it will have more power consumption. Also, the 5-V rail is used to power the op-amps which are important elements of the signal conditioning. It should be clean and quite. For these reason, one switching buck converter followed by a linear regulator can be used.

Following components are used for this design:

- 15 V to 6 V conversion using TPS62150
- 6 V to 5 V conversion using LP2992

4.3 Selection of Op-Amps

The op-amp is a critical piece of the analog signal chain and can often have a dramatic impact on the performance of the entire signal chain. Be it bipolar or unipolar signal conditioning circuit, the primary functions of this op-amp are:

1. To buffer the inputs coming from the sensor
2. To provide amplification of the low level input signals coming from the sensor
3. To provide the desired common-mode voltage at the output
4. To provide proper filtering for the signal connected to ADC

Table 1 gives a comprehensive list of the factors that need to be considered in determining the choice of the op-amp.

Table 1. Selection Considerations for Op-Amp

REQUIREMENT	BENEFIT
High input impedance	Minimizing this reduces input loading on sensor and minimizes input current offsets on input resistors.
Input current noise	Minimizing this reduces the amount of current noise that becomes converted to voltage noise on input resistors.
Voltage noise	Minimizing this improves the overall signal-to-noise ratio.
CMRR versus frequency	Maximizing this reduces the amount of input offset changes due to high dv/dt at the inverter output.
Voltage offset drift	Minimizing this reduces the amount that the total unadjusted error changes at the output of the op-amp.
Single supply or dual supply operation	Designing a single-supply amplifier simplifies the system supply requirements; this usually correlates with lower power architecture. However, if the signal coming from sensor itself is bipolar, it is good to use op-amp with dual supply options.
Input type	Rail-to-rail input can help to interface sensors having large input swings.
Output type	With rail-to-rail output configuration, the amplified input signal can reach the supply voltage and can use the FS range of ADC in a better way

For bipolar signal conditioning circuit, this reference design uses the OPA2192. It is a dual-channel op-amp with a supply voltage range from ±2 to ±18 V. With rail-to-rail input and output options, it has very low offset (±5 µV, typical).

For unipolar signal conditioning circuit, this reference design uses the OPA2322. The OPA2322 is a dual-channel CMOS operational amplifier featuring low noise and rail-to-rail inputs/outputs optimized for single-supply applications. It is a low-cost amplifier with a maximum offset voltage of 2 mV.

4.4 Selection of Voltage References

When external ADCs (which are powered using a 5-V single supply) are used for capturing the data, the reference voltage should be set to 2.5 V. When Internal ADCs (of Delfino controller) are used in single-ended mode, the reference pin needs to be powered from a 3.3-V reference (Delfino converts 3.3 V into a 1.65-V reference internally). To fulfill all these conditions, three reference voltages are required (2.5 V, 3.3 V, and 1.65 V).

The REF20xx series provides a reference voltage (V_{REF}) and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals. The V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the entire temperature range. The REF20xx family is specified to deliver a current load of ±20 mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA.

4.5 Selection of Comparator

Current state-of-the-art inverters are equipped with full IGBT protection, including overcurrent and ground-fault protection. An overcurrent condition is one of the fatal drive faults that could destroy IGBT devices in a motor-drive system. IGBT overcurrent conditions basically fall into three categories: line-to-line short, ground fault, and shoot through.

Table 2. Overcurrent Conditions and Possible Causes

OVERCURRENT CONDITION	POTENTIAL CAUSE
Ground fault	Motor insulation breakdown to ground
Line-to-line short	Mis-wiring, motor leads short, motor phase-to-phase insulation breakdown
Shoot-through	False IGBT turn-on

Table 2 lists overcurrent conditions and their potential causes. When considering an IGBT overcurrent protection scheme, two important factors must be evaluated. The first factor is what type of overcurrent protection the system should provide and how the system can be shut down. The second factor is the control architecture. Control architecture significantly influences the method and implementation of the overcurrent protection. Protection of IGBT devices is normally implemented in the hardware circuit. However, the circuit implementation and the type of overcurrent-sensing device vary depending on which overcurrent condition is being addressed.

The overcurrent protection can be implemented using two comparators. The two thresholds are required: one for positive cycle and one for negative cycle. These thresholds need to be derived based on the voltage across burden resistor. Total propagation delay of shutdown also is important. The current sensor itself has some delay, which includes delay for the sensing mechanism and its own response time. Therefore, no matter how the protection circuit is implemented, this delay time should be added to the circuit delay to meet the IGBT short-circuit duration time.

There are four criteria for choosing the comparator:

1. Propagation delay: Typically, industrial motor drives need an overcurrent protection shutdown to be triggered within 1 µs. It means that the comparator should have a propagation delay of 500 ns or less.
2. Supply voltage: The current output Hall-effect sensor LAH 25-NP operates on the dual supply, which means the output voltage (across burden resistor) also varies in positive as well as negative range. This asks for a comparator with dual supply same as the sensor, which is ±12 V.
3. Output type: The output of the comparator is digital signal indicating the overcurrent protection. It is typically connected to a GPIO or ADC of a microcontroller. Therefore, the maximum output voltage can go up to 3.3 V. If the comparator output is open-drain or open-collector type, then it can be connected to a 3.3-V supply using a pull-up resistor.
4. Size and cost: It is better to have single package with two comparators. The cost of the comparator should be as low as possible.

Based on the different requirements, this design uses the TLV1702 as comparator for overcurrent protection mechanism. The TLV1702 is dual supply (±1.1 to ±18 V) comparator with two channels. The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to 36 V regardless of the supply voltage. The propagation delay for the TLV1702 is 560 ns and is available in a VSSOP-8 package. It is specified for operation across the expanded industrial range of –40°C to 125°C.

5 System Design

5.1 Sensor Circuit Design

From the datasheet of sensor LAH 25-NP, it can be configured to measure nominal primary current of 8 A, 12 A, and 25 A. Figure 7 (taken from the datasheet of LAH 25-NP) shows the PCB connection to be done for using the sensor for different current ratings.

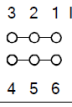
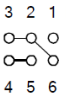
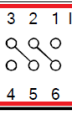
Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	
2	12	27	24	2 : 1000	0.81	0.054	
3	8	18	24	3 : 1000	1.62	0.110	

Figure 7. Recommended PCB Connection for LAH 25-NP

Based on Figure 7, connections are done on the schematic as shown in Figure 8.

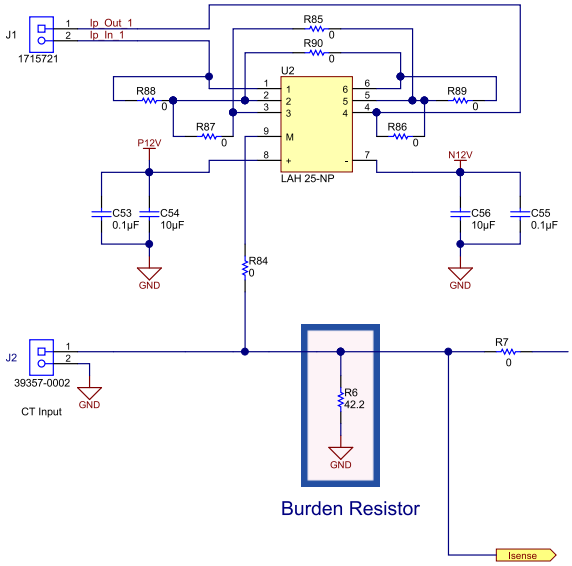


Figure 8. Schematic Section Showing Connections for LAH 25-NP

Table 3 gives the details about which resistors should be mounted to achieve a particular nominal input current setting.

Table 3. Resistor Straps on Board

NOMINAL PRIMARY CURRENT (A)	POPULATE THESE RESISTORS ONLY
8	R85, R90
12	R86, R90
25	R86, R87, R88, R89

5.2 Generation of ±12 V for Powering LAH 25-NP, OPA2192, and TLV1702

For applications that require positive and negative high performance rails, TI recommends using TPS7A40xx and TPS7A30xx families of linear regulators. Figure 9 shows the generation of ±12 V from a ±15-V input supply.

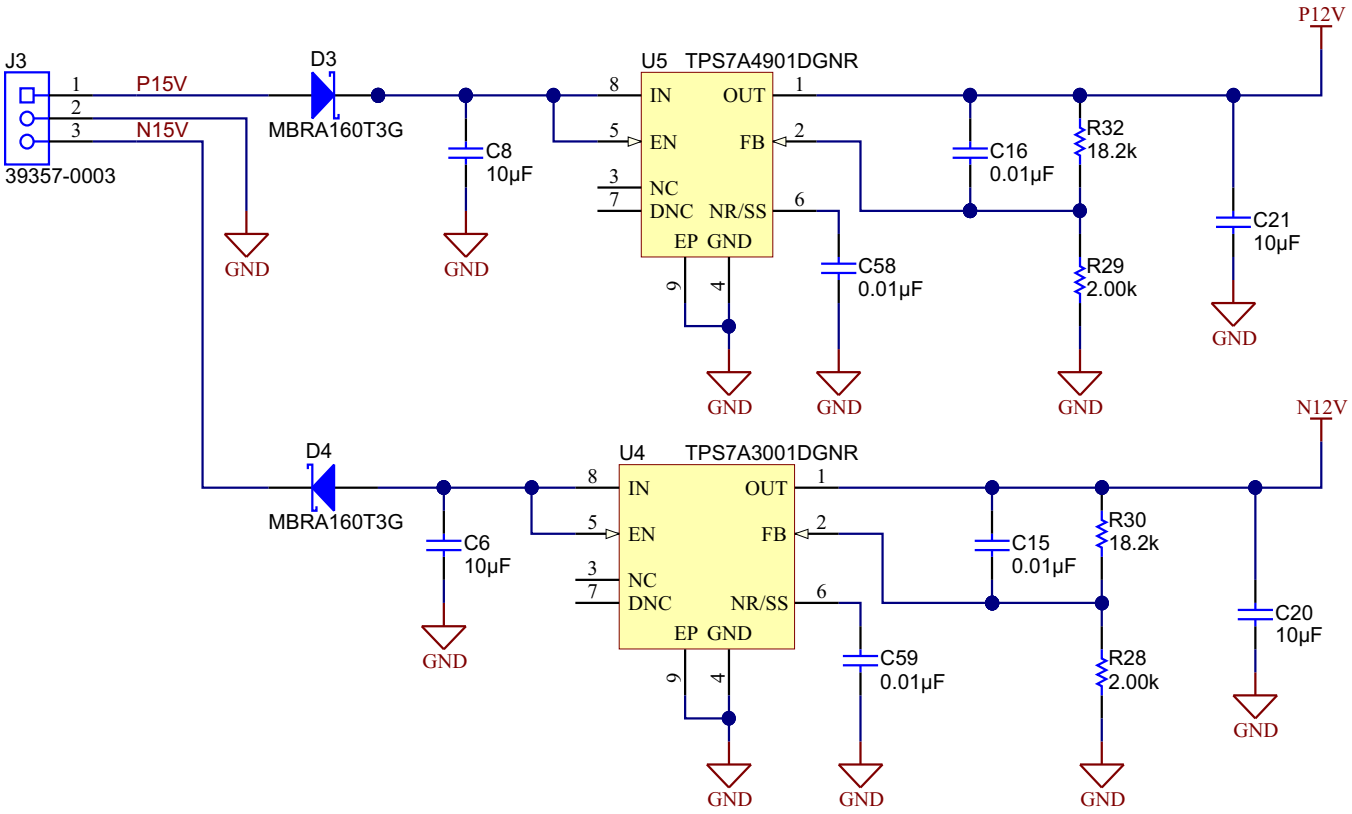


Figure 9. Generation of ±12 V from ±15 V

The TPS7A4901 is a high voltage, positive, highly accurate linear regulator designed to power operational amplifiers and other high-performance analog circuitry. In this design, the TPS7A4901 is used to generate 12 V from a 15-V rail. Two 10-µF caps are connected: C8 on the input and C21 on the output of TPS7A4901. The TPS7A4901 requires a capacitor ≥ 2.2 µF from output pin connected to ground to ensure stability. The TPS7A3001 is a high voltage, positive, highly accurate linear regulator designed to power op-amp and other high-performance analog circuitry. In this design, the TPS7A3001 is used to generate –12 V from a –15-V rail. Two 10-µF caps are connected: C6 on the input and C20 on the output of the TPS7A3001. The TPS7A3001 requires a capacitor ≥ 2.2 µF from output pin connected to ground to ensure stability.

For both the devices, NR/SS pin bypasses noise generated by the internal bandgap. Capacitors C58 and C59 (connected to NR/SS pin) allows RMS noise to be reduced to very low levels and also controls the soft-start function. The soft start time is calculated as given in Equation 3.

$$t_{ss}(ms) = 1.4 \times C_{NR/SS}(nF) \quad (3)$$

So for both the devices, with a capacitor value of 0.01 µF, the soft start time is 14 ns.

The outputs for the TPS7A4901 and TPS7A3001 are set to 12 V and –12 V respectively using Equation 4.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB(nom)}} - 1 \right), \text{ where } \frac{V_{FB(nom)}}{R_2} > 5\ \mu A \quad (4)$$

For a 12-V output, the feedback resistors are R32 = 18.2 kΩ and R29 = 2 kΩ. For a -12-V output, the feedback resistors are R30 = 18.2 kΩ and R28 = 2 kΩ.

5.3 Generation of PVMID

The TPS62150 is a synchronous step down DC-DC converter. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by using the DCS-Control™ topology. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High. It is mandatory to start with FSW = Low to limit inrush current, which can be done by connecting to VOUT or PG. To get a low ripple and full output current at the lower switching frequency, it is recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation if needed. A pull-down resistor of about 400 kΩ is internally connected to the pin.

The output voltage of the TPS62150 is adjustable. It can be programmed for output voltages from 0.9 to 6 V by using a resistive divider from V_{OUT} to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 5. It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_{13} = R_5 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{5}$$

with

- V_{OUT} = 6 V and V_{REF} = 800 mV
- R13 = 1 MΩ and R5 = 154 kΩ (see Figure 10).

For most applications, 10 µF will be sufficient and is recommended for the input capacitor, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply.

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{ss} \frac{2.5\ \mu A}{1.25\ V}\ [F] \tag{6}$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin and
- t_{SS} is the desired soft-start ramp time (seconds).

With C_{SS} = 3300pF, the soft-start time is 1.65 ms.

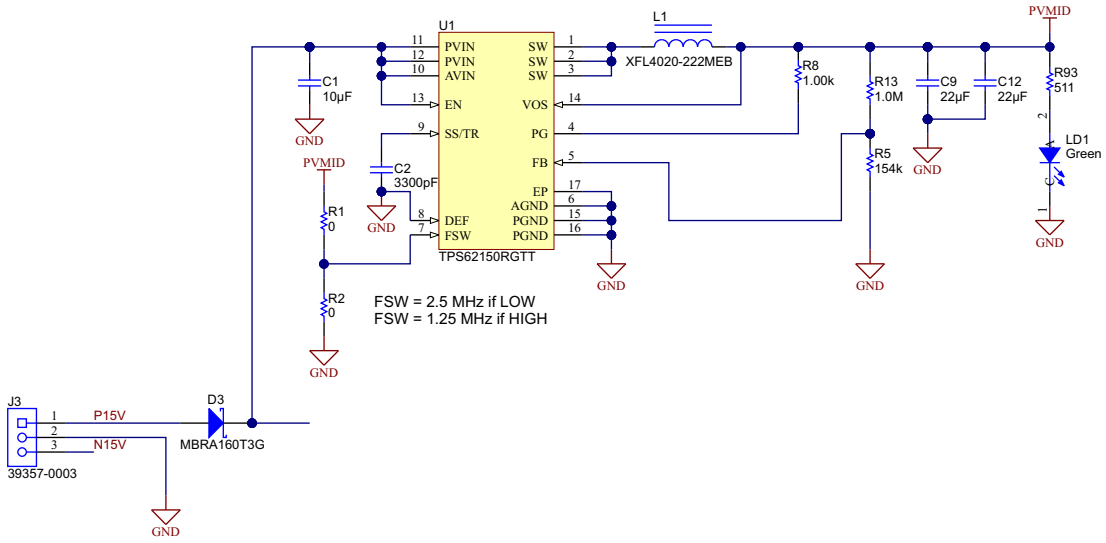


Figure 10. Generation of PVMID Using TPS62150

5.4 Generation of 5 V

From PVMID (which is equal to 6 V), it is required to generate 5 V to power the op-amps and voltage reference ICs. LP2992 is used to generate 5 V from PVMID as shown in Figure 11.

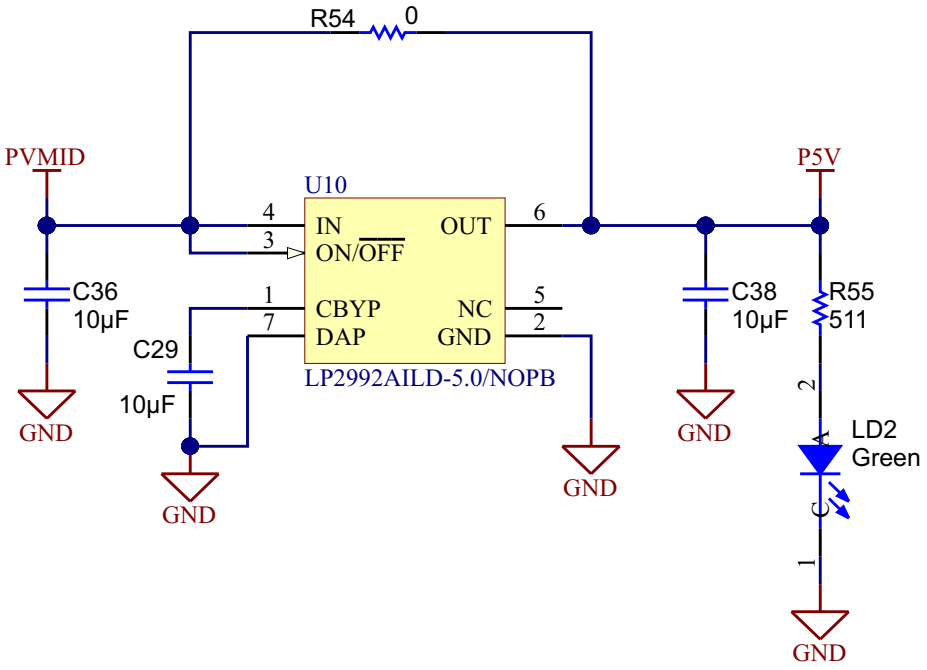


Figure 11. Generation of 5 V Using LP2992

NOTE: PVMID is currently set to 6 V and R54 is DNP. When LP2992 is not used, Mount R54 and set PVMID = 5 V.

5.5 Voltage Reference Circuit Design

Using external ADCs:
While using external ADCs (which are powered using a 5-V single supply), the reference voltage should be set to 2.5 V.

Using internal ADCs (of Delfino controller):
While using single-ended mode, the reference pin needs to be powered from a 3.3-V reference (Delfino converts 3.3 V into a 1.65-V reference internally). In case of the differential mode of internal ADC, the reference pin needs to be powered from a 2.5-V reference (Delfino converts 2.5 V into a 1.25-V reference internally).

To fulfill all these conditions, two reference devices are used. Figure 12 shows schematic section for REF2025 provides two reference voltages, 1.25 V and 2.5 V. The input to REF2025 is powered from 5 V. Both the reference outputs (2.5 V and 1.25 V) are provided with RC filters for any noise filtering.

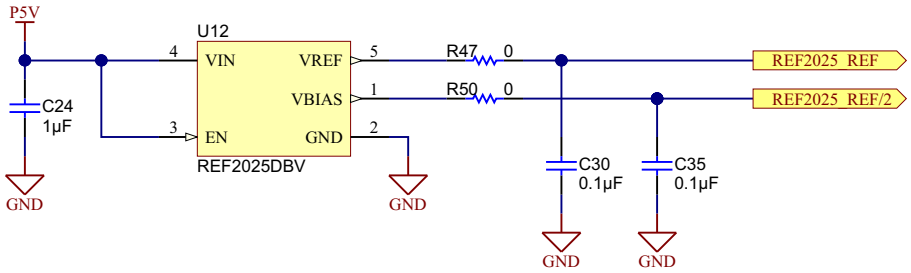


Figure 12. REF2025 Circuit to Provide 1.25 V and 2.5 V as Reference

Figure 13 shows schematic section for the REF2033 provides two reference voltages, 1.65 V and 3.3 V. The input to REF2033 is powered from 5 V. Both the reference outputs (1.65 V and 3.3 V) are provided with RC filters for any noise filtering.

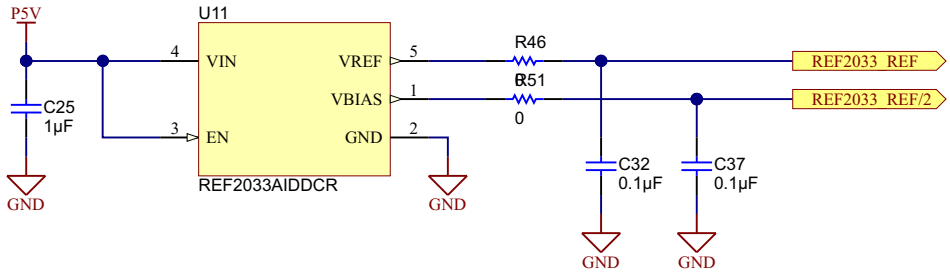


Figure 13. REF2033 Circuit to Provide 1.65 V and 3.3 V as Reference

5.6 Selecting the Filter Topology: MFB and SKF

The choice of a complex pole-pair circuit depends on performance requirements.

5.6.1 Multiple Feedback Topology

The MFB topology (sometimes called Infinite Gain or Rauch) is often preferred due to assured low sensitivity to component variations. The MFB topology creates an inverting second-order stage. In designs where an even number of stages are required, the output polarity will be the same as the input; this may not always be the case for filters employing the MFB because each stage brings about an output-to-input inversion. A typical MFB circuit is as shown in Figure 14.

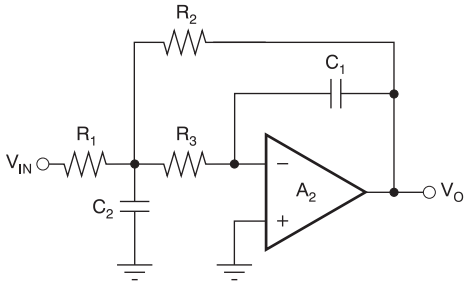


Figure 14. Multiple Feedback Filter Topology

5.6.2 Sallen-Key Topology

The Sallen-Key is a non-inverting circuit, which may make it preferable over the MFB, but this is not the only potential advantage. As a rule of thumb, the Sallen-Key topology is better if:

- Gain accuracy is important,
- A unity-gain filter is used, and
- Pole-pair Q is low (for example, Q < 3)

Figure 15 shows a typical Sallen-Key filter. At unity-gain, the Sallen-Key topology inherently has excellent gain accuracy. This is because the op-amp is used as a unity-gain buffer. With the MFB topology, gain is determined by the R2/R1 resistor ratio. The unity-gain Sallen-Key topology also requires fewer components—two resistors versus three for the MFB. The Sallen-Key topology may also be preferable for high-Q, high-frequency filter sections. In these sections, the value required for feedback capacitor in an MFB design can be quite low for reasonable resistor values. Low capacitor values can result in significant errors due to parasitic capacitance. The best filter design may be a combination of MFB and Sallen-Key sections.

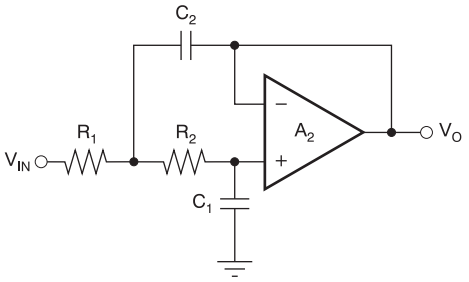


Figure 15. Sallen Key Filter Topology

5.7 Design of Unipolar AMP + Filter Stage

The following important points are observed while designing the unipolar signal conditioning circuit. Figure 16 shows the two-stage implementation of the same.

1. Single supply operation: The OPA2322 is powered through 5 V. One bypass capacitor of value 0.1 µF is placed very close to the AVDD pin of the OPA2322.
2. Output common-mode setting: The non-inverting pin of the op-amp is supplied with 2.5 V (coming from REF2025 REF) in case of interfacing with external ADC. But when the internal ADC of Delfino F2837x controller is used, the common-mode voltage needs to be 1.65 V. In that case, the external voltage on non-inverting pin of op-amp is supplied through 1.65 V (coming from REF2033 REF/2).
3. Unity gain buffer: The first stage of the OPA2322 is used to buffer the input signal.
4. Sallen key LPF: The second stage of the OPA2322 is connected as the Sallen Key Filter. The cut-off frequency of the filter is set to ~160 kHz, which is 10 times the maximum switching frequency of an IGBT inverter of industrial motor drive. The filter components are selected according to the Equation 7.

$$f = \frac{1}{2\pi \sqrt{C57 \times R42 \times C23 \times R26}} \quad (7)$$

With C57 = 200 pF, R42 = 9.76 kΩ, C23 = 100 pF, and R26 = 5.23 kΩ; the cut-off frequency is 157.518 kHz.

5. Selection of components: The 100-pF caps in the feedback helps in reducing overall noise of the system. One important thing to note that the resistors also have their internal noise. The resistor noise depends on the value of resistor. It is good to select the input and feedback resistor values in some kΩ (preferably < 5 kΩ) to reduce the effect of noise from resistors.
6. Input protection: The Hall sensor has a supply voltage of ±12 V. In case of any fault or short circuit condition, diodes D7 and D8 are used to clamp the input of op-amp to 5 V and GND, hence protecting the op-amp.

The output of unipolar signal condition circuit is connected to SMA jack J5 as well as it is connected to the input of Delfino F2837x control card.

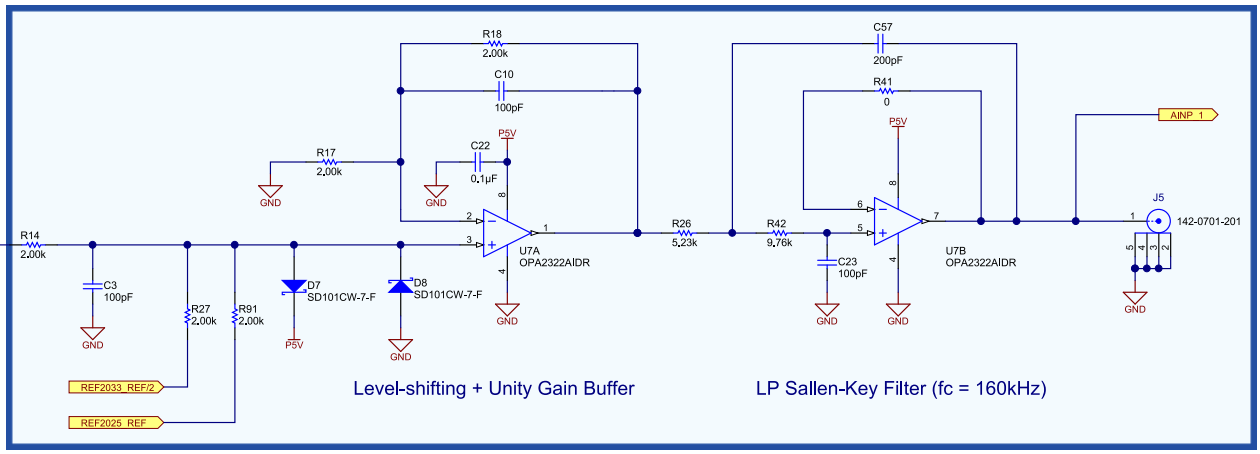


Figure 16. OPA2322 Interface Between Sensor and ADC

Figure 17 shows the TINA simulation for the schematic shown in Figure 16.

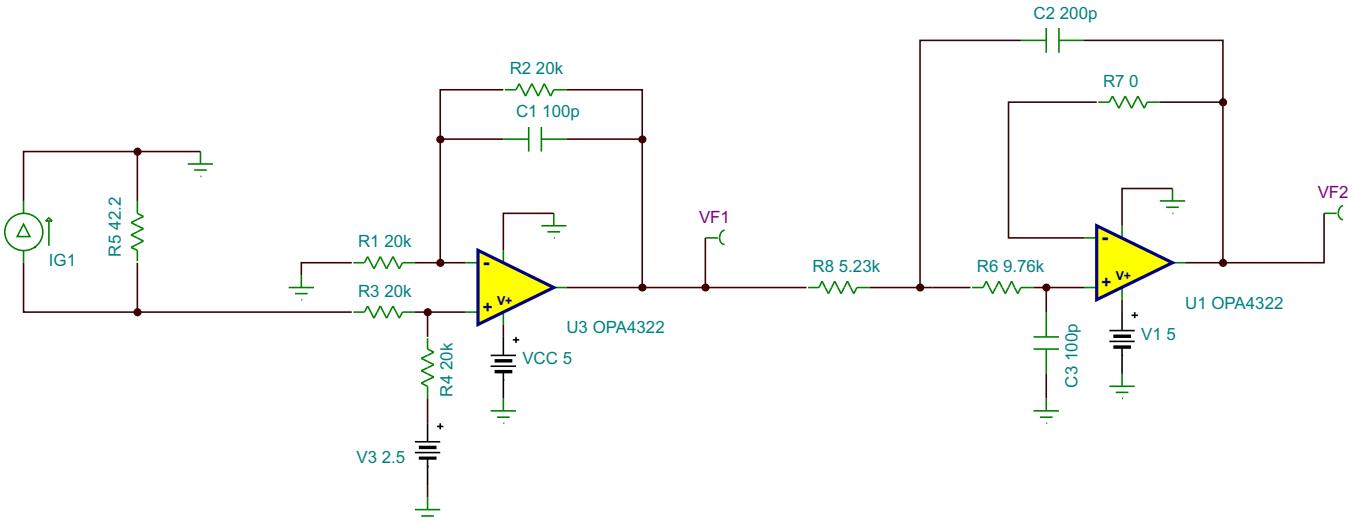


Figure 17. TINA Simulation for Unipolar Signal Conditioning Circuit

Figure 18 shows the simulated waveforms for Figure 17.

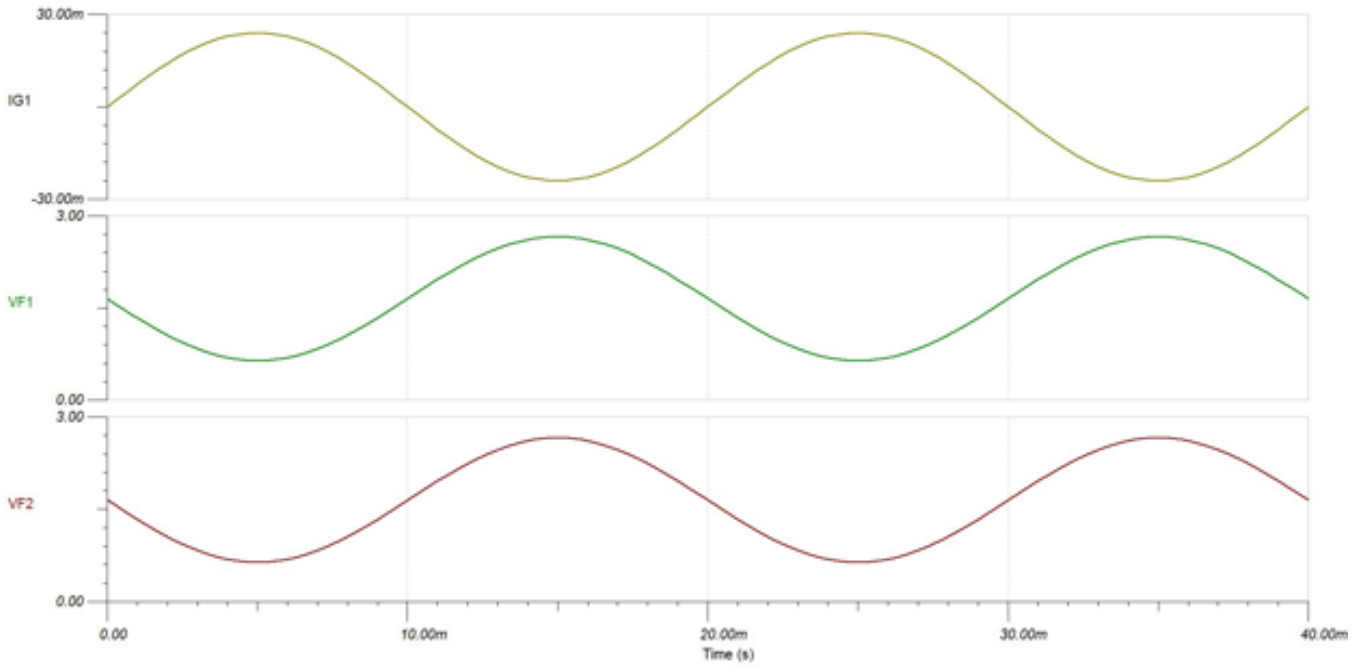


Figure 18. Waveforms for TINA Simulation

5.8 Design of Bipolar AMP + Filter Stage

The following important points are observed while designing the bipolar signal conditioning circuit. Figure 19 shows the two-stage implementation.

1. Dual supply operation: The OPA2192 is powered through ±12 V. One bypass capacitor of value 0.1 µF is placed very close to the AVDD pin and AVSS pin of the OPA2192.
2. Unity gain buffer: The first stage of the OPA2192 is used to buffer the input signal.
3. Multiple feedback LPF: The second stage of the OPA2192 is connected as the multiple feedback filter. The cut-off frequency of the filter is set to ~160 kHz, which is 10 times the maximum switching frequency of an IGBT inverter of industrial motor drive. The filter components are selected according to Equation 8.

$$f = \frac{1}{2\pi \sqrt{C14 \times R34 \times C19 \times R35}} \quad (8)$$

With C14 = 2700 pF, R34 = 673 Ω, C19 = 470 pF, and R35 = 1.15 kΩ; the cut-off frequency is 160.595 kHz.

4. Selection of components: The 100-pF caps in the feedback helps in reducing overall noise of the system. One important thing to note that the resistors also have their internal noise. The resistor noise depends on the value of resistor. Select the input and feedback resistor values in some kΩ (preferably < 5 kΩ) to reduce the effect of noise from resistors.
5. Output common-mode setting: The output common-mode voltage is set by setting up bias in filter stage. The non-inverting pin of the filter stage is supplied with 2.5 V (coming from the REF2025 REF) in case of interfacing with external ADC. But when the internal ADC of Delfino F2837x controller is used, the common-mode voltage needs to be 1.65 V. In that case, the external voltage on non-inverting pin of op-amp is supplied through 1.65 V (coming from the REF2033 REF/2).

The output of bipolar signal condition circuit is connected to SMA jack J5 as well as it is connected to the input of Delfino F2837x control card.

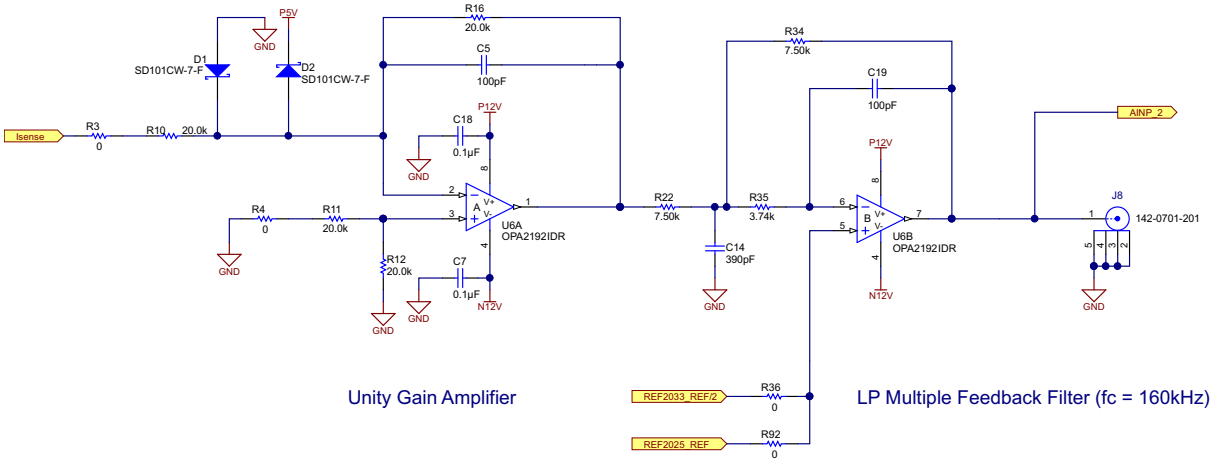


Figure 19. OPA2192 Interface Between Sensor and ADC

Figure 20 shows the TINA Simulation for the schematic shown in Figure 19.

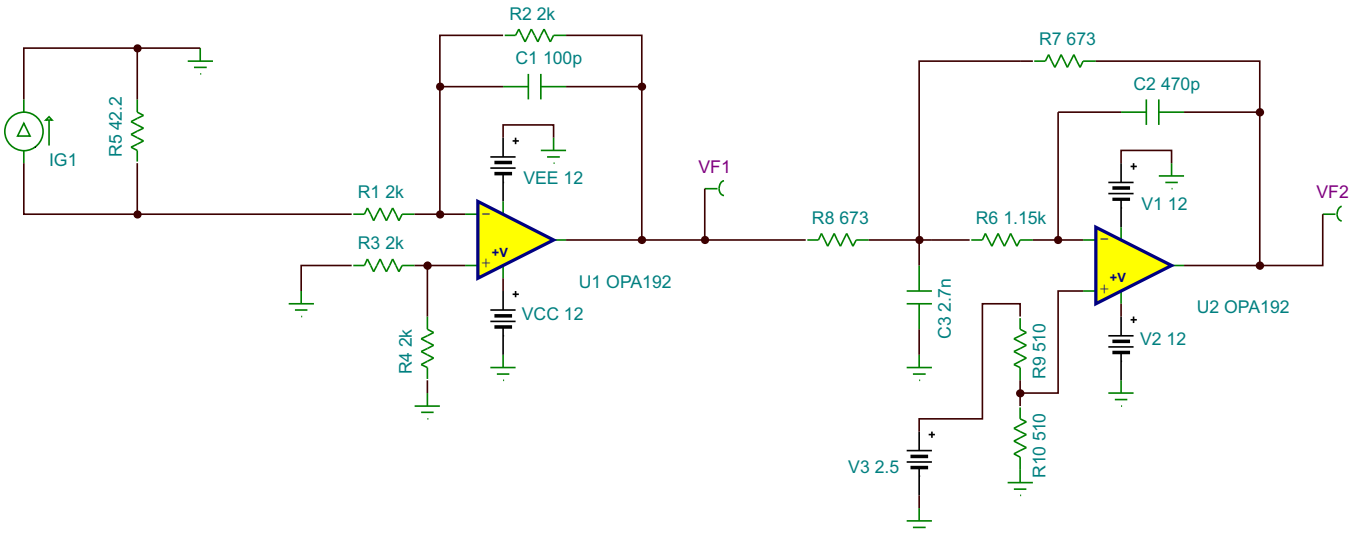


Figure 20. TINA Simulation for Bipolar Signal Conditioning Circuit

Figure 21 shows the simulated waveforms for Figure 20.

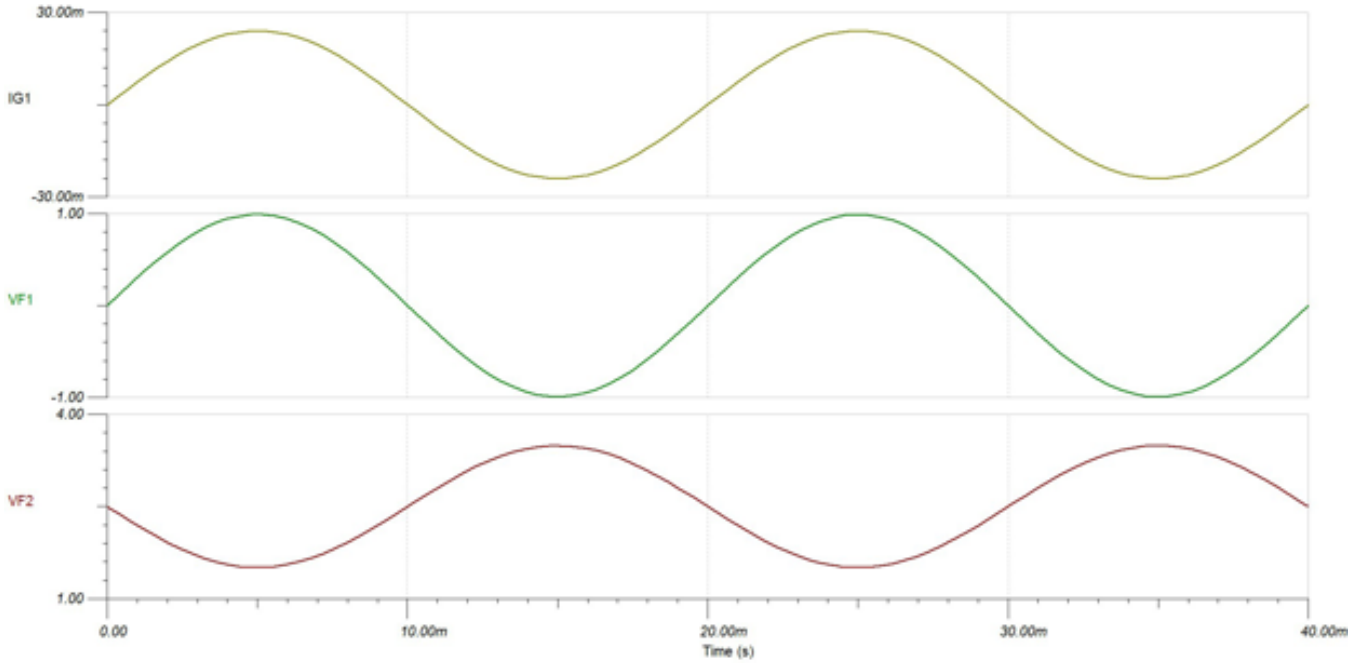


Figure 21. Waveforms for TINA Simulation

5.9 Design of Overcurrent Detection Circuit

In industrial motor drives, it is very common to use the sensor up to 200% of its rating. If the current goes beyond 200%, the protection mechanism should be enabled. In this design, the thresholds are calculated as follows:

- Nominal current rating (In) = 8 A
- Corresponding nominal output current = 24 mA (from Figure 7)
- Maximum current rating = 18 A (which is 225% of the nominal primary current)
- Corresponding nominal output current = 54 mA (from Figure 7)
- Corresponding output voltage = 2.25 V (with burden resistor = 42.2 Ω)

The overcurrent protection is implemented as shown in Figure 22. The comparators used in the protection circuits are open-drain outputs. The pull-up resistors are connected to 3.3 V (which is typically equal to digital supply of the microcontroller or any other motor controller) so that the high and low levels of the comparator outputs are within the sensing range of the controller.

The resistor divider to generate the thresholds is calculated for VTH (pos) = 2.25 V and VTH (neg) = –2.25 V.

The calculated value of VTH (pos) and VTH (neg) are as given in Equation 9 and Equation 10, respectively.

$$\text{VTH}\left(\text{pos}\right) = \frac{\left\{12-\left(-12\right)\right\}\times\left(43.2\text{ k}+20\text{ k}\right)}{43.2\text{ k}+20\text{ k}+43.2\text{ k}} = 14.2556\text{ V} = 2.2556\text{ V for 12 V} \tag{9}$$

$$\text{VTH}\left(\text{neg}\right) = \frac{\left\{12-\left(-12\right)\right\}\times 43.2\text{ k}}{43.2\text{ k}+20\text{ k}+43.2\text{ k}} = 9.744\text{ V} = -2.2566\text{ V for }-12\text{ V} \tag{10}$$

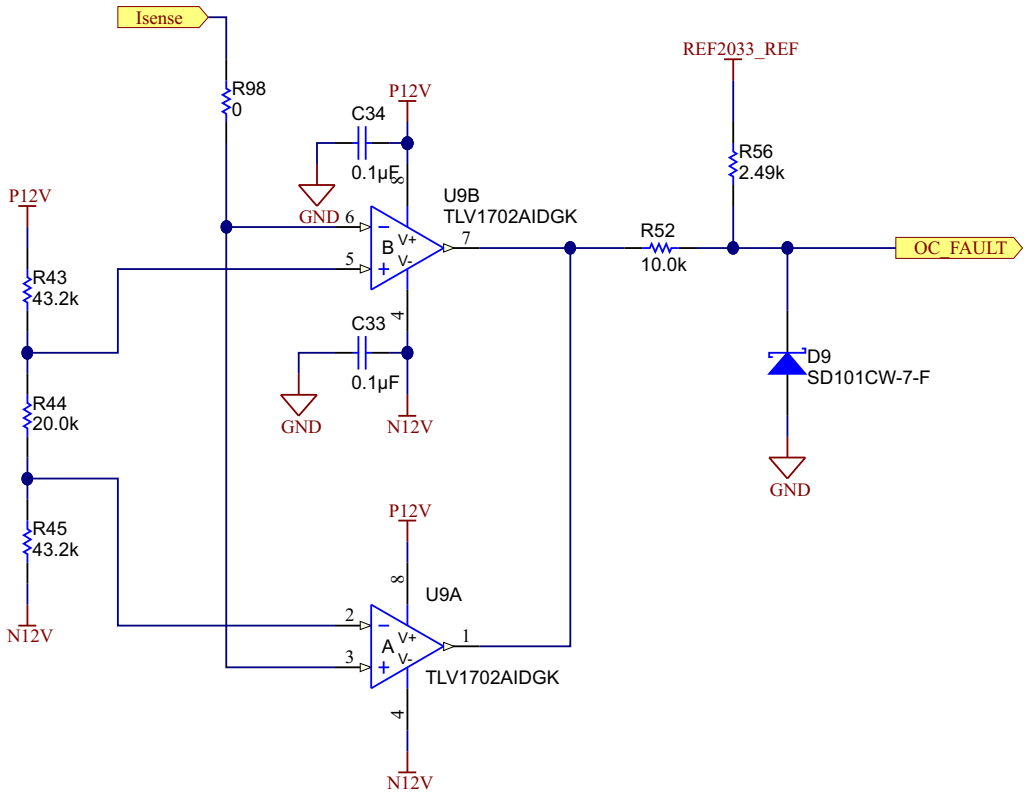


Figure 22. Overcurrent Protection Using TLV1702

5.10 Connection to the Delfino F2837x Control Card

The Delfino F28377D Control Card (TMDSCNCD28377D) from TI provides a great way to learn and experiment with the F2837x device family within TI's C2000™ family of MCUs. This 180-pin control card is intended to provide a well-filtered robust design capable of working in most Industrial environments.

F28377D Control Card features:

- Delfino F28377D MCU: This high performance C2000 MCU is located on the control card.
- 180-pin HSEC8 Edge Card Interface: This interface llows for compatibility with all of C2000's 180-pin control card application kits and control cards. Compatibility with 100-pin control cards can be accomplished using the TMDSADAP180TO100 adapter card (sold separately).
- Built-in Isolated JTAG Emulation: An XDS100v2 emulator provides a convenient interface to Code Composer Studio (CCS) without additional hardware. Flipping a switch allows an external JTAG emulator to be used.
- Connectivity: The control card contains connectors that allow the user to experiment with USB, a microSD card, and isolated UART/SCI with the F2837x MCU.
- Key Signal Breakout: Most GPIO, ADC, and other key signals routed to hard gold connector fingers.
- Robust Power Supply Filtering: A single 5-V input supply powers an on-card 3.3-V LDO. All MCU inputs are then decoupled using LC filters near the device.
- ADC Clamping: ADC inputs are clamped by protection diodes.

An image of the control card is shown in the Figure 23:

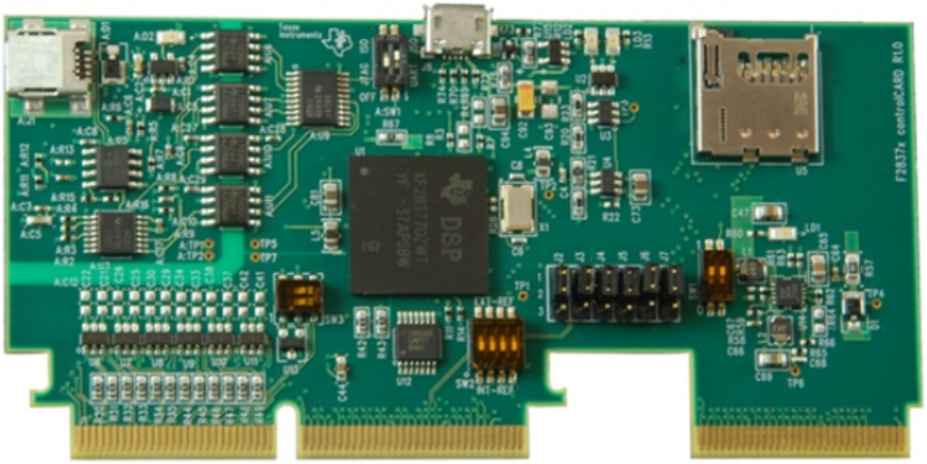


Figure 23. Image of Delfino F2837x Control Card

Pin-mapping for the Delfino F2837x Control Card

Figure 24 shows the pin-mapping for 180-pin connector available on the Delfino F2837x Control Card. The signals are routed as shown in Table 4.

Table 4. Pin-Mapping Details

PIN NUMBER ON CONTROL CARD	PIN FUNCTIONALITY	MAPPING ON TIDA-00316 BOARD (J10 AND J11)
7, 10, 19, 22, 35, 38, 43, 46, 47, 65, 83, 97, 111, 135, 157, 179	GND	GND
11	ADC-A1, DAC	REF2025_REF/2 and REF2033_REF/2
15	ADC-A2, COMP+	AINP-1
17	ADC-A3	AINP-2
45	All VREFHIs	REF2025_REF and REF2033_REF
48, 84, 98, 112, 158, 180	AVDD	AVDD (PVMID)

Date:				cCARD Pinout:		F28377D (180pin)				HSEC Pinout:
7-May-2014										2.10
		HSEC pin	MCU pin	HSEC function		HSEC function	MCU pin	HSEC pin		
		1	GPIO-71 **	JTAG-EMU1		JTAG-EMU0	GPIO-70 **	2		
		3	TMS	JTAG-TMS		JTAG-TRSTn	TRSTn	4		
		5	TCK	JTAG-TCK		JTAG-TDO	TDO	6		
		7		GND		JTAG-TDI	TDI	8		
		9	ADC-A0, DAC	ADC1 (and/or DACA)		GND		10		
		11	ADC-A1, DAC	ADC1 (and/or DACB)		ADC2	ADC-B0	12		
		13		Rsvd		ADC2	ADC-B1	14		
		15	ADC-A2, COMP+	ADC1 (and/or CMPIN+)		Rsvd		16		
		17	ADC-A3	ADC1		ADC2	ADC-B2, COMP+	18		
		19		GND		ADC2	ADC-B3	20		
		21	ADC-A4, COMP+	ADC1 (and/or CMPIN+)		GND		22		
		23	ADC-A5	ADC1		ADC2	ADC-B4, COMP+	24		
		25	ADCIN14, COMP+	ADC (and/or CMPIN+)		ADC2	ADC-B5	26		
		27	ADCIN15	ADC		ADC	ADC-D0, COMP+	28		
		29		Rsvd		ADC	ADC-D1	30		
		31	ADC-C2, COMP+	ADC		Rsvd		32		
		33	ADC-C3	ADC		ADC	ADC-D2, COMP+	34		
		35		GND		ADC	ADC-D3	36		
		37	ADC-C4	ADC		GND		38		
		39	ADC-C5	ADC		ADC	ADC-D4	40		
		41		Rsv		ADC	ADC-D5	42		
		43		A-GND (VREFLO on certain MCU)		Rsv		44		
		45	All VREFHIs *	Rsv (VREFHI on certain MCU)		GND		46		
		47		GND		5V0		48		
		49	GPIO-00	PWM1A		PWM3A	GPIO-04	50		
		51	GPIO-01	PWM1B		PWM3B	GPIO-05	52		
		53	GPIO-02	PWM2A		PWM4A	GPIO-06	54		
		55	GPIO-03	PWM2B		PWM4B	GPIO-07	56		
		57	GPIO-08	PWM5A		PWM7A or TZ1	GPIO-12	58		
		59	GPIO-09	PWM5B		PWM7B or TZ2	GPIO-13	60		
		61	GPIO-10	PWM6A		PWM8A or TZ3	GPIO-14	62		
		63	GPIO-11	PWM6B		PWM8B or TZ1/4	GPIO-15	64		
		65		GND		12V0?		66		
		67	GPIO-16	SPISIMOA		QEP1A (McBSP-MDXA)	GPIO-20	68		
		69	GPIO-17	SPISOMIA		QEP1B (McBSP-MDRA)	GPIO-21	70		
		71	GPIO-18	SPICLKA		QEP1S (McBSP-MFSXA)	GPIO-22	72		
		73	GPIO-19	SPISTEA		QEP1I (McBSP-MCLKXA)	GPIO-23	74		
		75	GPIO-24	ECAP1 or SPISIMOB		SCIRXA	GPIO-28	76		
		77	GPIO-25	ECAP2 or SPISOMIB		SCITXA	GPIO-29	78		
		79	GPIO-26	ECAP3 or SPICLKB		CANRXA	GPIO-30	80		
		81	GPIO-27	ECAP4 or SPISTEB		CANTXA	GPIO-31	82		
		83		GND		5V0		84		
		85	GPIO-32	I2CSDAA		GPIO	GPIO-34	86		
		87	GPIO-33	I2CSCLA		GPIO	GPIO-39	88		
		89	GPIO-40	GPIO		GPIO	GPIO-44	90		
		91	GPIO-41	GPIO		GPIO	GPIO-45	92		
		93	GPIO-42 ***	GPIO		GPIO	GPIO-46 ***	94		
		95	GPIO-43 ***	GPIO		GPIO	GPIO-47 ***	96		
		97		GND		5V0		98		
		99	GPIO-48	GPIO		QEP2A or GPIO	GPIO-54	100		
		101	GPIO-49	GPIO		QEP2B or GPIO	GPIO-55	102		
		103	GPIO-50	GPIO		QEP2S or GPIO	GPIO-56	104		
		105	GPIO-51	GPIO		QEP2I or GPIO	GPIO-57	106		
		107	GPIO-52	GPIO		GPIO (McBSP-MCLKRA)	GPIO-58	108		
		109	GPIO-53	GPIO		GPIO (McBSP-MFSRA)	GPIO-59	110		
		111		GND		5V0		112		
		113		Rsv		Rsv		114		
		115		Rsv		Rsv		116		
		117		Rsv		Rsv		118		
		119		Rsv		Device Reset (Active low)	XRSn	120		
		121	GPIO-35	GPIO		GPIO	GPIO-36	122		
		123	GPIO-37	GPIO		GPIO	GPIO-38	124		
		125	GPIO-60	GPIO		GPIO	GPIO-61	126		
		127	GPIO-62	GPIO		GPIO	GPIO-63	128		
		129	GPIO-64	GPIO		GPIO	GPIO-65	130		
		131	GPIO-66	GPIO		GPIO	GPIO-67	132		
		133	GPIO-68	GPIO		GPIO	GPIO-69	134		
		135		GND		12V0?		136		
		137	GPIO-70	GPIO		GPIO	GPIO-71	138		
		139	GPIO-72	GPIO		GPIO	GPIO-73	140		
		141	GPIO-74	GPIO		GPIO	GPIO-75	142		
		143	GPIO-76	GPIO		GPIO	GPIO-77	144		
		145	GPIO-78	GPIO		GPIO	GPIO-79	146		
		147	GPIO-80	GPIO		GPIO	GPIO-81	148		
		149	GPIO-82	GPIO		GPIO	GPIO-83	150		
		151	GPIO-84	GPIO		GPIO	GPIO-85	152		
		153	GPIO-86	GPIO		GPIO	GPIO-87	154		
		155	GPIO-88	GPIO		GPIO	GPIO-89	156		
		157		GND		5V0		158		
		159	GPIO-90	GPIO		GPIO	GPIO-91	160		
		161	GPIO-92	GPIO		GPIO	GPIO-93	162		
		163	GPIO-94	GPIO		GPIO	GPIO-133	164		
		165	GPIO-120 ***	GPIO		GPIO	GPIO-121 ***	166		
		167	GPIO-161	GPIO		GPIO	GPIO-162	168		
		169	GPIO-163	GPIO		GPIO	GPIO-164	170		
		171		Rsv		Rsv		172		
		173		Rsv		Rsv		174		
		175		Rsv		Rsv		176		
		177		Rsv		12V0?		178		
		179		GND		5V0		180		

Analog (HSEC pin 9 – 45)

Analog (HSEC pin 10 – 46)

Digital (HSEC pin 49 – 119)

Digital (HSEC pin 50 – 120)

* Switches may be altered to connect VREFHIs to the HSEC connector

** 0ohm resistors can be removed in order to tie GPIO-70 and 71 to EMU0 and EMU1

*** Can be dedicated to on-card USB or brought through the connector via jumpers on the cCARD

Figure 24. Pin Mapping on Delfino F2837x Control Card (180-Pin Connector)

Figure 25 shows the schematic capture for the pin-mapping explained in Table 4. Although the control card has clamping diodes at each of the analog inputs, this design provides an option to mount external clamping diodes as well.

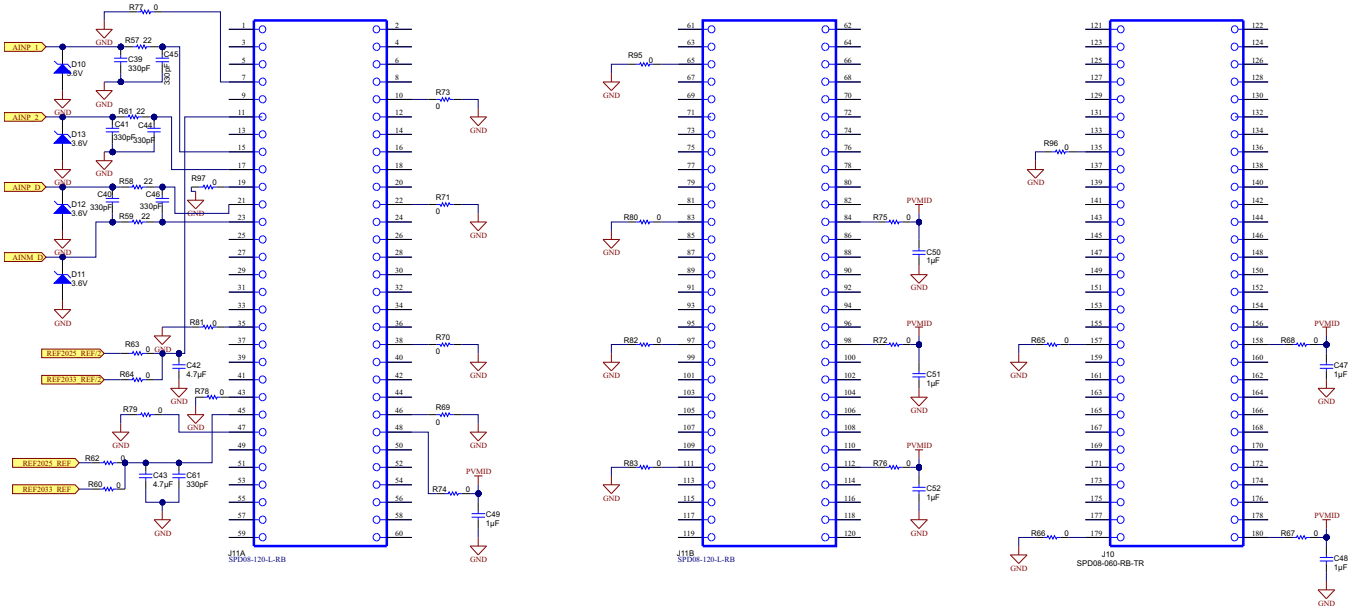


Figure 25. Schematic Capture for J10 and J11 (to be Connected to 180-Pin Connector on Control Card)

NOTE: The control card can be powered through the onboard 6 V (that is, PVMID) or using an external 5 V from USB. When an external USB connection is used for powering the control card, disconnect the PVMID voltage by removing the corresponding resistors (shown in Figure 25).

The output of the bipolar signal conditioning circuit is connected to Channel A3 of the internal ADC of Delfino controller and the output of the unipolar signal conditioning circuit is connected to Channel A2 of the ADC. As shown in Figure 25, the inputs are provided with RC filters for anti-aliasing purposes.

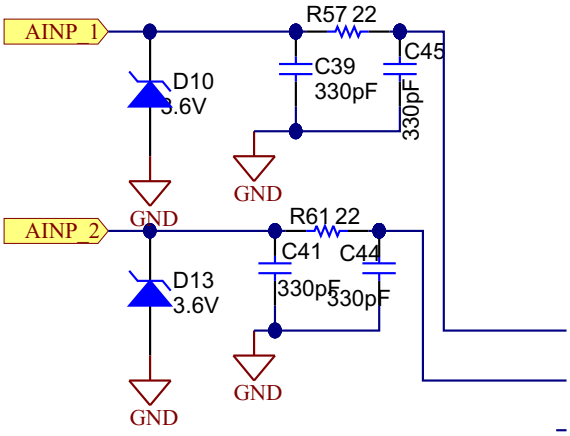


Figure 26. Filtering for ADC Inputs

The references are connected to VREFHI inputs on the 180-pin control card connector as shown in Figure 27.

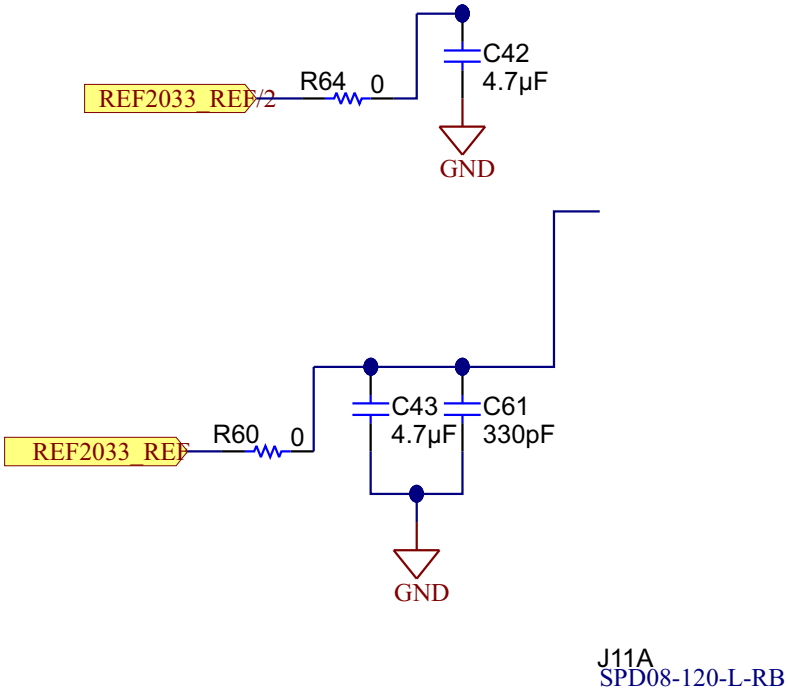


Figure 27. Reference and Common-Mode Voltage

5.11 Connectors to Connect With External Motor Controller

As shown in Figure 28, two connectors J12 and J4 are provided on the board with all the signals (outputs of signal conditioning circuits, reference voltages, and so on) so as to interface with external motor controller. Also, the overcurrent fault signal is available on connector J9.

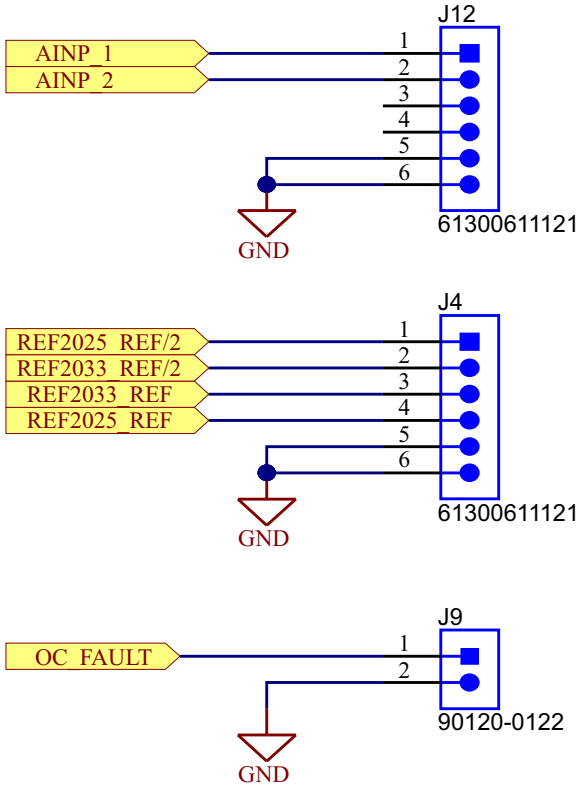


Figure 28. Connectors to Interface With External Motor Controller

6 Test Setup

Figure 29 shows the setup used for AC and DC performance measurements for this reference design.

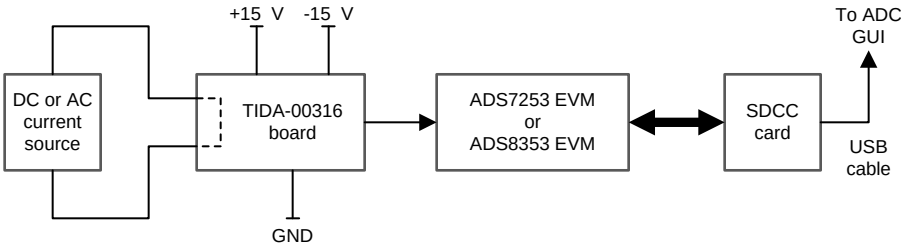


Figure 29. Test Setup for AC and DC Tests Using ADS7253/ADS8353

7 Test Data

7.1 Power Supply and Reference Circuit Functionality Tests

Table 5. Power Supply Rails

	RAIL	DESIGNED FOR (V)	MEASURED VALUE (V)
POWER SUPPLY	PVMID	6	6.0304
	P5V	5	4.9593
	P12V	12	11.9248
	N12V	–12	–11.8757
REFERENCES	REF2033_REF	3.3	3.2999
	REF2033_REF/2	1.65	1.6501
	REF2025_REF	2.5	2.5001
	REF2025_REF/2	1.25	1.2502

Figure 30 shows the output of the TPS62150 set at 6 V.

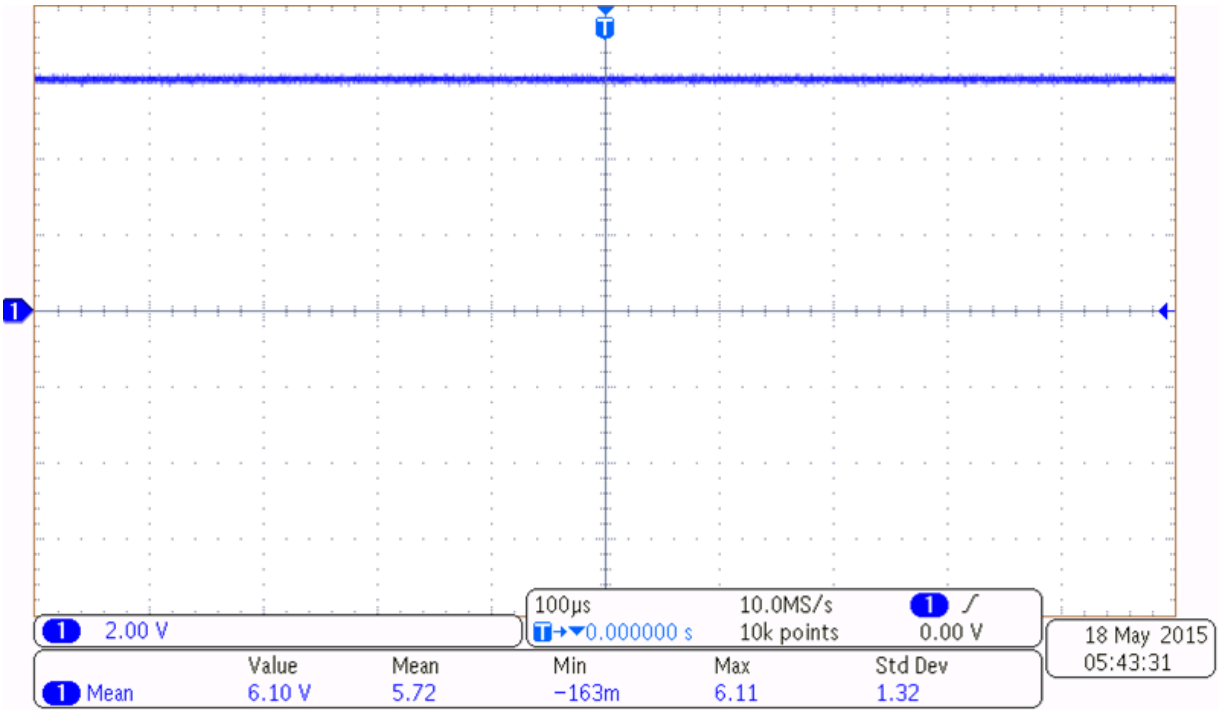


Figure 30. 6-V Signal From TPS62150

The ripple measured on the same 6 V is shown in Figure 31. The ripple value is 100 mV.

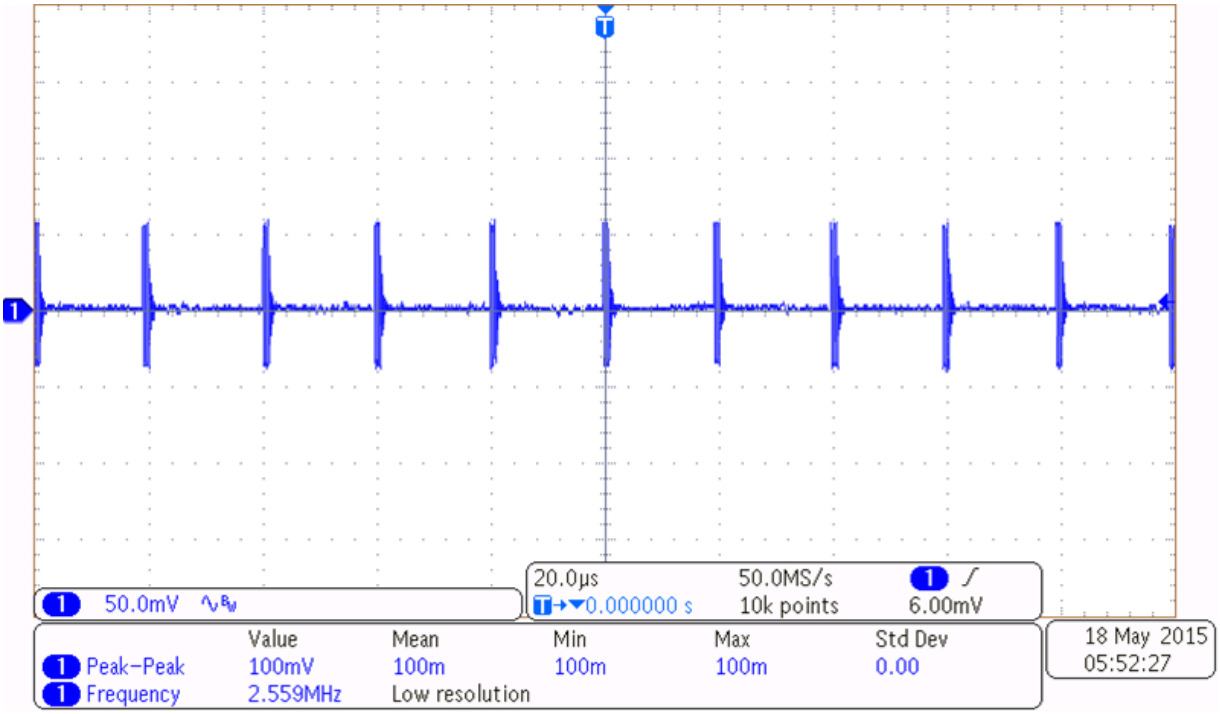


Figure 31. Ripple on 5-V Signal

Figure 32 shows the 5-V supply voltage generated using the LP2992.

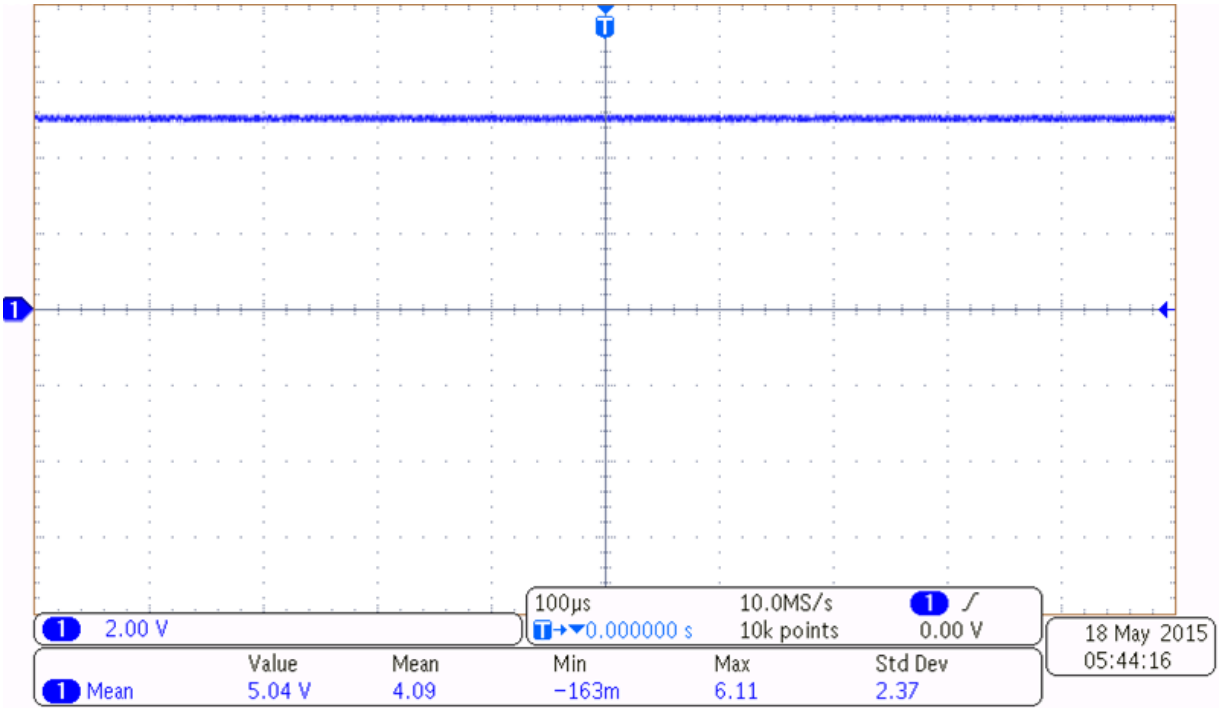


Figure 32. 5-V Signal Generated by LP2992

The ripple measured on the same 5 V is shown in Figure 33. The ripple value is much less than 10 mV. (The signal captured in Figure 33 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much lesser than what is seen.)

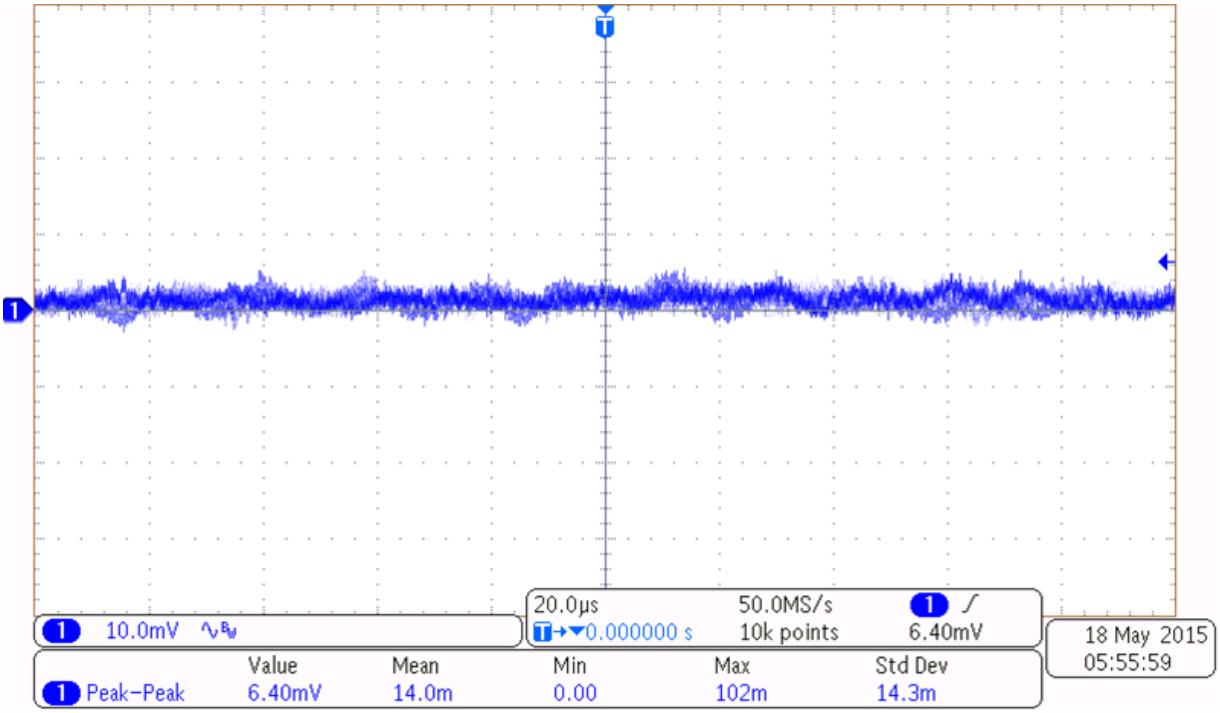


Figure 33. Ripple on 5-V Signal

Figure 34 shows the output of the TPS7A4901 set at 12 V.

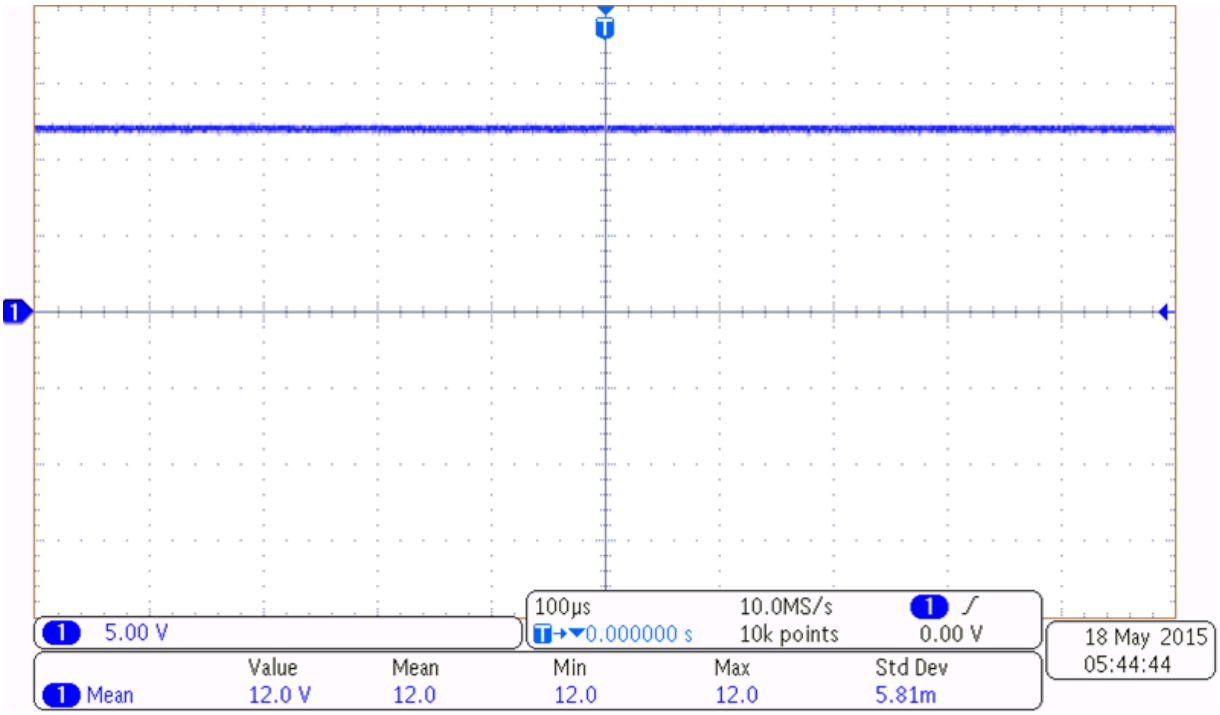


Figure 34. 12-V Signal From TPS7A4901

The ripple measured on the same 12 V is shown in Figure 35. The ripple value is less than 10 mV. (The signal captured in Figure 35 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much lesser than what is seen.)

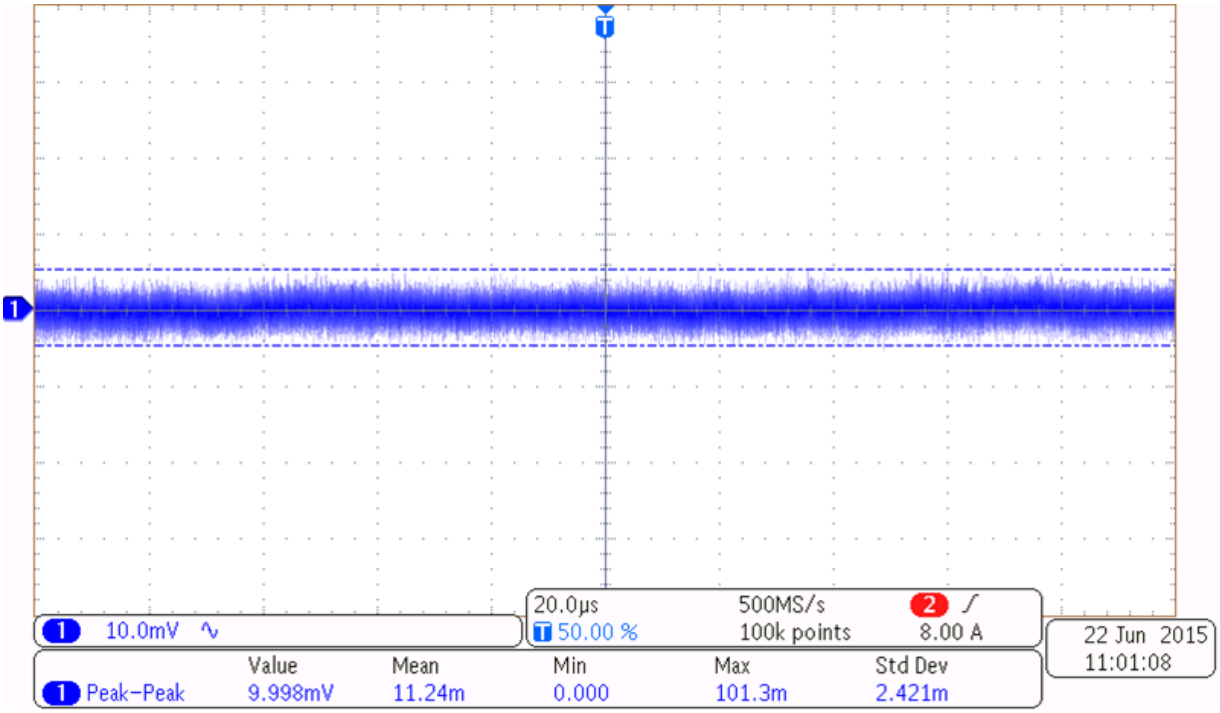


Figure 35. Ripple on 12-V Signal

Figure 36 shows the output of the TPS7A3001 set at –12 V.

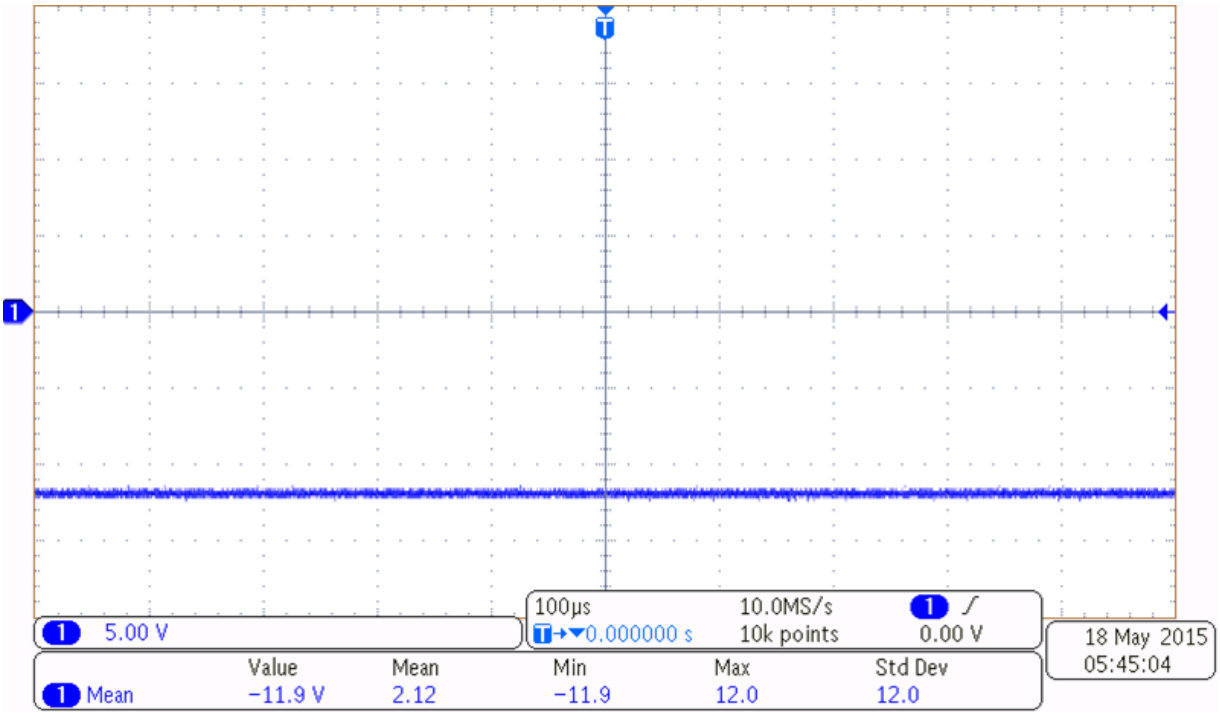


Figure 36. –12-V Signal From TPS7A3001

The ripple measured on the same –12 V is shown in Figure 37. The ripple value is much less than 10 mV. (The signal captured in Figure 37 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much lesser than what is seen.)

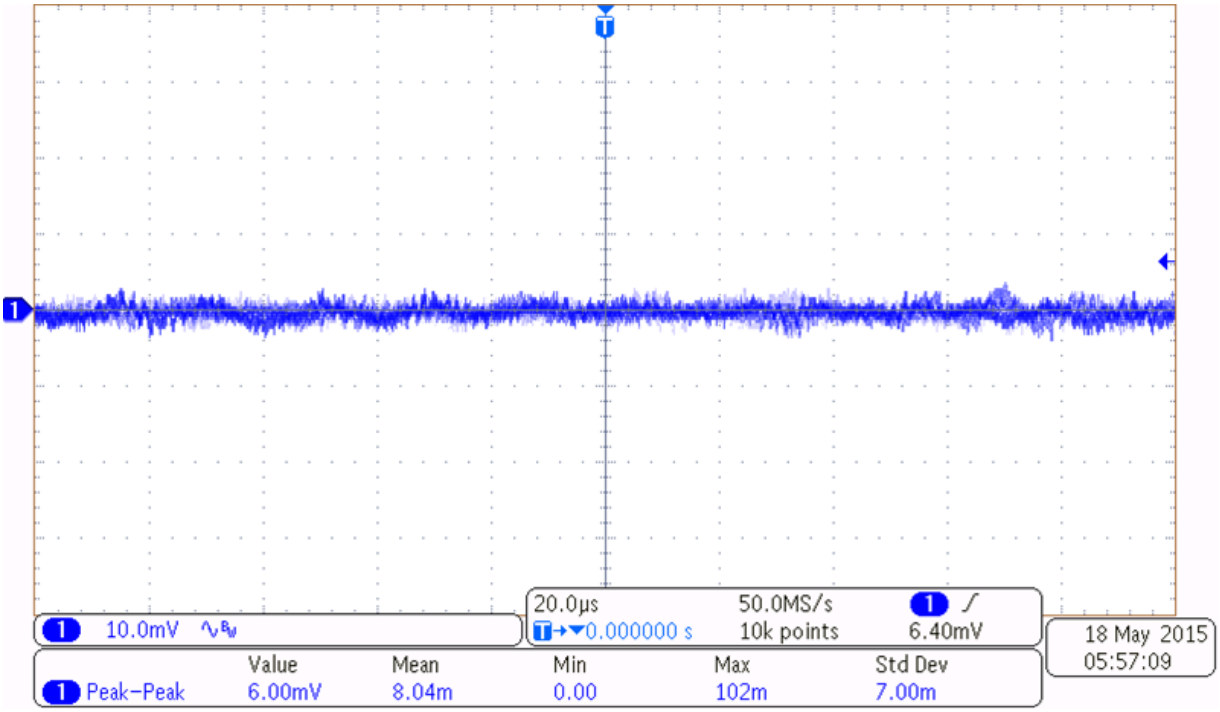


Figure 37. Ripple on –12-V Signal

Figure 38 and Figure 39 show the two outputs of REF2025 set internally at 2.5 V and 1.25 V, respectively.

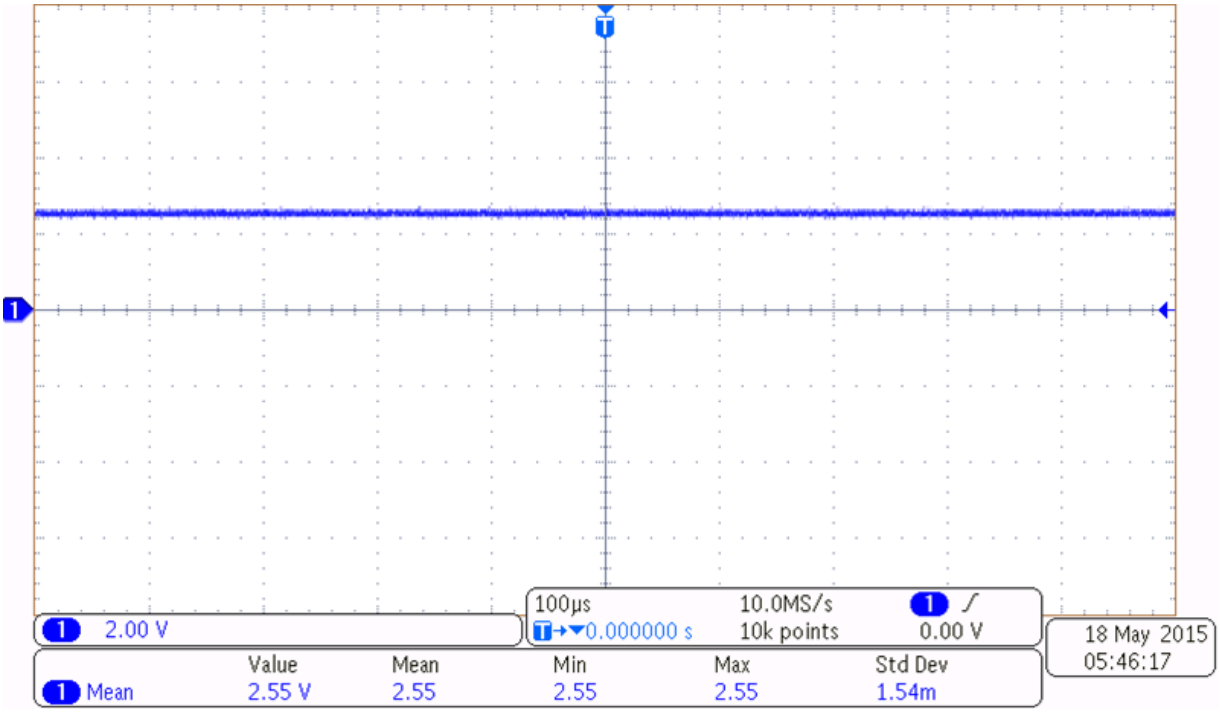


Figure 38. 2.5-V Reference Signal Generated by REF2025

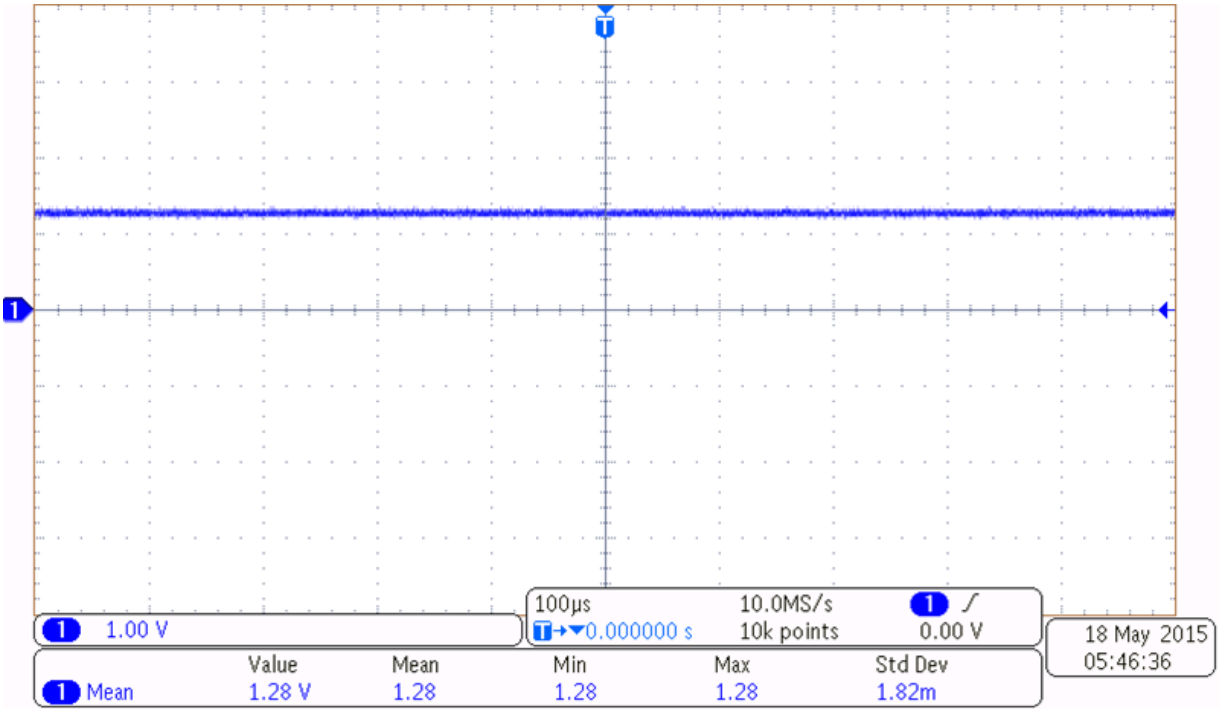


Figure 39. 1.25-V Reference Signal Generated by REF2025

Figure 40 and Figure 41 show the two outputs of the REF2033 set internally at 3.3 V and 1.65 V, respectively.

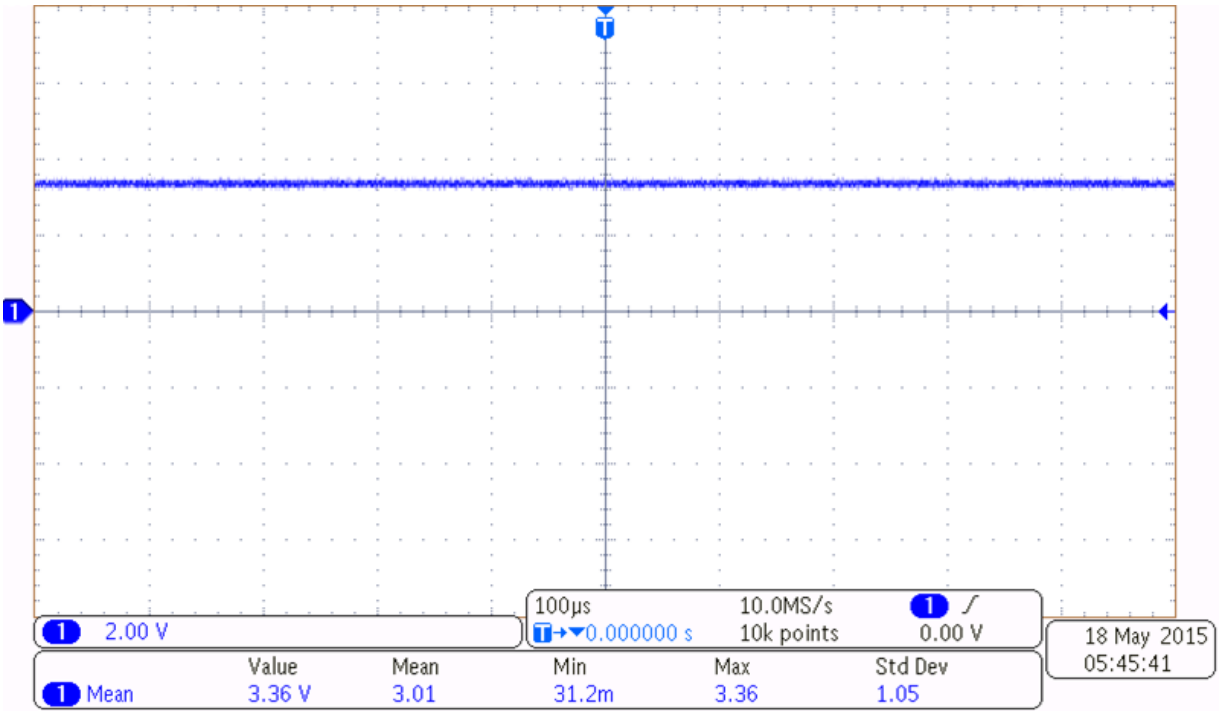


Figure 40. 3.3-V Reference Signal Generated by REF2033

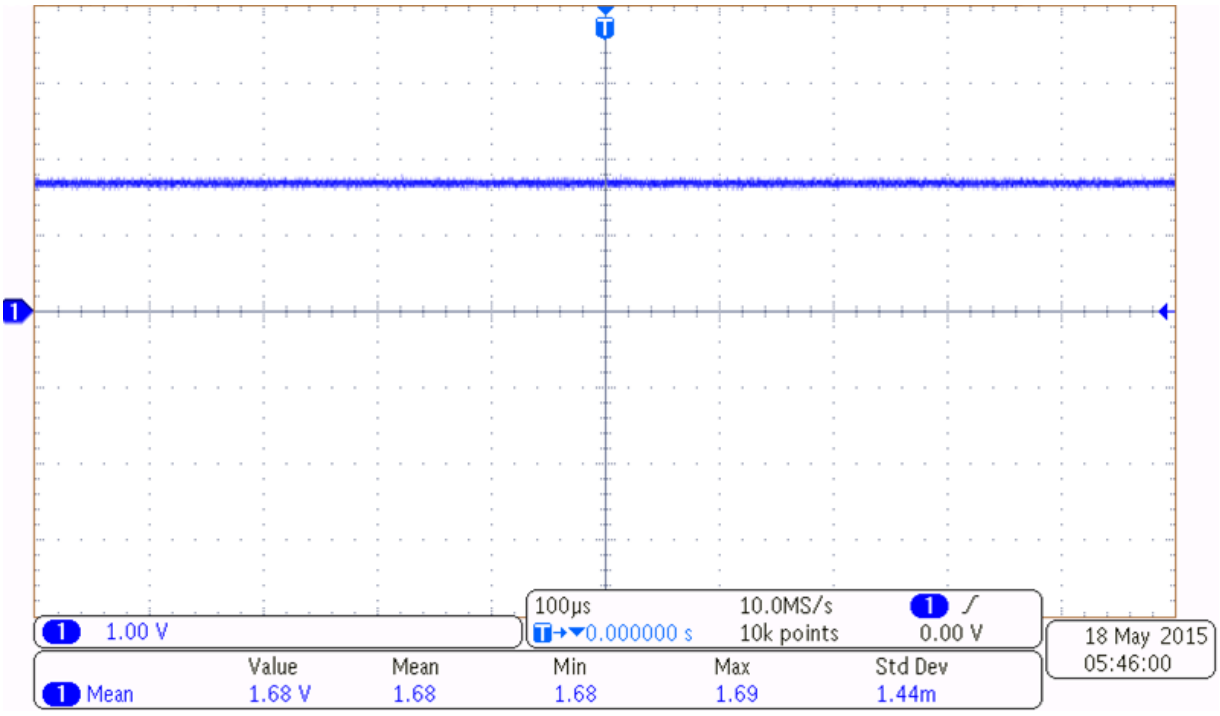


Figure 41. 1.65-V Reference Signal Generated by REF2033

7.2 Power Consumption of the Board Under Different Test Conditions

Table 6 shows the power consumption of the TIDA-00316 board under different test conditions.

Table 6. Power Consumption Test Data

1	TIDA-00316 BOARD POWERED UP WITH ±15 V (NO CURRENT PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.057	Iin–	0.016		
	Pin+	0.854829	Pin–	0.24	Total power	1.094829
2	TIDA-00316 BOARD POWERED UP WITH ±15 V AND 8 A PASSING THROUGH THE HALL SENSOR					
	Vin+	14.997	Vin–	15.001		
	Iin+	0.099	Iin–	0.017		
	Pin+	1.484703	Pin–	0.255017	Total power	1.73972
3	TIDA-00316 BOARD POWERED UP WITH ±15 V AND –8 A PASSING THROUGH THE HALL SENSOR					
	Vin+	14.997	Vin–	15		
	Iin+	0.054	Iin–	0.038		
	Pin+	0.809838	Pin–	0.57	Total power	1.379838
4	TIDA-00316 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (NO CURRENT PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.126	Iin–	0.014		
	Pin+	1.889622	Pin–	0.21	Total power	2.099622
5	TIDA-00316 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (8 A PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.167	Iin–	0.015		
	Pin+	2.504499	Pin–	0.225	Total power	2.729499
6	TIDA-00316 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (–8 A PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.121	Iin–	0.037		
	Pin+	1.814637	Pin–	0.555	Total power	2.369637

7.3 DC Performance Tests

For any signal conditioning circuit, it is important to know the DC accuracy and performance. Note that in a typical drive application, the current sensor would be used from 30% to 100% of its nominal current rating so the accuracy should be considered for primary current from ±2 A to ±8 A for LAH 25-NP.

7.3.1 DC Performance of Bipolar Signal Conditioning Circuit

For analyzing the DC performance of the bipolar signal conditioning circuit, the ADS7253EVM and ADS8353EVM (for 12-bit and 16-bit performance, respectively) are used along with the TIDA-00316 boards as shown in Figure 29. The DC accuracy is measured at each of the stages:

- On TIDA-00316 board:
  - Sensor output
  - Output of op-amp
  - Output of Sallen-key Filter
- On ADC board:
  - Input of ADC
  - Output data on ADC GUI

7.3.1.1 DC Performance of Bipolar Signal Chain (Amplifier + Filter + ADC)

The DC accuracy is observed for the bipolar signal chain. Figure 42 and Figure 43 show the two accuracy graphs for the negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

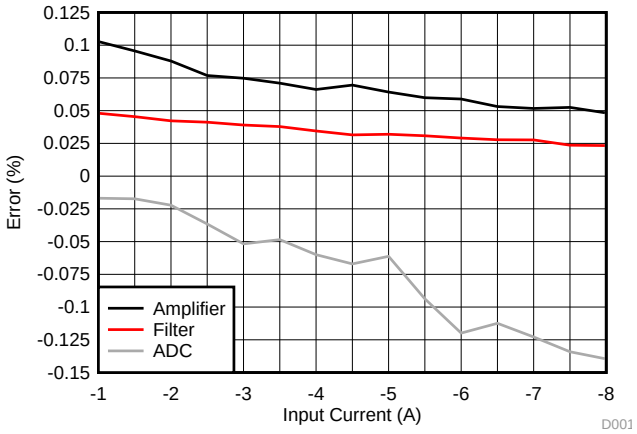


Figure 42. Bipolar Signal Chain DC Accuracy (for Negative Input Current Range)

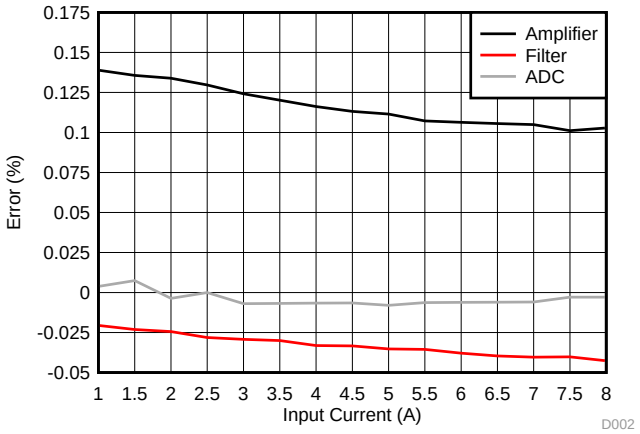


Figure 43. Bipolar Signal Chain DC Accuracy (for Positive Input Current Range)

7.3.1.2 DC Performance of Bipolar Signal Chain With ADS7253EVM (12-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and –25°C. Figure 44 and Figure 45 show the two accuracy graphs for the negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

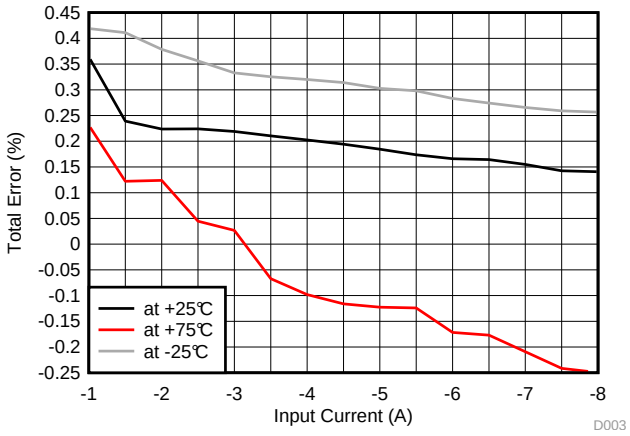


Figure 44. Bipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Negative Input Current Range—With 12-Bit ADC

While measuring the voltages at each of the outputs of the bipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 1.7 mV and the reference on the ADS7253EVM changes by 1.6 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.8 mV and the reference on the ADS7253EVM changes by 3.3 mV throughout the negative input current range.

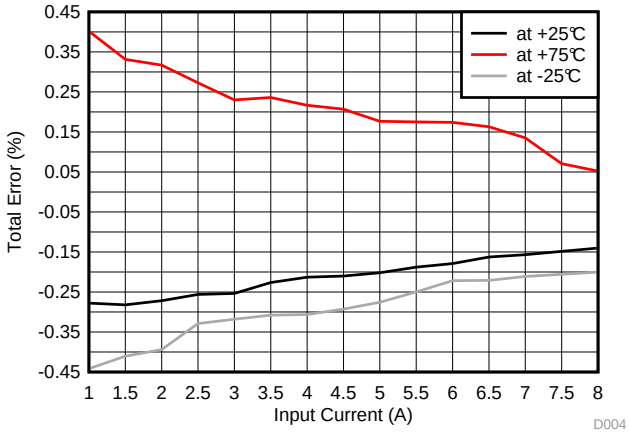


Figure 45. Bipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Positive Input Current Range—With 12-Bit ADC

While measuring the voltages at each of the outputs of the bipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.4 mV and the reference on the ADS7253EVM changes by 2.5 mV throughout the positive input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.8 mV and the reference on the ADS7253EVM changes by 3.1 mV throughout the positive input current range.

With the ADS7253EVM GUI, the DC Code histogram is also observed. Figure 46 shows the histogram for the same. From the histogram, it is shown that

- ENOB (calculated using standard deviation) = 12 bits
- Noise free bits (calculated using peak-to-peak noise) = 11.63 bits

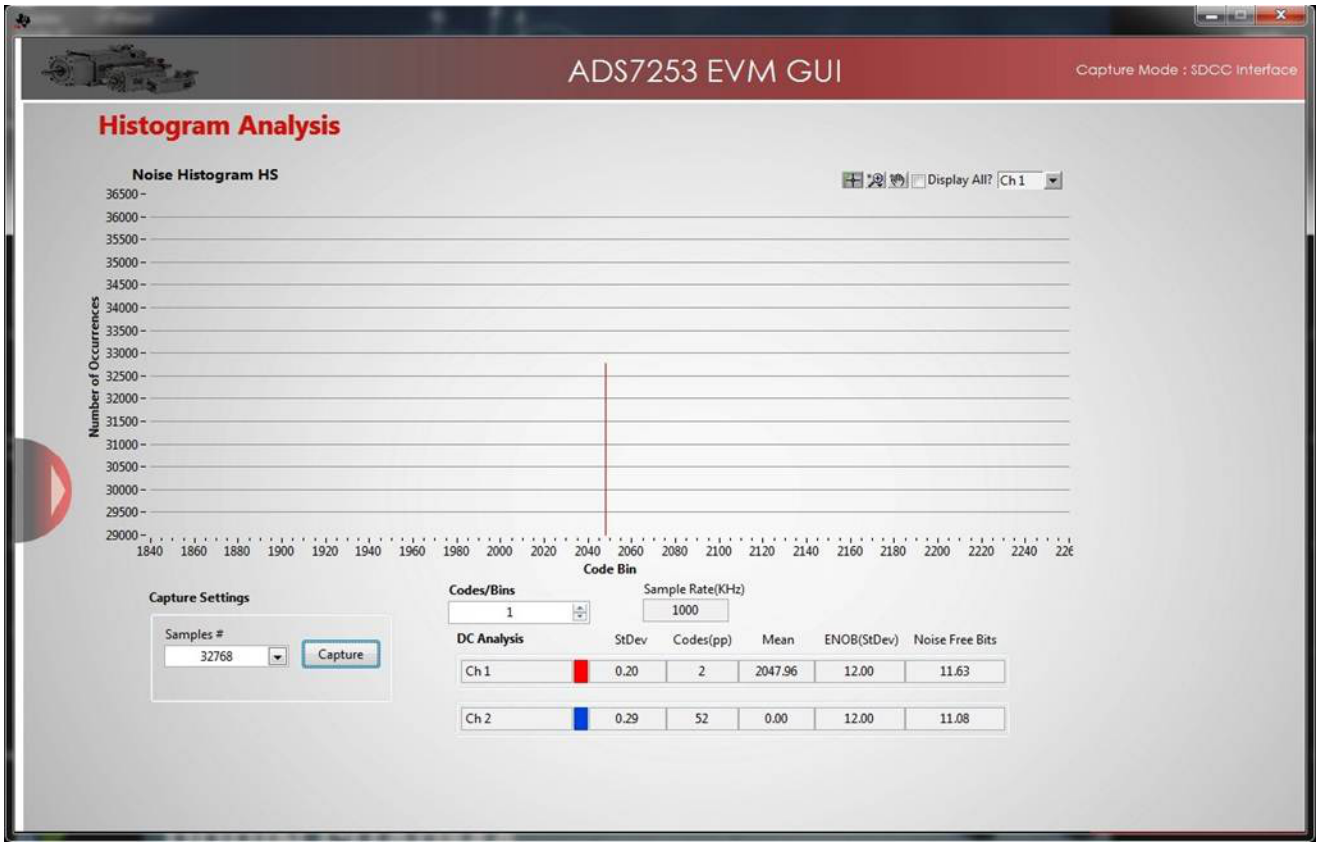


Figure 46. DC Code Histogram

7.3.1.3 DC Performance of Bipolar Signal Chain With ADS8353EVM (16-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and –25°C. Figure 47 and Figure 48 show the two accuracy graphs for negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

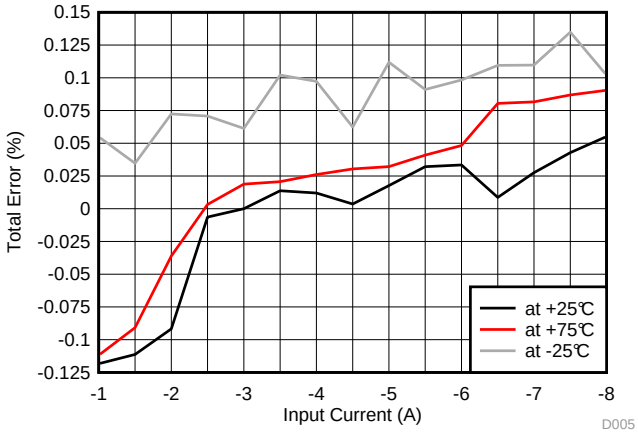


Figure 47. Bipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Negative Input Current Range—With 16-Bit ADC

While measuring the voltages at each of the outputs of the bipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.3 mV and the reference on the ADS8353EVM changes by 1.8 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 2.3 mV and the reference on the ADS8353EVM changes by 1.8 mV throughout the negative input current range.

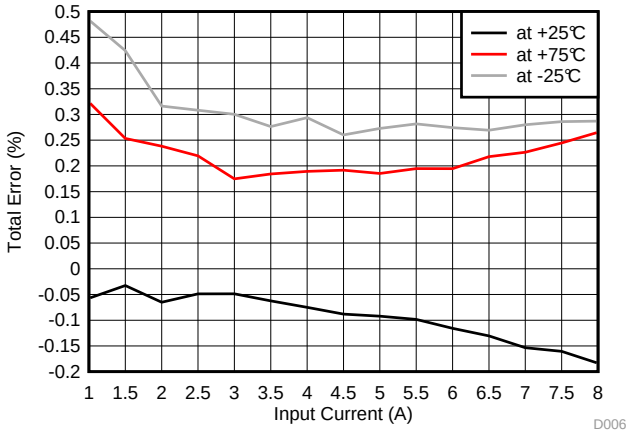


Figure 48. Bipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Positive Input Current Range—With 16-Bit ADC

While measuring the voltages at each of the outputs of the bipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.3 mV and the reference on the ADS8353EVM changes by 2.3 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.5 mV and the reference on the ADS8353EVM changes by 1.5 mV throughout the negative input current range.

With the ADS8353EVM GUI, the DC Code histogram is also observed. Figure 49 shows the histogram for the same. From the histogram, it is shown that

- ENOB (calculated using standard deviation) = 15.45 bits
- Noise free bits (calculated using peak-to-peak noise) = 12.73 bits

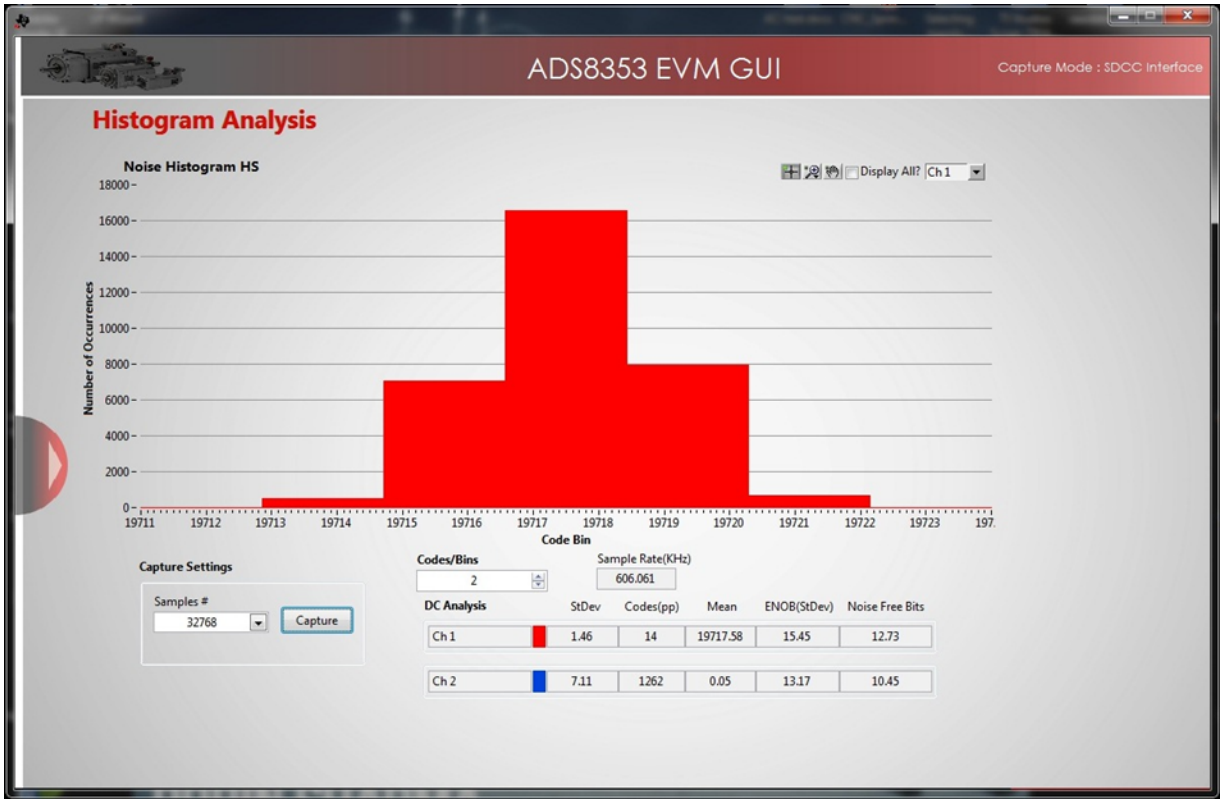


Figure 49. DC Code Histogram

7.3.2 DC Performance of Unipolar Signal Conditioning Circuit

For analyzing the DC performance of the unipolar signal conditioning circuit, the ADS7253EVM and ADS8353EVM (for 12-bit and 16-bit performance, respectively) are used along with the TIDA-00316 boards as shown in Figure 29. The DC accuracy is measured at each of the stages:

- On TIDA-00316 board:
  - Sensor output
  - Output of op-amp
  - Output of Sallen-key Filter
- On ADC board:
  - Input of ADC
  - Output data on ADC GUI

7.3.2.1 DC Performance of Unipolar Signal Chain (Amplifier + Filter + ADC)

The DC accuracy is observed for the unipolar signal chain. Figure 50 and Figure 51 show the two accuracy graphs for the negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

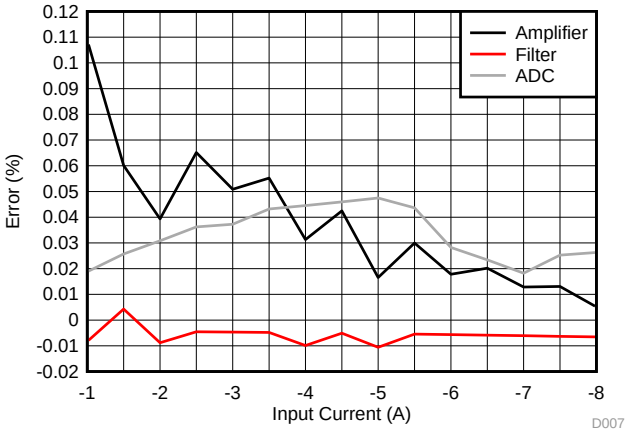


Figure 50. Unipolar Signal Chain DC Accuracy (for Negative Input Current Range)

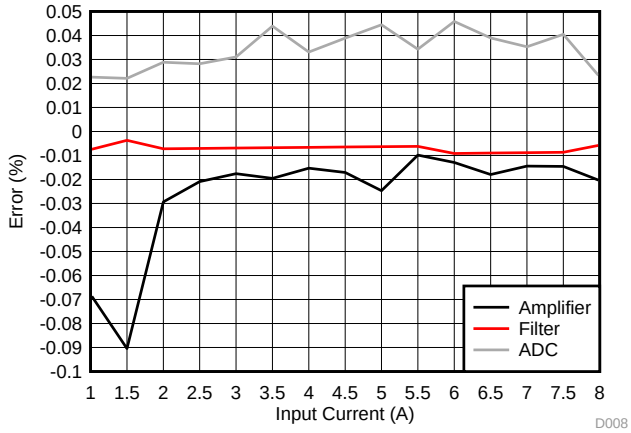


Figure 51. Unipolar Signal Chain DC Accuracy (for Positive Input Current Range)

7.3.2.2 DC Performance of Unipolar Signal Chain With ADS7253EVM (12-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and –25°C. Figure 52 and Figure 53 show the two accuracy graphs for the negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

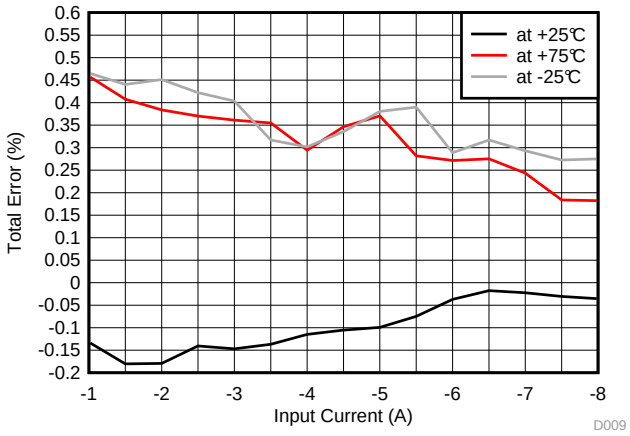


Figure 52. Unipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Negative Input Current Range—With 12-Bit ADC

While measuring the voltages at each of the outputs of the unipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.6 mV and the reference on the ADS7253EVM changes by 2.5 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.6 mV and the reference on the ADS7253EVM changes by 1.6 mV throughout the negative input current range.

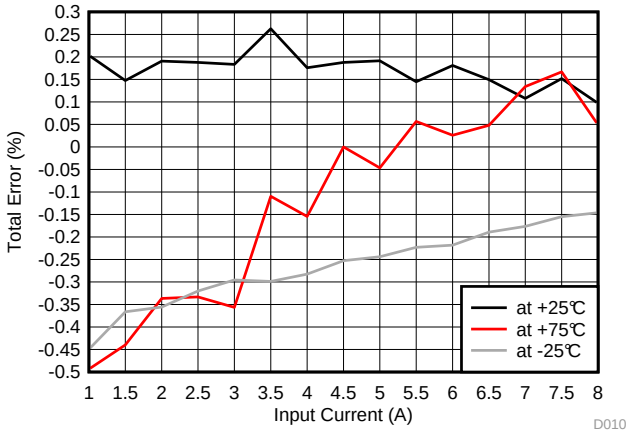


Figure 53. Unipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Positive Input Current Range—With 12-Bit ADC

While measuring the voltages at each of the outputs of the unipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.2 mV and the reference on the ADS7253EVM changes by 2.2 mV throughout the positive input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.4 mV and the reference on the ADS7253EVM changes by 1.4 mV throughout the positive input current range.

With the ADS7253EVM GUI, the DC code histogram is also observed. Figure 54 shows the histogram for the same. From the histogram, it is shown that

- ENOB (calculated using standard deviation) = 12 bits
- Noise free bits (calculated using peak-to-peak noise) = 11.86 bits

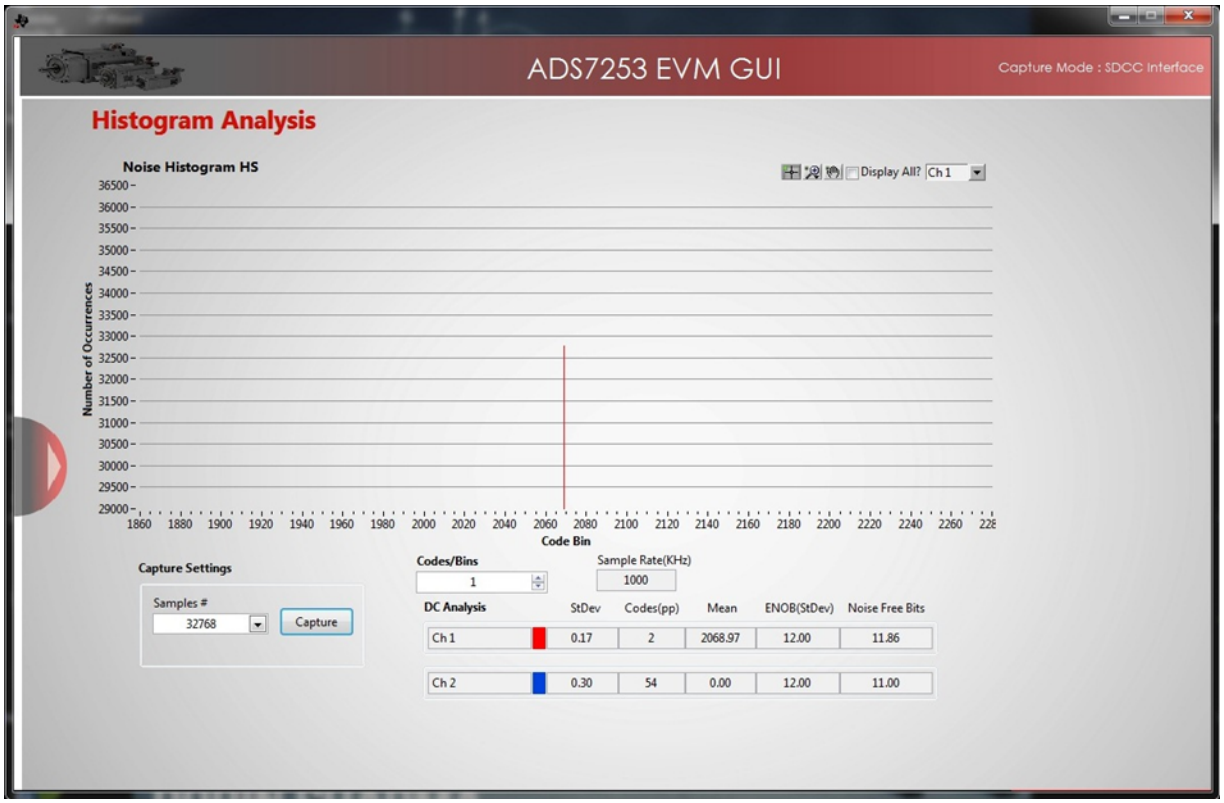


Figure 54. DC Code Histogram

7.3.2.3 DC Performance of Unipolar Signal Chain With ADS8353EVM (16-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and –25°C. Figure 55 and Figure 56 show the two accuracy graphs for the negative current range (–1 to –8 A) and positive current range (1 to 8 A), respectively.

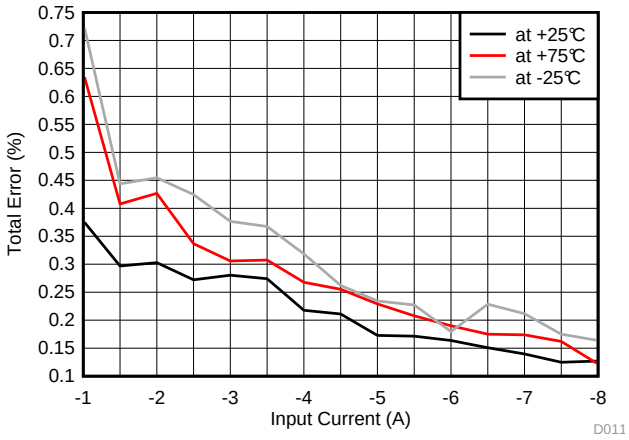


Figure 55. Unipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Negative Input Current Range—With 16-Bit ADC

While measuring the voltages at each of the outputs of the unipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 2.3 mV and the reference on the ADS8353EVM changes by 2.1 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.7 mV and the reference on the ADS8353EVM changes by 1.6 mV throughout the negative input current range.

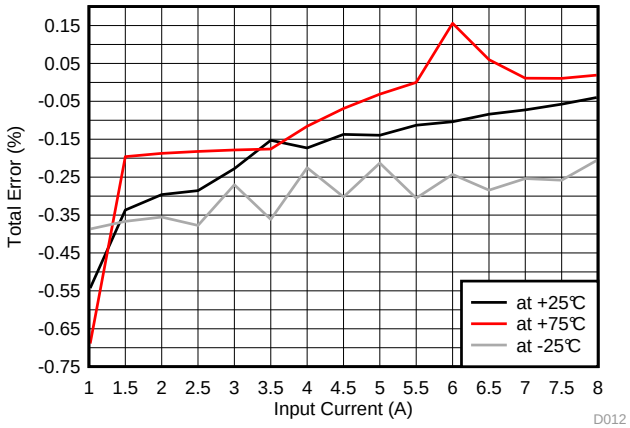


Figure 56. Unipolar Signal Chain Circuit DC Accuracy at Three Different Temperatures—For Positive Input Current Range—With 16-Bit ADC

While measuring the voltages at each of the outputs of the unipolar signal chain, the following changes in the reference voltages are observed.

At –25°C, the reference voltage on the TIDA-00316 board changes by 1.6 mV and the reference on the ADS8353EVM changes by 2.1 mV throughout the negative input current range.

At 75°C, the reference voltage on the TIDA-00316 board changes by 1.7 mV and the reference on the ADS8353EVM changes by 2.2 mV throughout the negative input current range.

With the ADS8353EVM GUI, the DC Code histogram is also observed. Figure 57 shows the histogram for the same. From the histogram, it is shown that

- ENOB (calculated using standard deviation) = 15.22 bits
- Noise free bits (calculated using peak-to-peak noise) = 12.50 bits

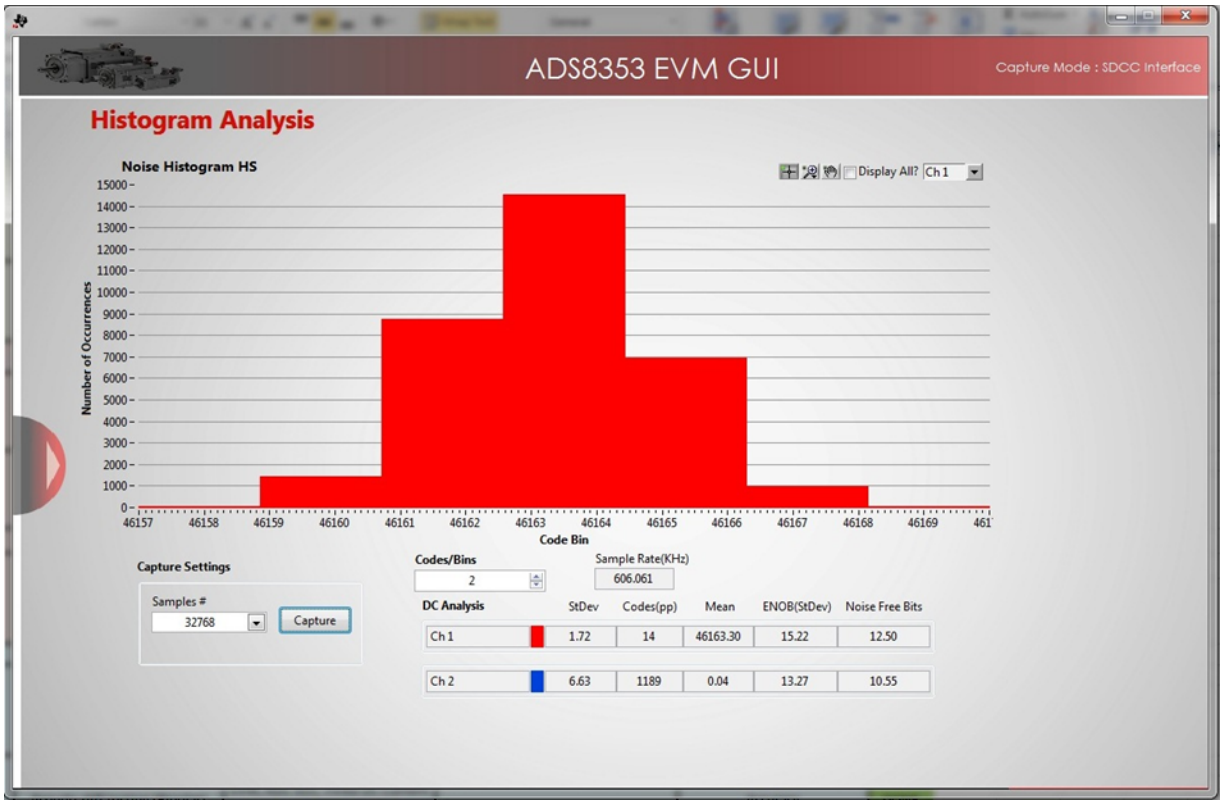


Figure 57. DC Histogram

7.3.3 DC Performance of Bipolar Signal Conditioning Circuit Using Delfino F2837x Internal ADC

The DC accuracy of the bipolar signal conditioning circuit is also measured with the internal ADC of Delfino F2837x. Figure 58 shows the DC accuracy graph for the negative input current range, and Figure 59 shows the DC accuracy graph for the positive input current range.

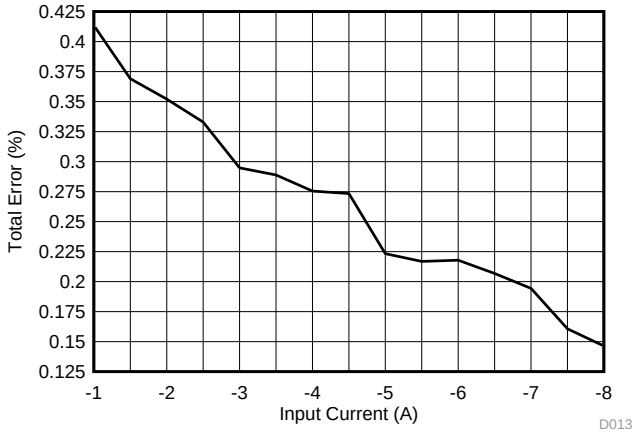


Figure 58. Bipolar Signal Chain Circuit DC Accuracy—For Negative Input Current Range—With 12-Bit Internal ADC of Delfino Controller

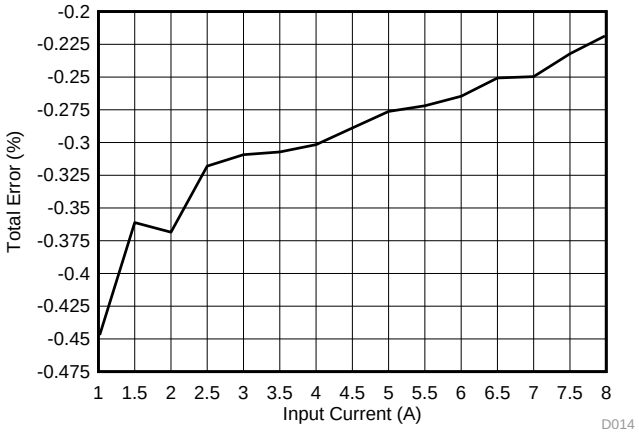


Figure 59. Bipolar Signal Chain Circuit DC Accuracy—For Positive Input Current Range—With 12-Bit Internal ADC of Delfino Controller

7.3.4 DC Performance of Unipolar Signal Conditioning Circuit Using Delfino F2837x Internal ADC

The DC accuracy of the unipolar signal conditioning circuit is also measured with the internal ADC of Delfino F2837x. Figure 60 shows the DC accuracy graph for the negative input current range, and Figure 61 shows the DC accuracy graph for the positive input current range.

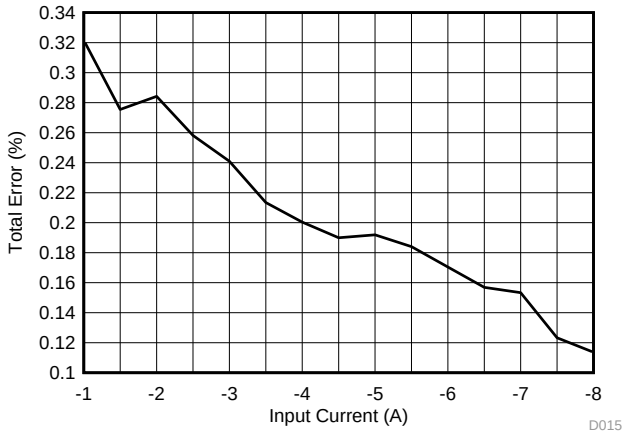


Figure 60. Unipolar Signal Chain Circuit DC Accuracy—For Negative Input Current Range—With 12-Bit Internal ADC of Delfino Controller

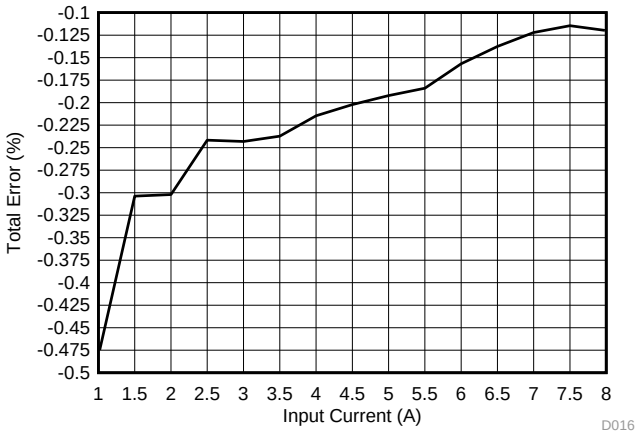


Figure 61. Unipolar Signal Chain Circuit DC Accuracy—For Positive Input Current Range—With 12-Bit Internal ADC of Delfino Controller

7.4 AC (or Dynamic) Performance

For any data acquisition system, an important focus is to achieve excellent dynamic performance while minimizing the total power consumption of the system. The main AC specifications that can be considered are THD, SNR, SINAD, and ENOB. Essentially, all these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a Fast-Fourier Transform (FFT) analysis. A typical FFT plot for an ADC is shown in Figure 62.

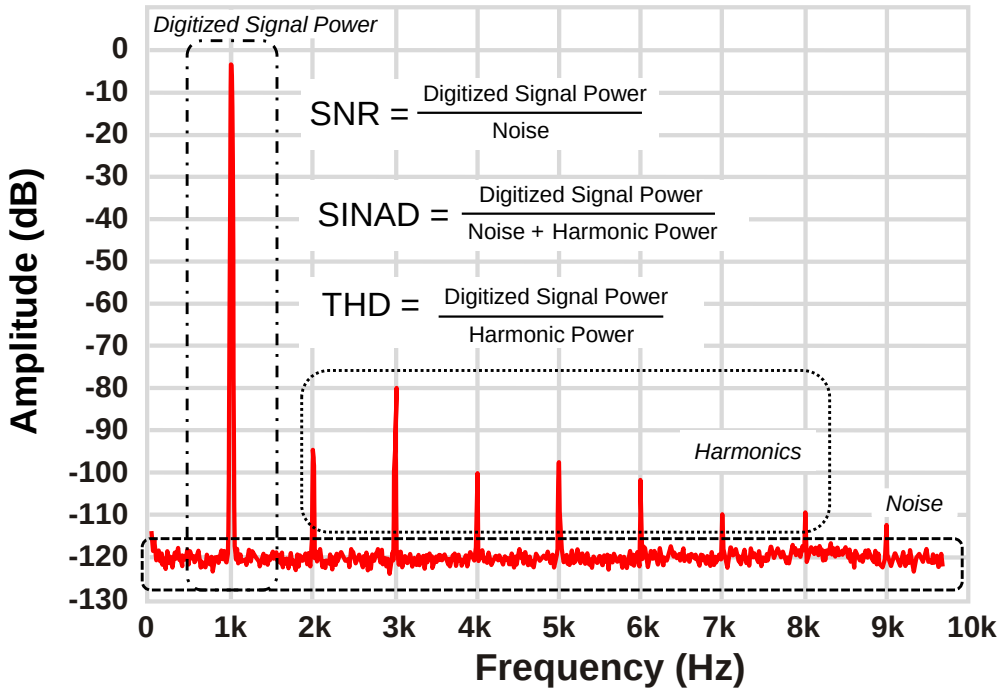


Figure 62. Typical FFT Plot Showing Different Dynamic Parameters

Signal-to-noise ratio (SNR) provides insight into the total noise of the system. The total noise of the data acquisition system is the rss of front-end amplifier noise (Vn_AMP_RMS) and the ADC noise (Vn_ADC_RMS). The ADC noise includes the quantization noise as well as the noise contributed by ADC internal circuitry or the input-referred noise of the ADC. The total noise contributions from all these sources, denoted as Vn_TOT_RMS are referred to the input of the ADC for calculating the total SNR of the system (SNRSYS).

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2}$$

$$SNR_{SYS} = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \quad (11)$$

Effective number of bits (ENOB) is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated as:

$$SNR = 6.02 \times N + 1.76 \quad (12)$$

While ENOB provides a good summary of the ADC dynamic performance, it does not describe the converter's entire performance over the operating frequency ranges and input signals. Additionally, ENOB does not include the ADC dc specifications such as offset and gain error. Therefore, it is important to pay attention to other converter specifications as well depending on the application in which the ADC is being used.

7.4.1 AC Performance of Bipolar Signal Conditioning Circuit Using ADS7253EVM

With the following test conditions, the waveform signal as well as the FFT of the signal is observed and captured using the ADS7253EVM.

Input current flowing through LAH 25-NP = ±8A (peak-to-peak) @ 50 Hz
Corresponding output voltage of LAH 25-NP (with burden resistor = 42.2 Ω) = ±1.05 V (peak-to-peak)

The settings done on ADS7253EVM GUI while capturing the signal are:

- Number of samples = 32768
- Sample rate = 476.471 kHz
- Internal reference = 2.5 V
- 2-VREF mode selected

Figure 63 shows the waveform captured using the ADS7253EVM GUI. The measured voltage is ~2 V (peak-to-peak) @ 50 Hz.

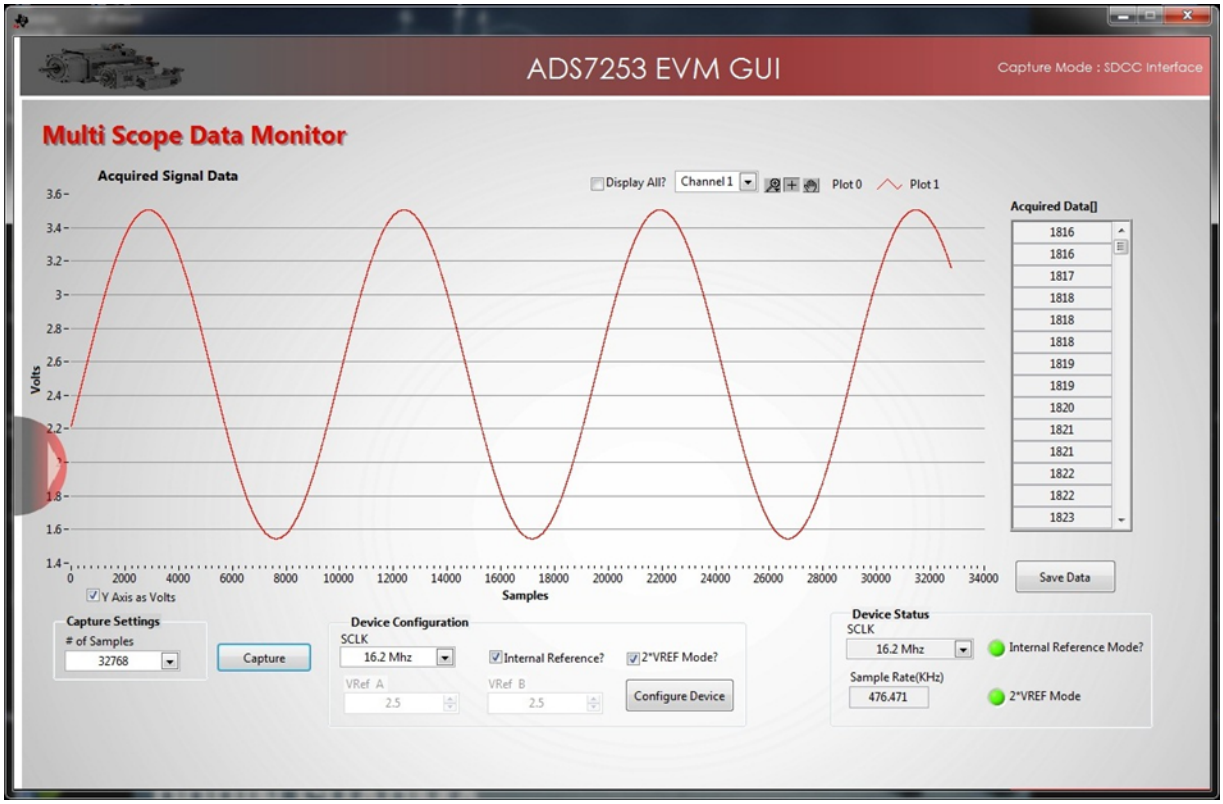


Figure 63. Current Waveform Captured With ADS7253EVM GUI

For the same signal, FFT is also captured using the ADS7253EVM GUI. The settings done for capturing FFT are:

- Number of samples = 16384
- Window = 7-term B-Harris
- Sample rate = 476.471 kHz

Figure 64 shows the FFT signal captured using the ADS7253EVM GUI. The measured SNR at the signal level of –8.1377 dBFS is 65.8556 dB. It is important to note that an 8-A current is not the full-scale value for which the signal chain is designed. That is the reason why the signal level is shown –8.1377 dBFS and not 0 dBFS.

Figure 64. FFT Captured With ADS7253EVM GUI

Observed results are:

- SNR = 65.8556 dB
- THD = –105.5 dB
- SINAD = 65.9 dB

The zoomed version of FFT, shown in Figure 65, shows the 50-Hz signal.

Figure 65. Zoomed FFT Showing 50-Hz Signal

7.4.2 AC Performance of Unipolar Signal Conditioning Circuit Using ADS7253EVM

With the following test conditions, the waveform signal as well as FFT of the signal is observed and captured using the ADS7253EVM.

Input current flowing through LAH 25-NP = ±8 A (peak-to-peak) @ 50 Hz
Corresponding output voltage of LAH 25-NP (with burden resistor = 42.2 Ω) = ±1.05 V (peak-to-peak)

The settings done on the ADS7253EVM GUI while capturing the signal are:

- Number of samples = 32768
- Sample rate = 476.471 kHz
- Internal reference = 2.5 V
- 2-VREF mode selected

Figure 66 shows the waveform captured using the ADS7253EVM GUI. The measured voltage is ~2 V (peak-to-peak) @ 50 Hz.

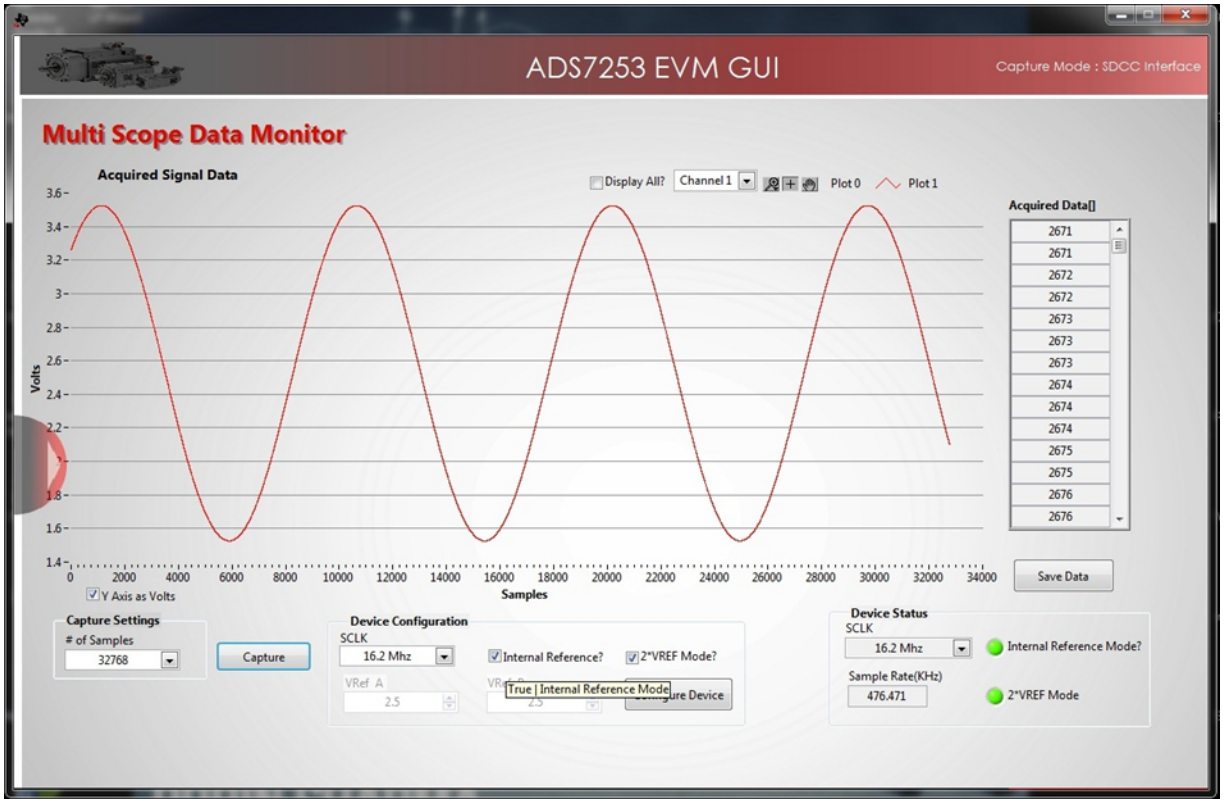


Figure 66. Current Waveform Captured With ADS7253EVM GUI

For the same signal, FFT is also captured using the ADS7253EVM GUI. The settings done for capturing FFT are:

- Number of samples = 32768
- Window = 7-term B-Harris
- Sample rate = 476.471 kHz

Figure 67 shows the FFT signal captured using the ADS7253EVM GUI. The measured SNR at the signal level of –8.1377 dBFS is 65.8118 dB. It is important to note that an 8-A current is not the full-scale value for which the signal chain is designed. That is the reason why the signal level is shown –8.1377 dBFS and not 0 dBFS.

Figure 67. FFT Captured With ADS7253EVM GUI

The zoomed version of FFT shown in Figure 68, shows the 50-Hz signal.

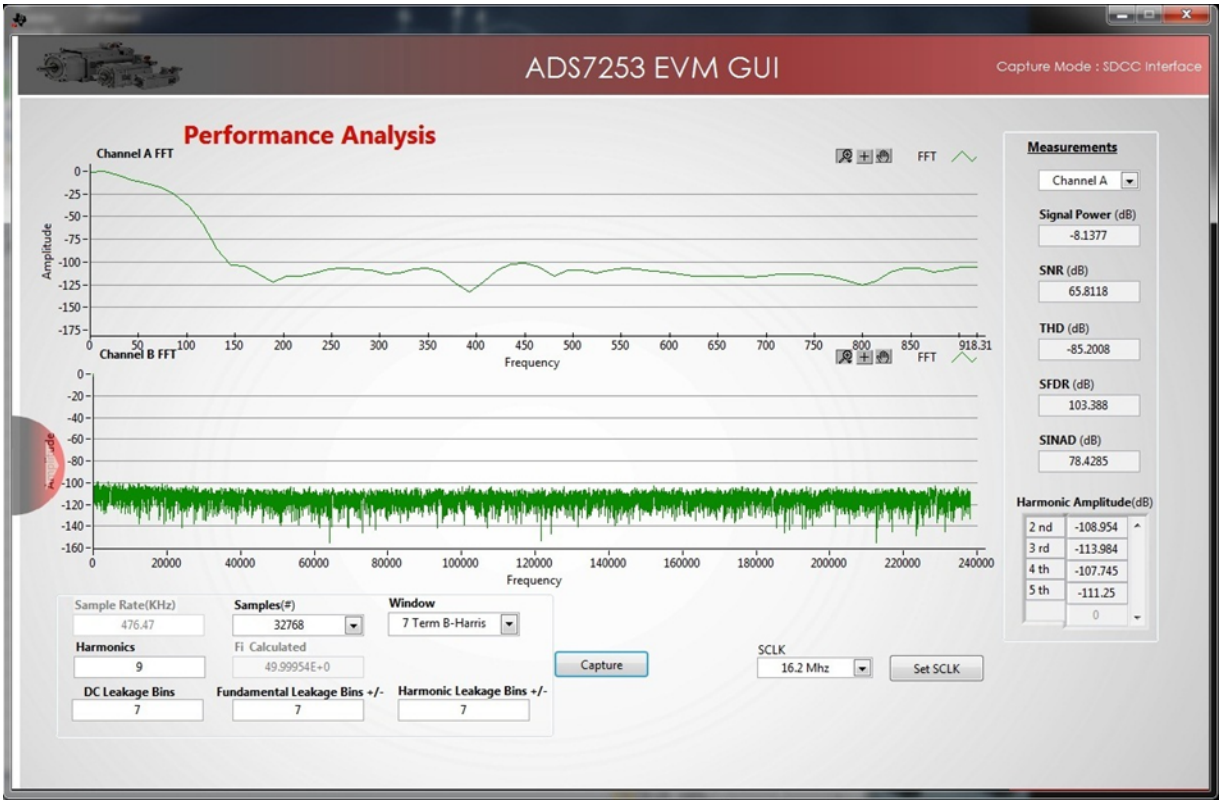


Figure 68. Zoomed FFT Showing 50-Hz Signal

Observed results are:

- SNR = 65.8118 dB
- THD = –104.7 dB
- SINAD = 65.8 dB

7.4.3 AC Performance of Bipolar Signal Conditioning Circuit Using Delfino F2837x Internal ADC

With the following test conditions, the waveform signal as well as FFT of the signal is observed and captured using the Delfino F2837x Control Card.

Input current flowing through LAH 25-NP = ±8 A (peak-to-peak) @ 50 Hz
Corresponding output voltage of LAH 25-NP (with burden resistor = 27 Ω) = ±422 mV (peak-to-peak)

The settings done on the Delfino F2837x software while capturing the signal are:

- ADC mode = Single ended
- Resolution = 12 bits
- ADC clock frequency = 30 MHz
- Through put (including ACQPS + Conversion time) = 567 ksps
- Reference voltage = 3.3 V
- Supply voltage = 3.3 V
- Number of sample = 100000
- FFT window = Blackman

Figure 69 shows the waveform captured using the Delfino GUI.

Figure 69. Current Waveform Captured With Delfino GUI

For the same signal, FFT is also captured using Delfino GUI. Figure 70 shows the FFT signal captured using the Delfino GUI.

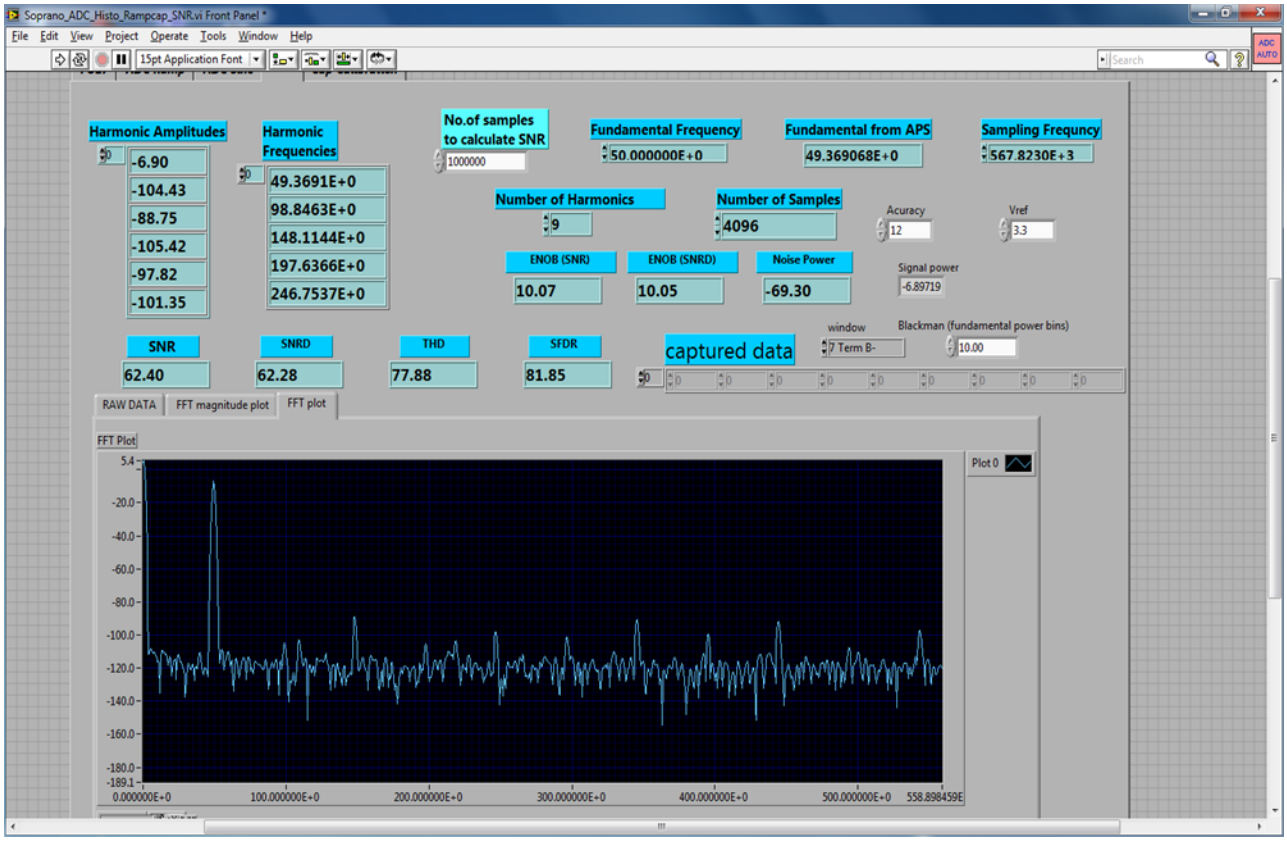


Figure 70. FFT Captured With Delfino GUI (Showing 50-Hz Signal)

Observed results are:

- SNR = 62.40 dB (with signal strength = –6.89719 dBFS)
- SINAD or SNRD = 62.28 dB
- THD = 77.88 dB
- SFDR = 81.85 dB
- ENOB (calculated using SNR) = 10.07 bits

The measured SNR at the signal level of –6.89719 dBFS is 62.40 dB. It is important to note that an 8-A current is not the full-scale value for which the signal chain is designed. That is the reason why the signal level is shown –6.89 dBFS and not 0 dBFS.

7.4.4 AC Performance of Unipolar Signal Conditioning Circuit Using Delfino F2837x Internal ADC

With the following test conditions, the waveform signal as well as FFT of the signal is observed and captured using the Delfino F2837x Control Card.

Input current flowing through LAH 25-NP = ±8 A (peak-to-peak) @ 50 Hz
Corresponding output voltage of LAH 25-NP (with burden resistor = 27 Ω) = ±422 mV (peak-to-peak)

The settings done on the Delfino F2837x software while capturing the signal are:

- ADC mode = Single ended
- Resolution = 12 bits
- ADC clock frequency = 30 MHz
- Through put (including ACQPS + Conversion time) = 567 ksps
- Reference voltage = 3.3 V
- Supply voltage = 3.3 V
- Number of sample = 100000
- FFT window = Blackman

Figure 71 shows the waveform captured using the Delfino GUI.

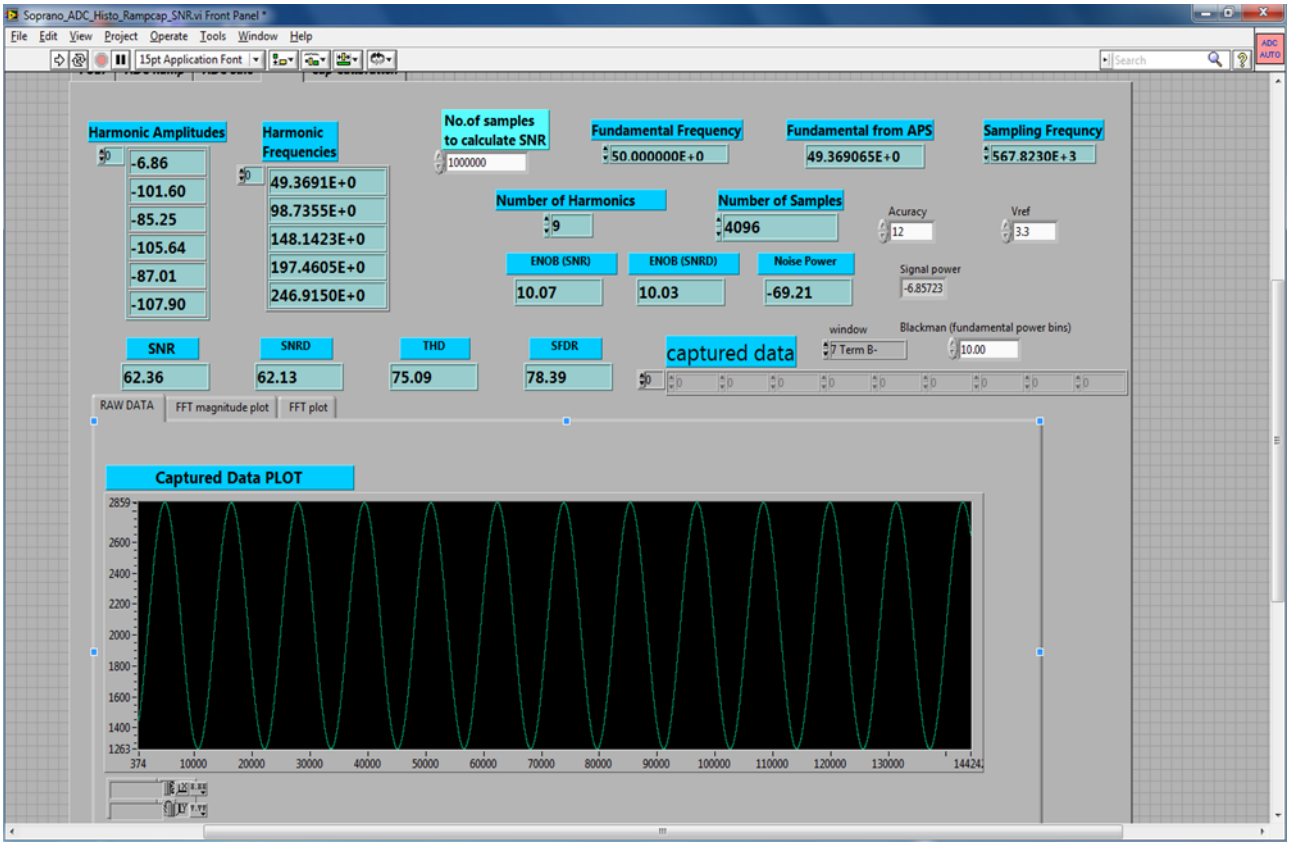


Figure 71. Current Waveform Captured With Delfino GUI

For the same signal, FFT is also captured using the Delfino GUI. Figure 72 shows the FFT signal captured using the Delfino GUI.

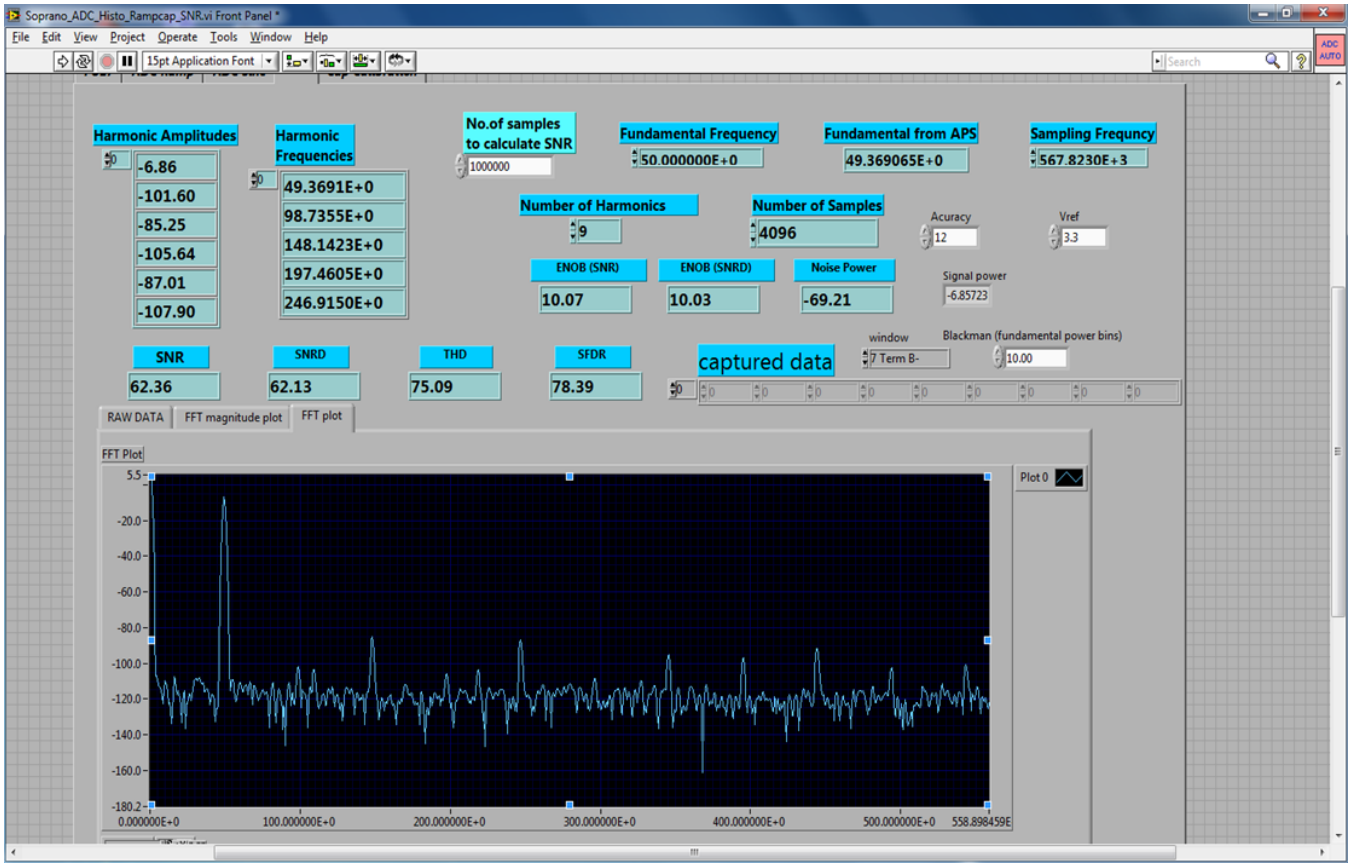


Figure 72. FFT Captured With Delfino GUI (Showing 50-Hz Signal)

The observed results are:

- SNR = 62.36 dB (with signal strength = –6.85723 dBFS)
- SINAD or SNRD = 62.13 dB
- THD = 75.09 dB
- SFDR = 78.39 dB
- ENOB (calculated using SNR) = 10.07 bits

The measured SNR at the signal level of –6.85723 dBFS is 62.36 dB. It is important to note that an 8-A current is not the full-scale value for which the signal chain is designed. That is the reason why the signal level is shown –6.85723 dBFS and not 0 dBFS.

7.5 Testing With ACIM and Motor Drive

The design is tested with a 3-kW AC motor drive and 2HP AC induction motor. Figure 73 shows the test setup.

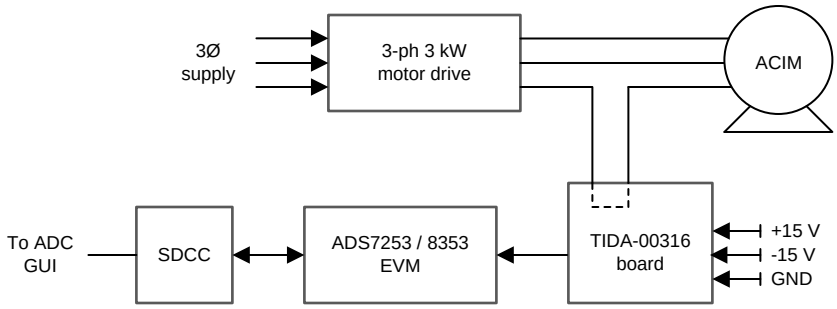


Figure 73. Test Setup Block Diagram

Figure 74 shows the picture of the test setup.

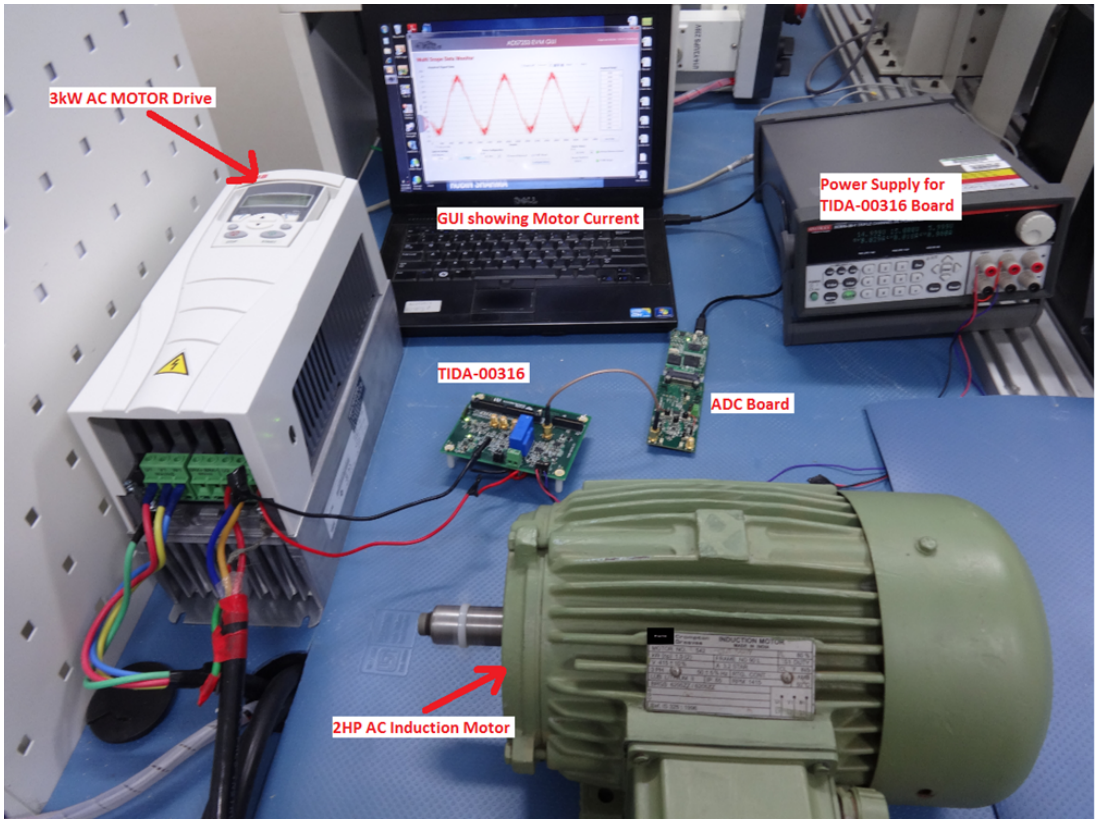


Figure 74. Image Showing the Test Setup

As shown in Figure 74, the TIDA-00316 board is connected with an ADC board (ADS7253EVM) to capture the motor current. The following parameters are set on the motor drive:

- Motor voltage = 415-V AC
- Motor frequency = 50 Hz
- Motor speed = 1440 rpm
- Motor current = 1.4 A
- Acceleration and deceleration time = 5 seconds

7.5.1 Testing of Bipolar Signal Conditioning Circuit

The ADC board (ADS7253EVM) is connected to the SMA jack J8 and the motor current is monitored using the ADS7253EVM GUI. The sine wave signal (Figure 75) as well as FFT (Figure 77) of the motor current is captured using the ADS7253EVM GUI. The motor current is also measured with a current probe using an oscilloscope (Figure 76). The inverter switching frequency of the motor drive (used for testing) is 4 kHz and it is visible from the zoomed FFT plot (Figure 78) as well as FFT captured on an oscilloscope (Figure 79).

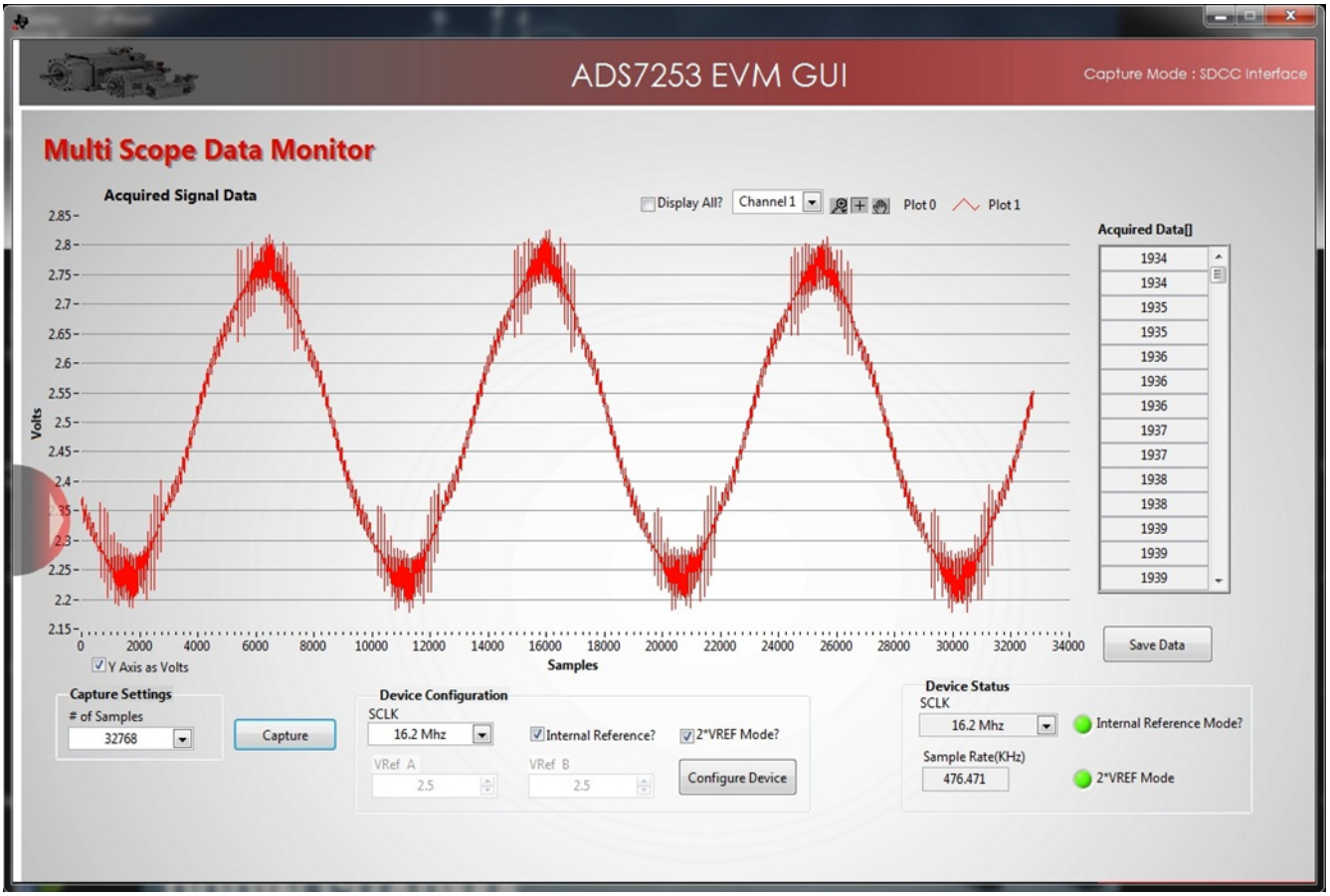


Figure 75. Motor Current Waveform Observed on ADS7253EVM GUI

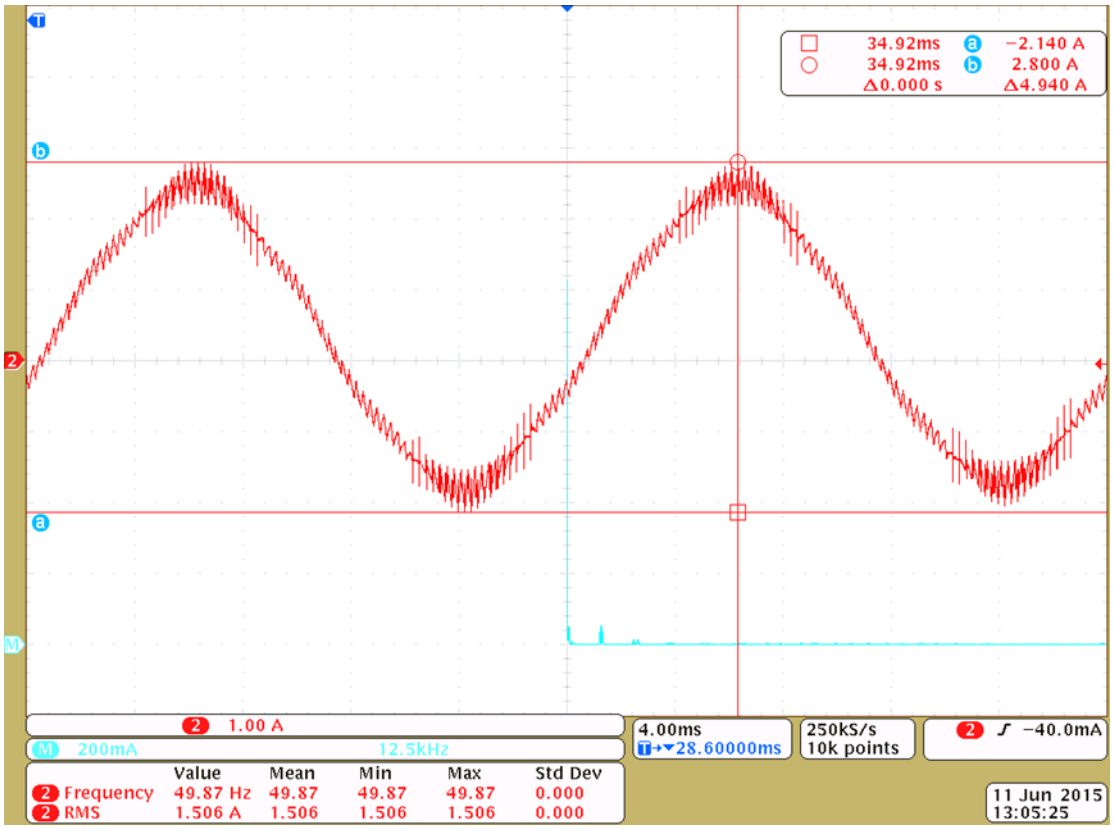


Figure 76. Motor Current Waveform Measured Using Oscilloscope

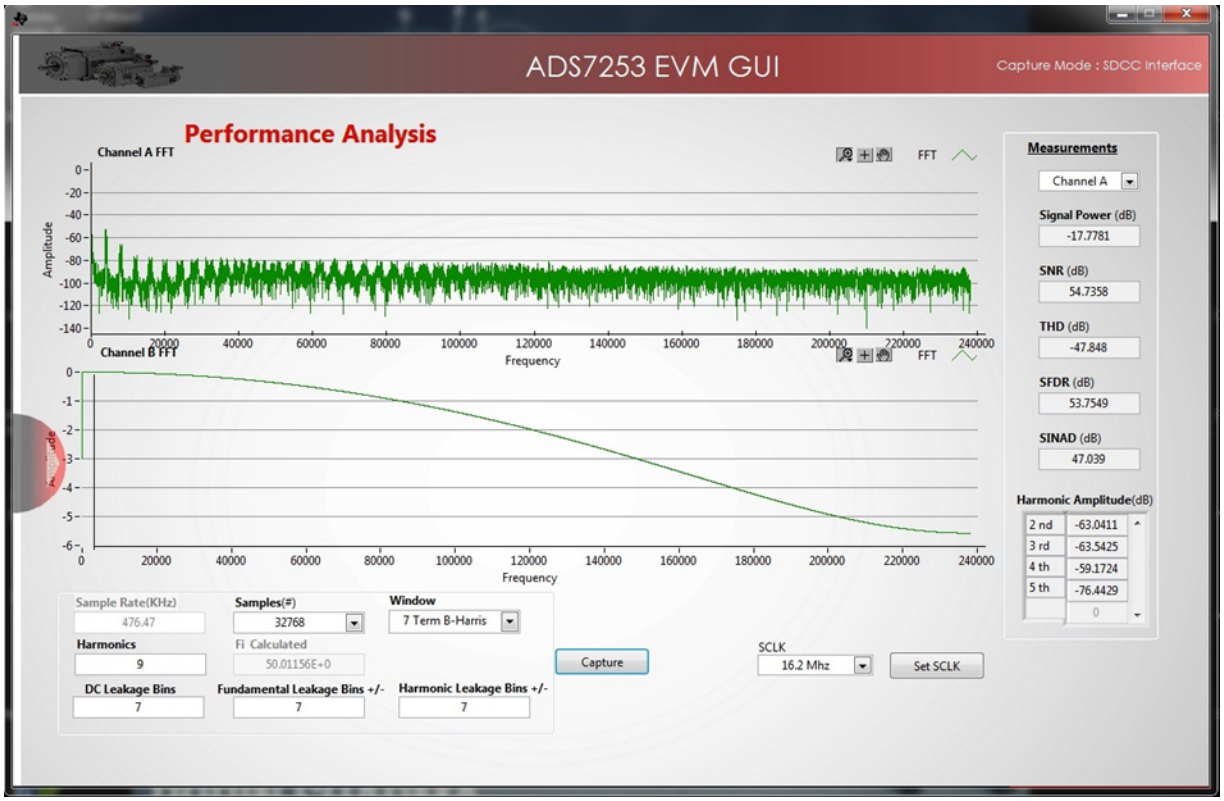


Figure 77. FFT of Motor Current (Measured Using ADS7253 EVM GUI)

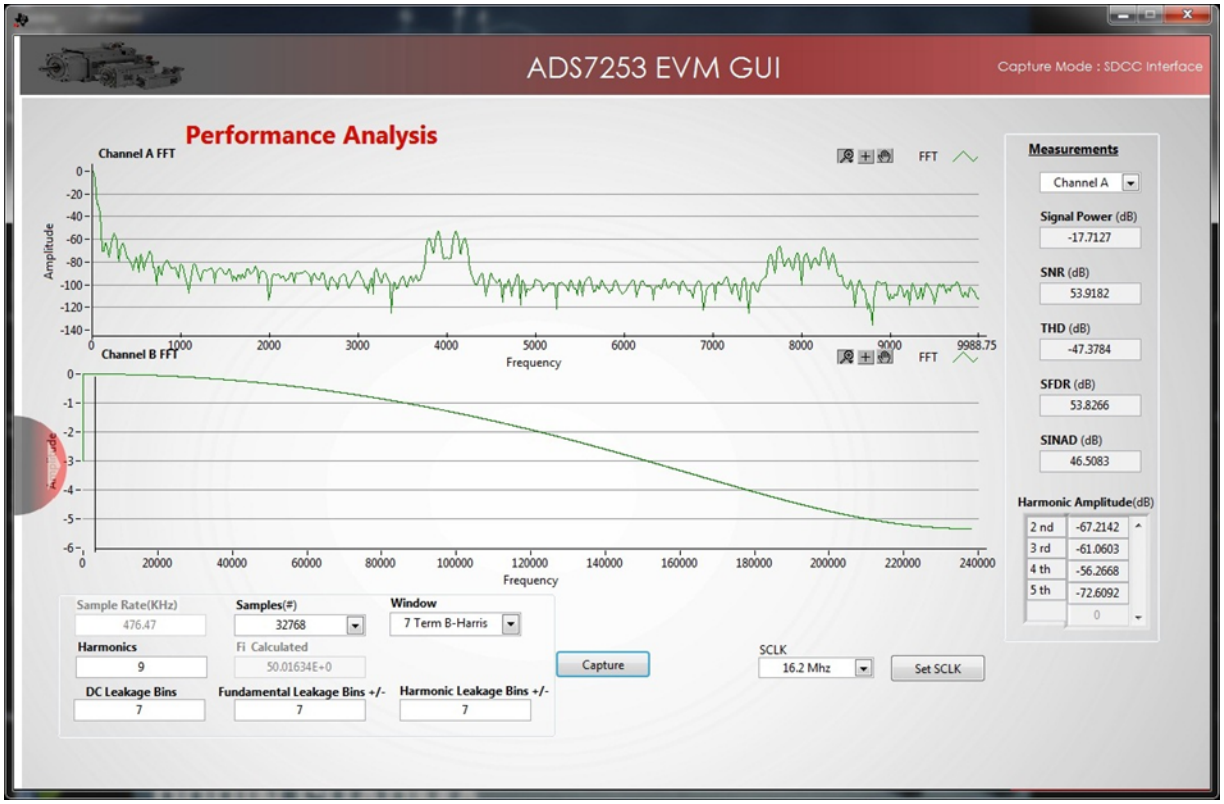


Figure 78. FFT of Motor Current (Zoomed)—Shows Switching Frequency at 4 kHz and its Harmonics

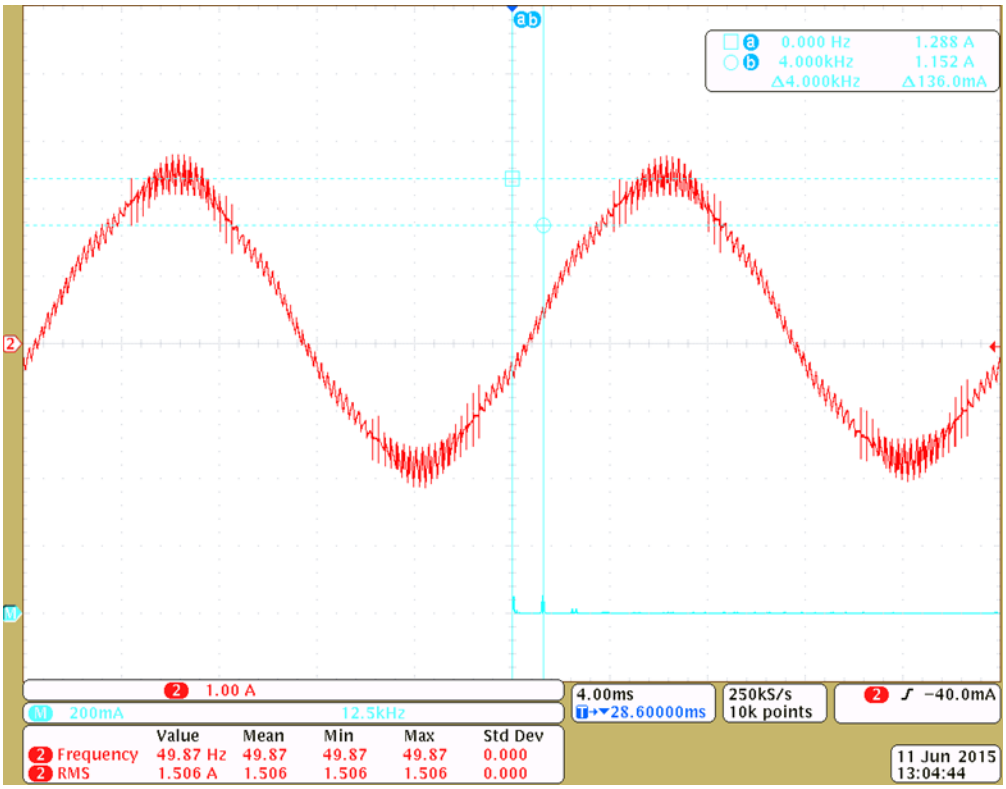


Figure 79. FFT of Motor Current Shown With Blue Graph

7.5.2 Testing of Unipolar Signal Conditioning Circuit

The ADC board (ADS7253EVM) is connected to the SMA jack J5 and the motor current is monitored using the ADS7253EVM GUI. The sine wave signal (Figure 80) as well as FFT (Figure 82) of the motor current is captured using the ADS7253EVM GUI. The motor current is also measured with a current probe using an oscilloscope (Figure 81). The inverter switching frequency of the motor drive (used for testing) is 4 kHz and it is visible from the zoomed FFT plot (Figure 83) as well as FFT captured on an oscilloscope (Figure 84).

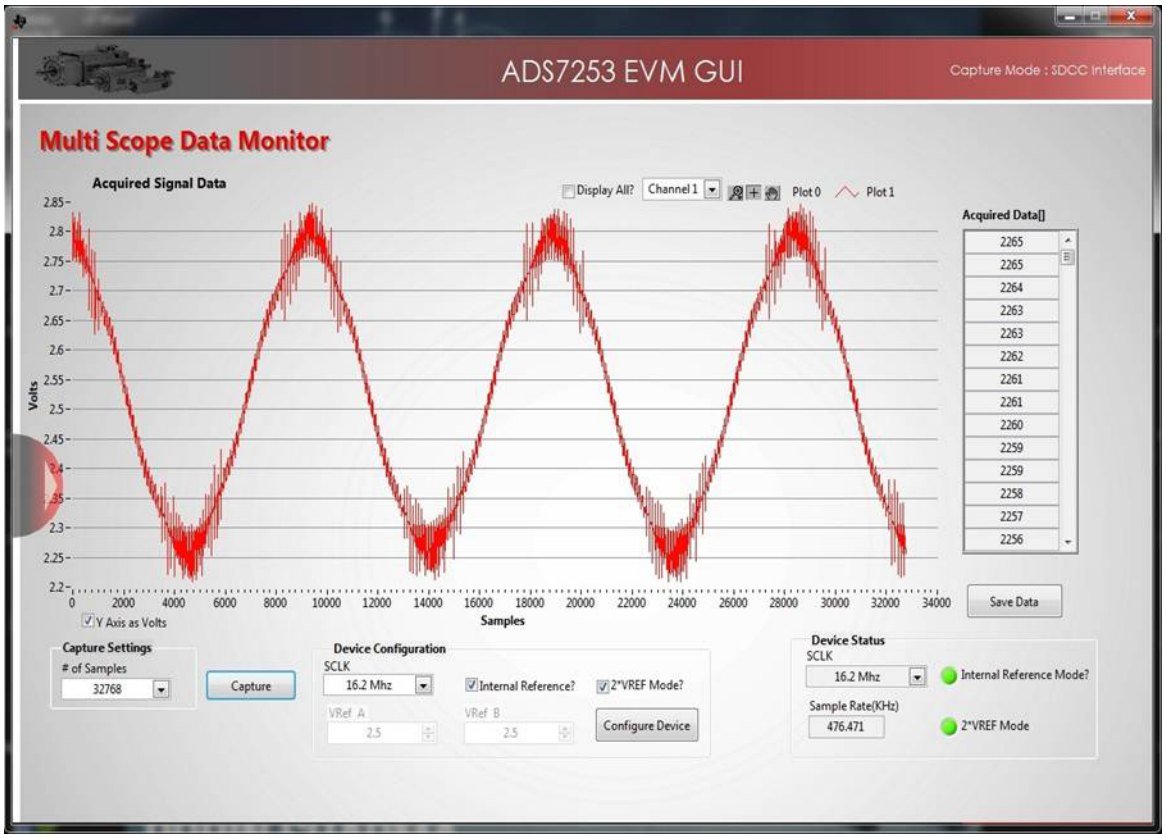


Figure 80. Motor Current Waveform Observed on ADS7253EVM GUI

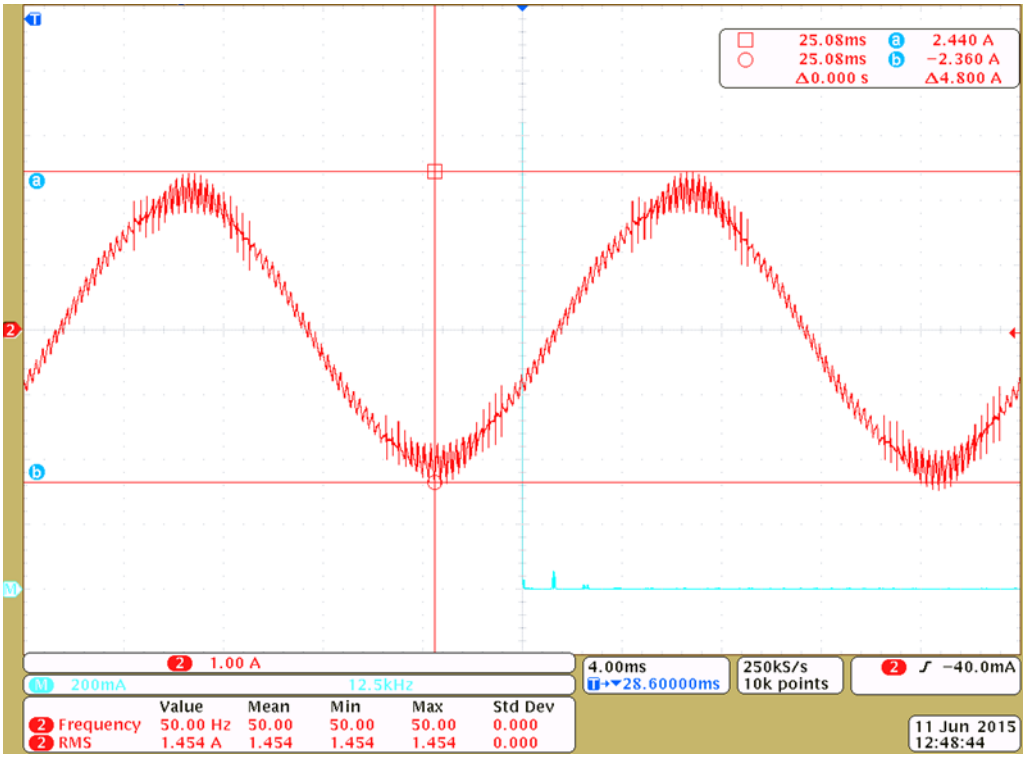


Figure 81. Motor Current Waveform Measured Using Oscilloscope

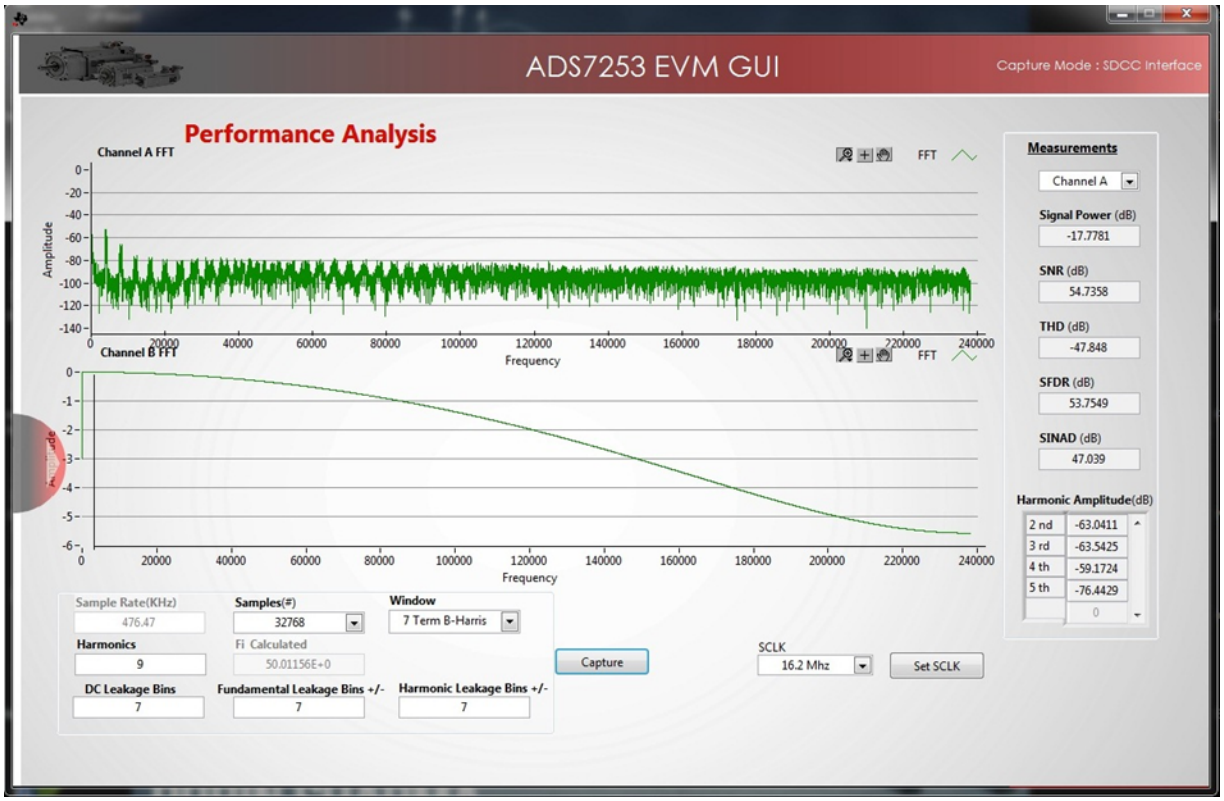


Figure 82. FFT of Motor Current (Measured Using ADS7253 EVM GUI)

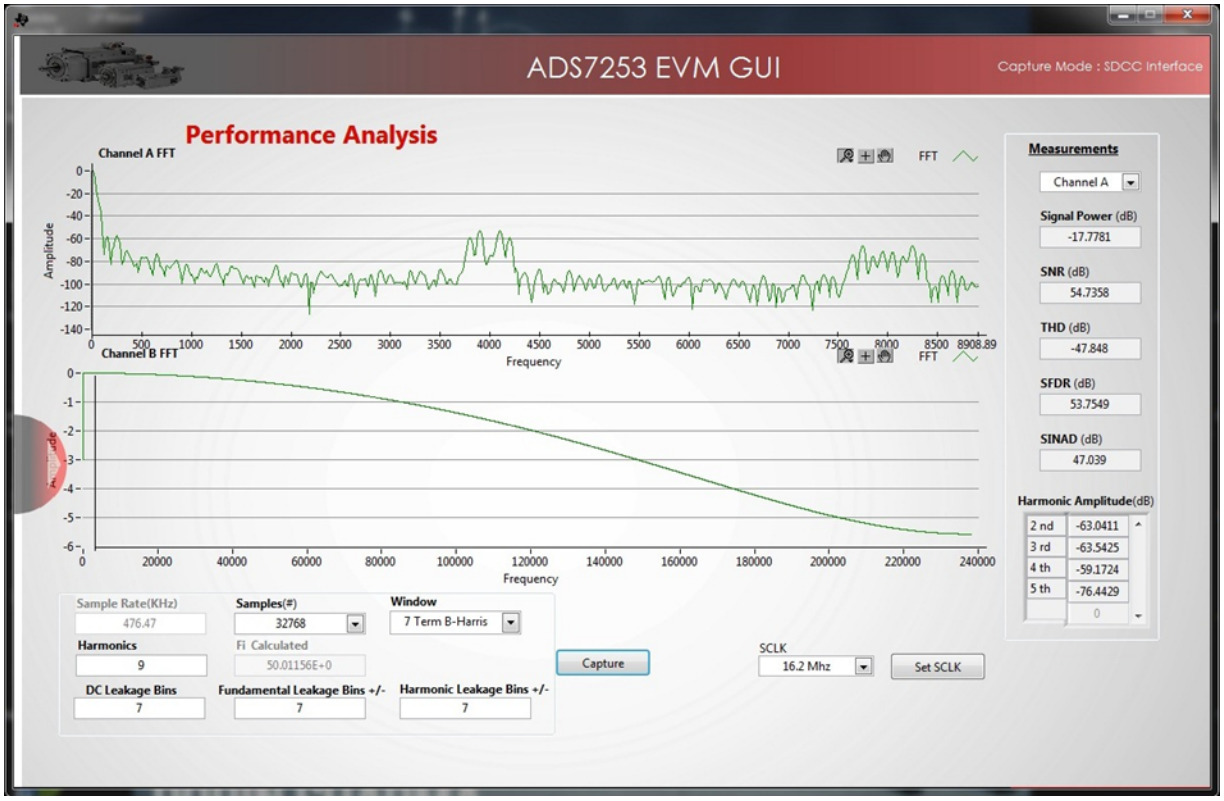


Figure 83. FFT of Motor Current (Zoomed)—Shows Switching Frequency at 4 kHz and its Harmonics

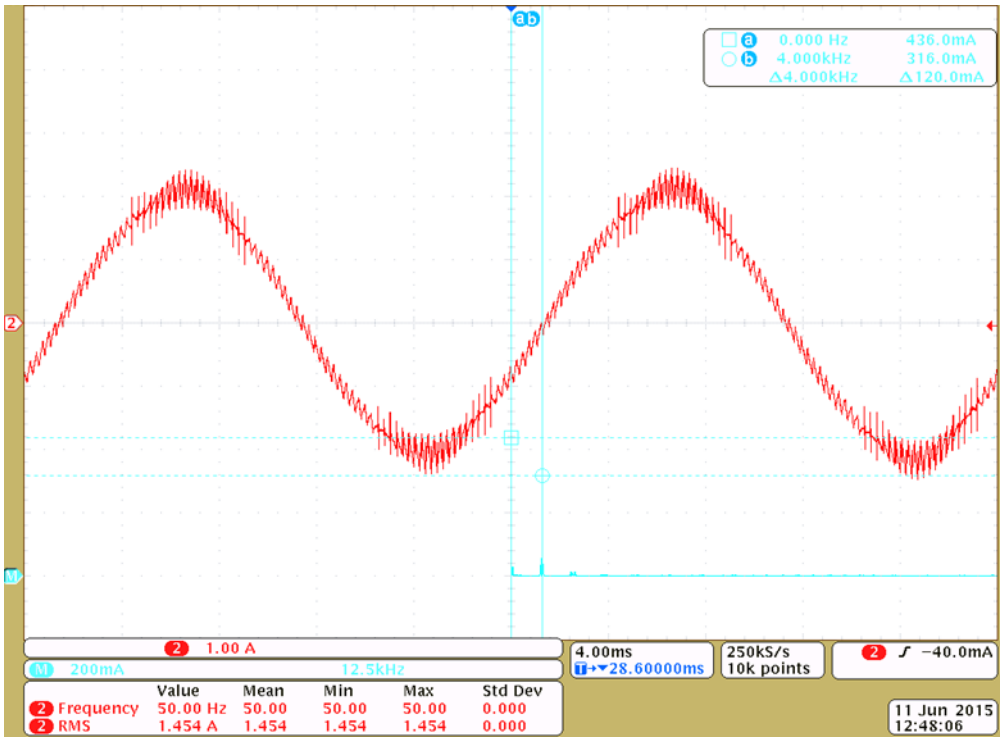


Figure 84. FFT of Motor Current Shown With Blue Graph

7.6 Overcurrent Protection Test Results

The overcurrent protection circuit is typically tested above 200% of the nominal current of the Hall-effect current sensor. As shown in Figure 7, LAH 25-NP with INP of 8 A can take a peak current up to 18 A. The overcurrent protection at 18 A is 225% of nominal primary current. The TIDA-00316 is tested at 18 A. The waveforms shown in Figure 85 and Figure 86 indicate the sensing of overcurrent condition at the positive threshold VTH (pos). The time required for the detection of the signal is 800 ns.

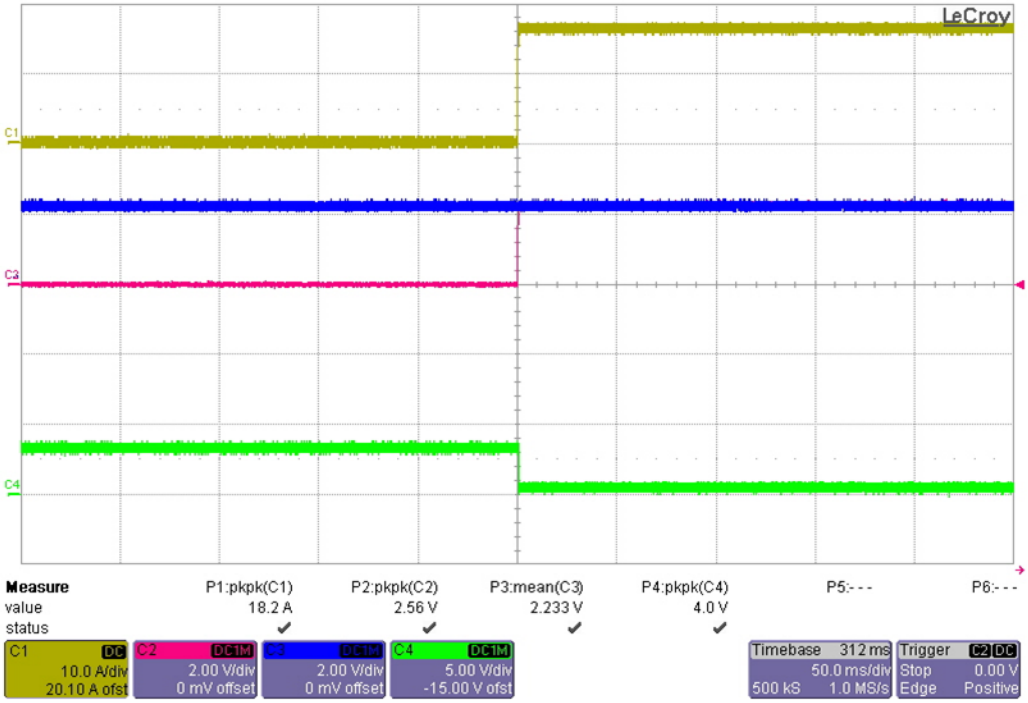


Figure 85. Overcurrent Detection at VTH (pos)

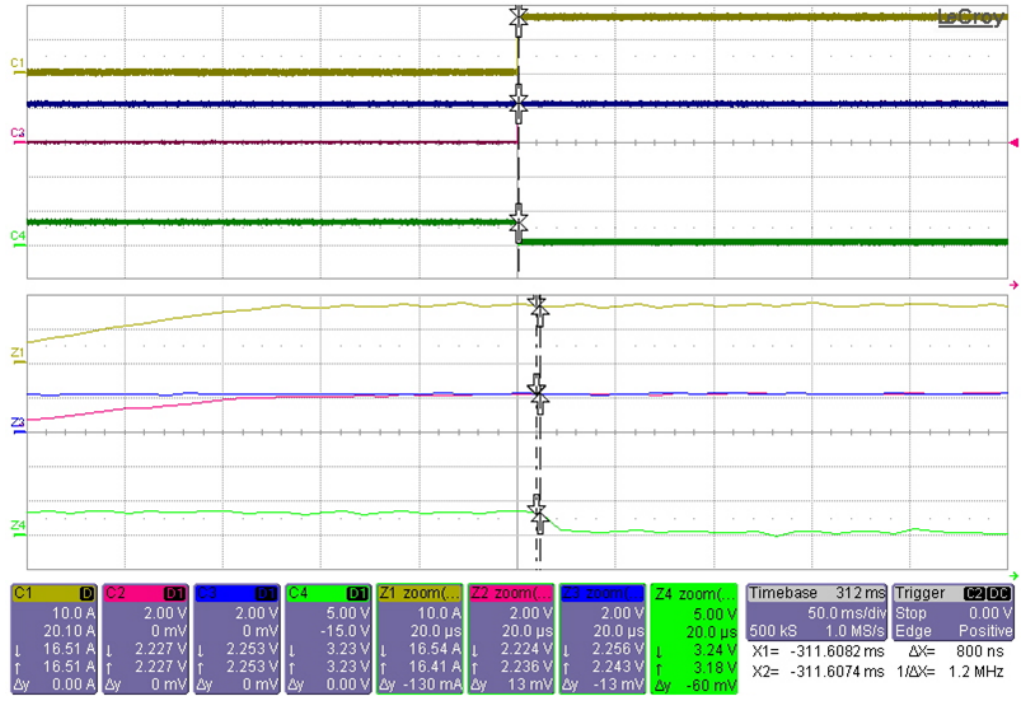


Figure 86. Overcurrent Detection at VTH (pos)—Zoomed

The waveforms shown in Figure 87 and Figure 88 indicate the sensing of overcurrent condition at negative threshold VTH(neg). The time required for the detection of the signal is 800 ns.

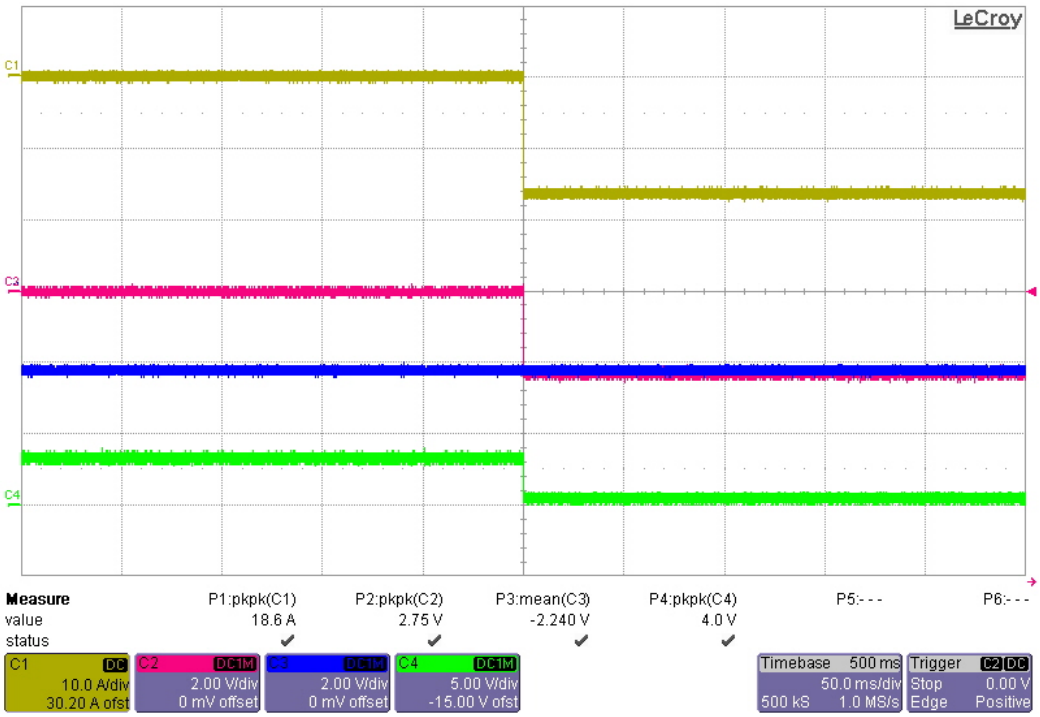


Figure 87. Overcurrent Detection at VTH (neg)

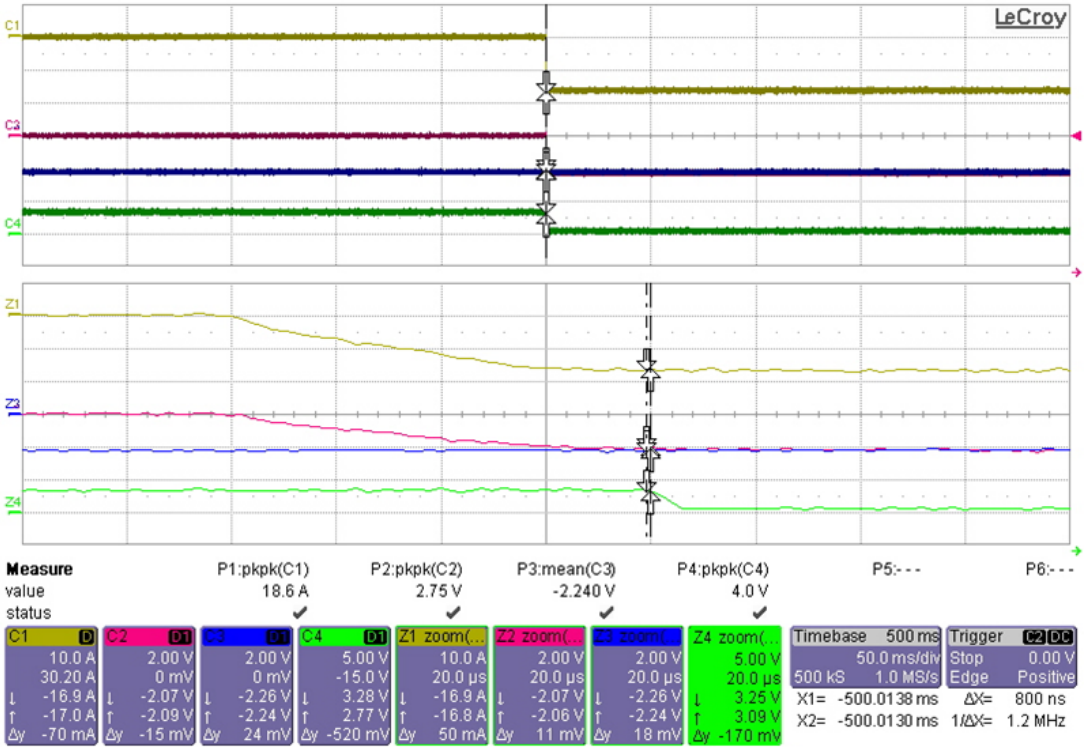


Figure 88. Overcurrent Detection at VTH (neg)—Zoomed

7.7 Testing with CT

This design has an option to connect external CT to connector J2. The burden resistor for CT still remains same (R6) as for LAH 25-NP.

NOTE: When tested with external CT, the resistor R84 should be unpopulated to prevent any error in the outputs.

CT turns ratio = 7: 3750
Burden resistor (R6) = 42.2 Ω

Table 7 shows the voltage measured at the output of bipolar signal conditioning circuit and the unipolar signal conditioning circuit.

Table 7. Test Results While Testing With CT

AC INPUT CURRENT (A)	OUTPUT VOLTAGE (V) FOR BIPOLAR SIGNAL CONDITIONING CIRCUIT	OUTPUT VOLTAGE (V) FOR UNIPOLAR SIGNAL CONDITIONING CIRCUIT
0	0.002 mV	0.001 mV
1	0.03975	0.03969
2	0.07951	0.07941
3	0.11935	0.11932
4	0.15898	0.15883
5	0.19875	0.19852
6	0.23851	0.23821
7	0.27818	0.27785
8	0.31796	0.31762
9	0.35765	0.35723
10	0.39743	0.39696
11	0.43713	0.43658
12	0.47692	0.47626
13	0.51664	0.51593
14	0.55635	0.55563
15	0.59668	0.59593
16	0.63660	0.63577

While the CT primary current is 8 A, Figure 89 and Figure 90 show the output voltage captured on the ADS7253 EVM for bipolar and unipolar signal conditioning circuit, respectively.

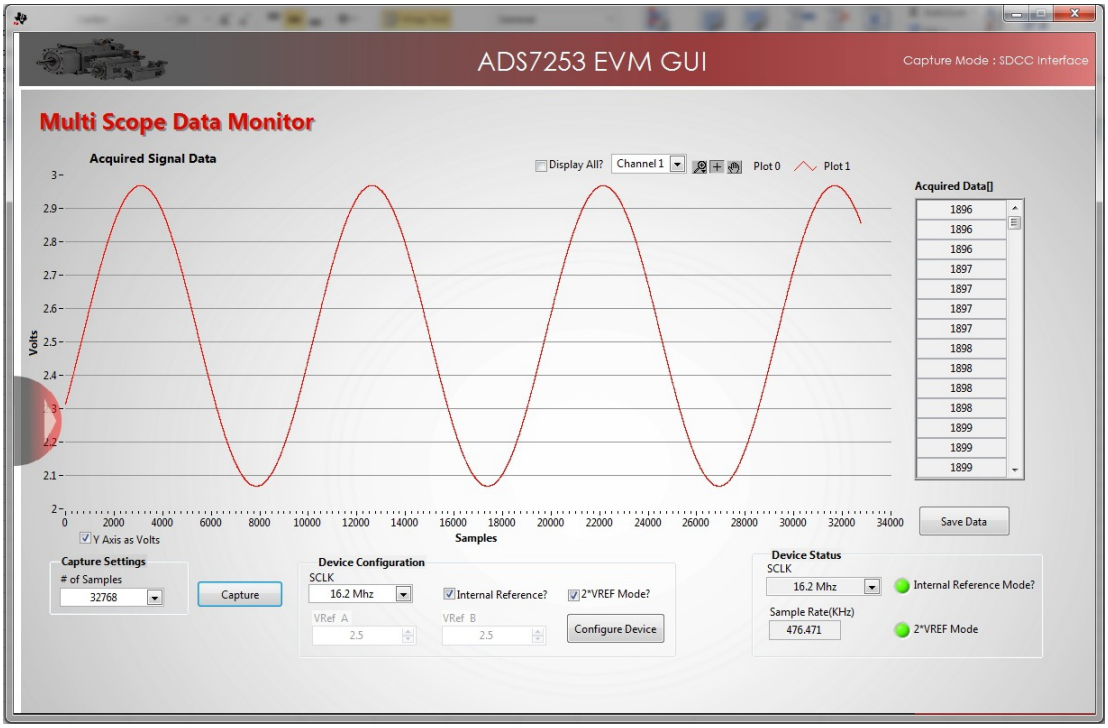


Figure 89. Output Voltage Captured While Testing With CT (Bipolar Signal Conditioning)

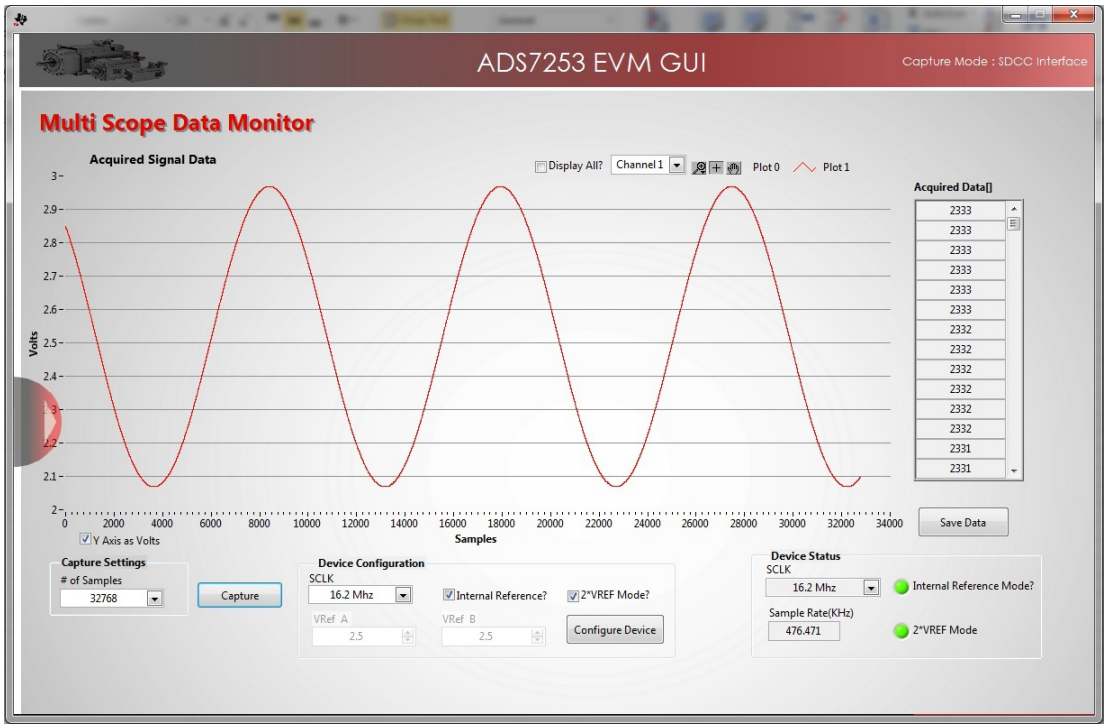


Figure 90. Output Voltage Captured While Testing With CT (Unipolar Signal Conditioning)

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00316.

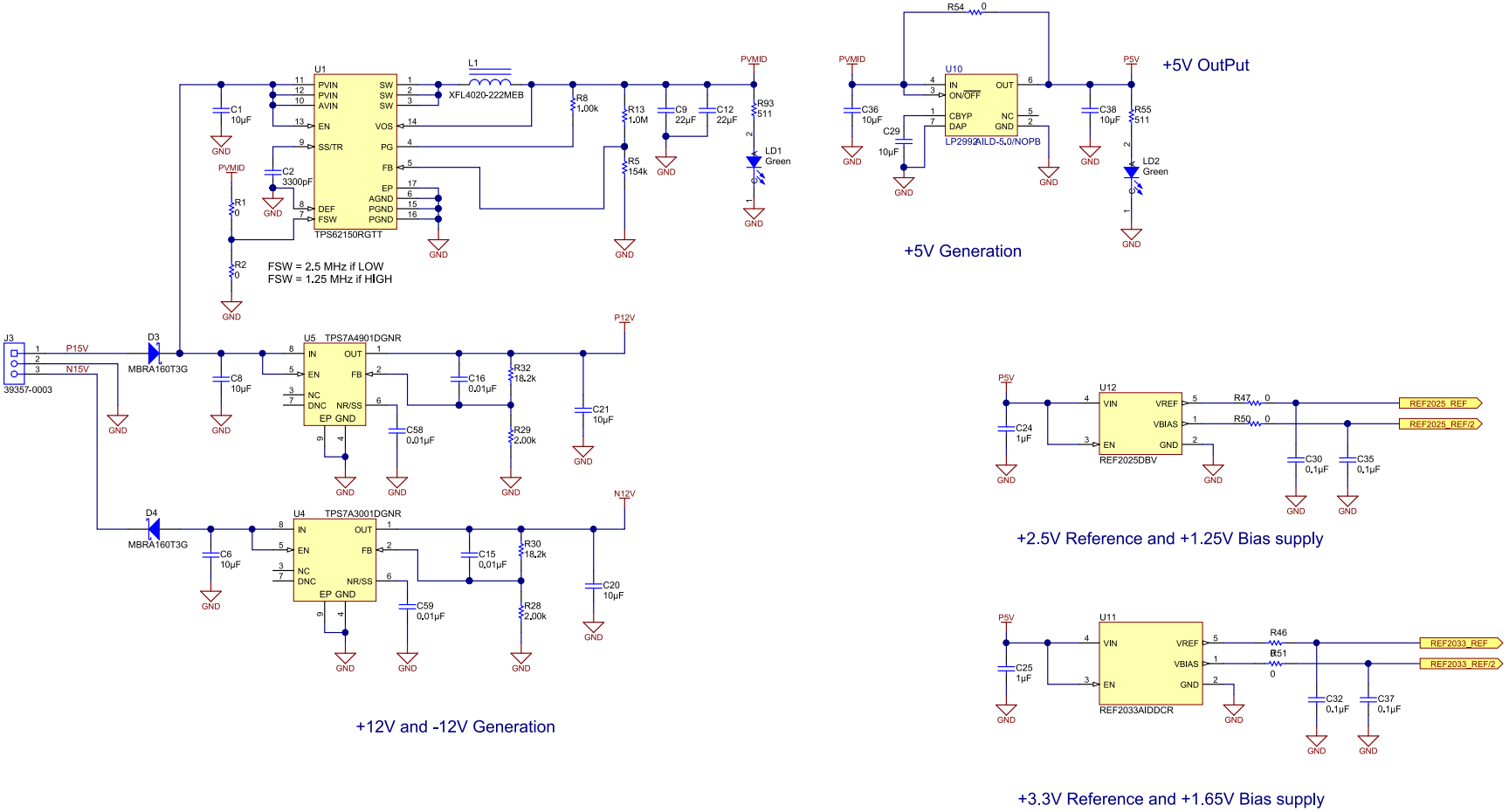
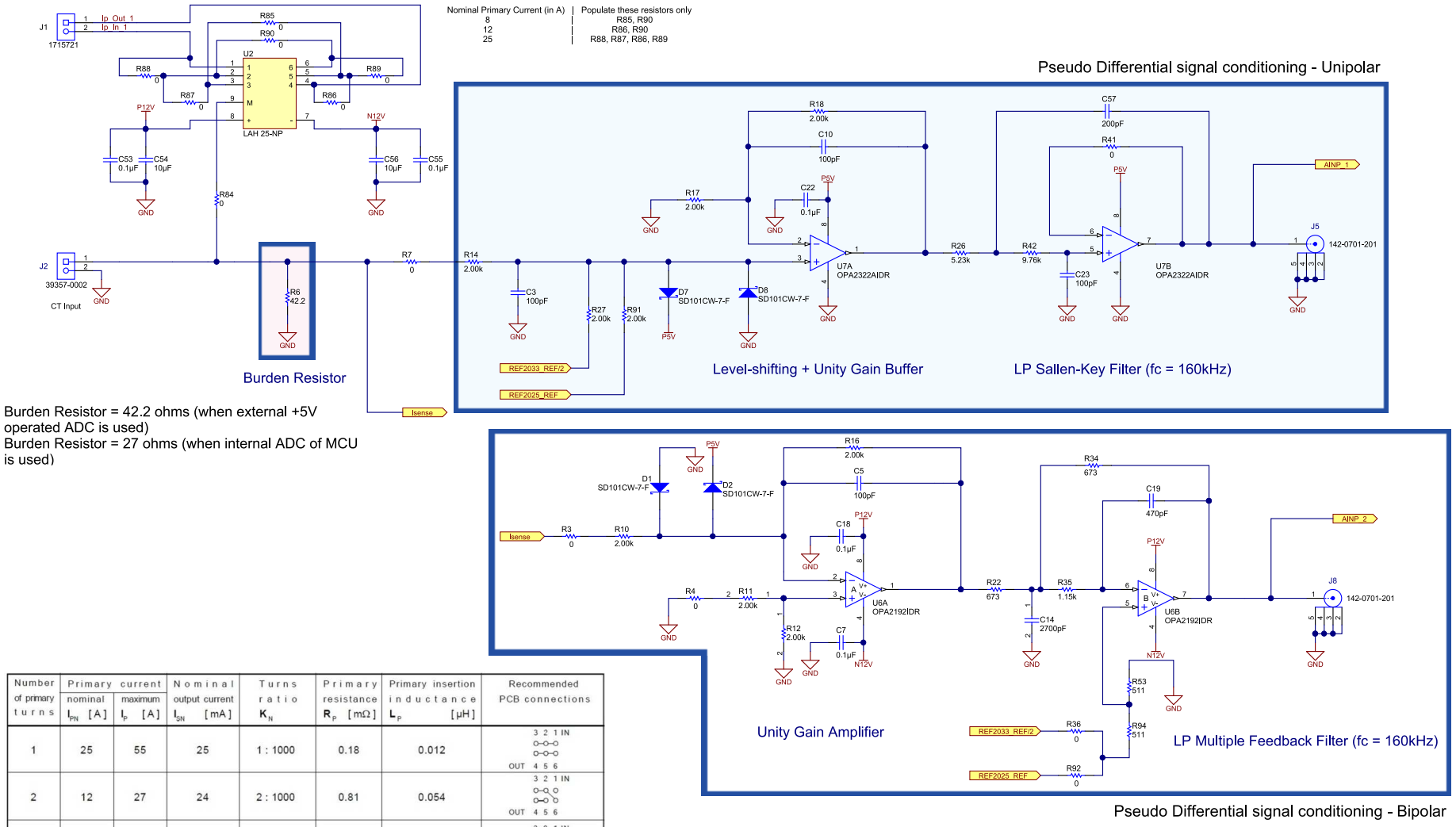


Figure 91. Power Supply Schematic



Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_p [mΩ]	Primary insertion inductance L_p [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	3 2 1 IN / OUT 4 5 6
2	12	27	24	2 : 1000	0.81	0.054	3 2 1 IN / OUT 4 5 6
3	8	18	24	3 : 1000	1.62	0.110	3 2 1 IN / OUT 4 5 6

Figure 92. Signal Chain—Pseudo Differential Schematic

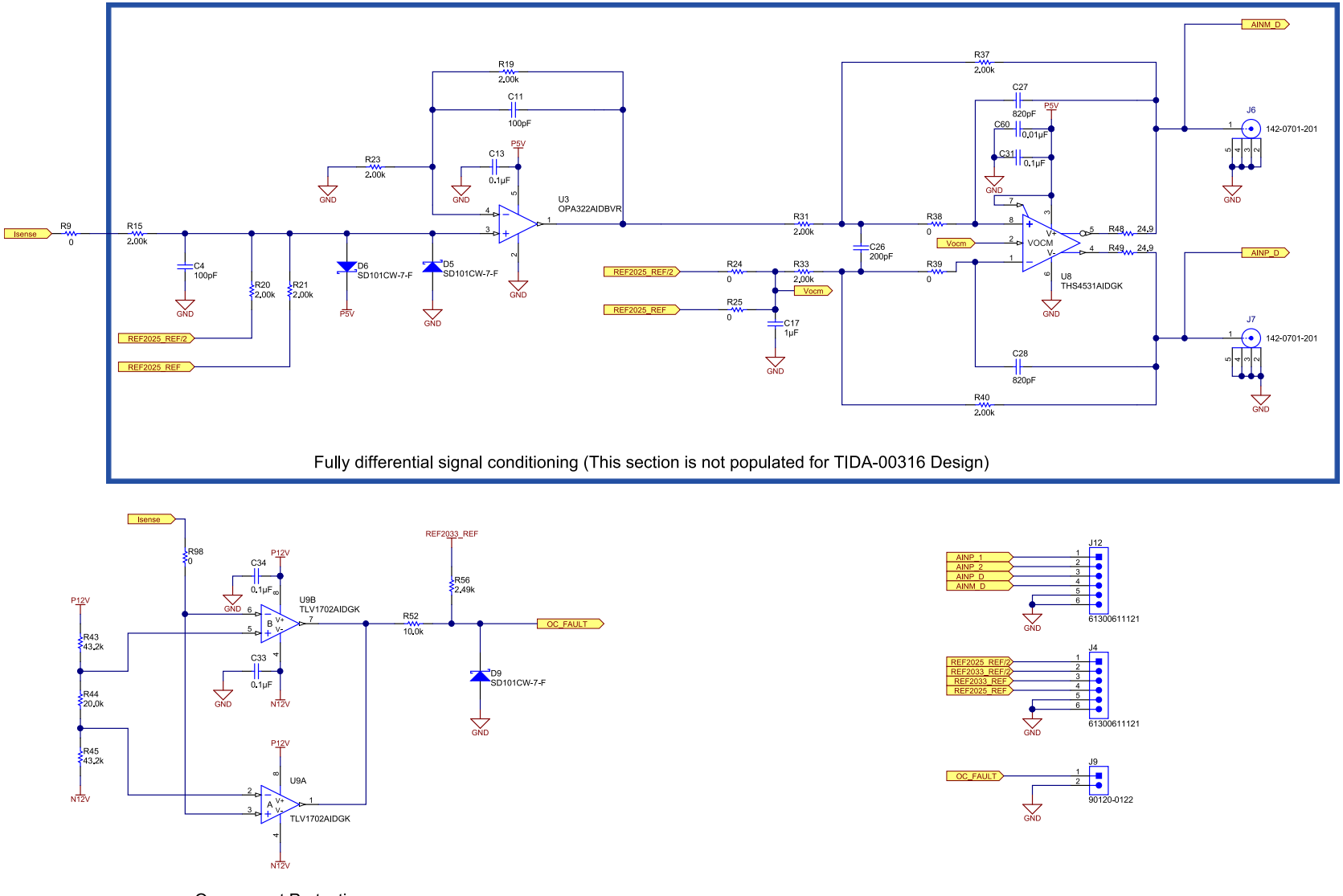


Figure 93. Signal Chain—Fully Differential + ADS7854 Schematic

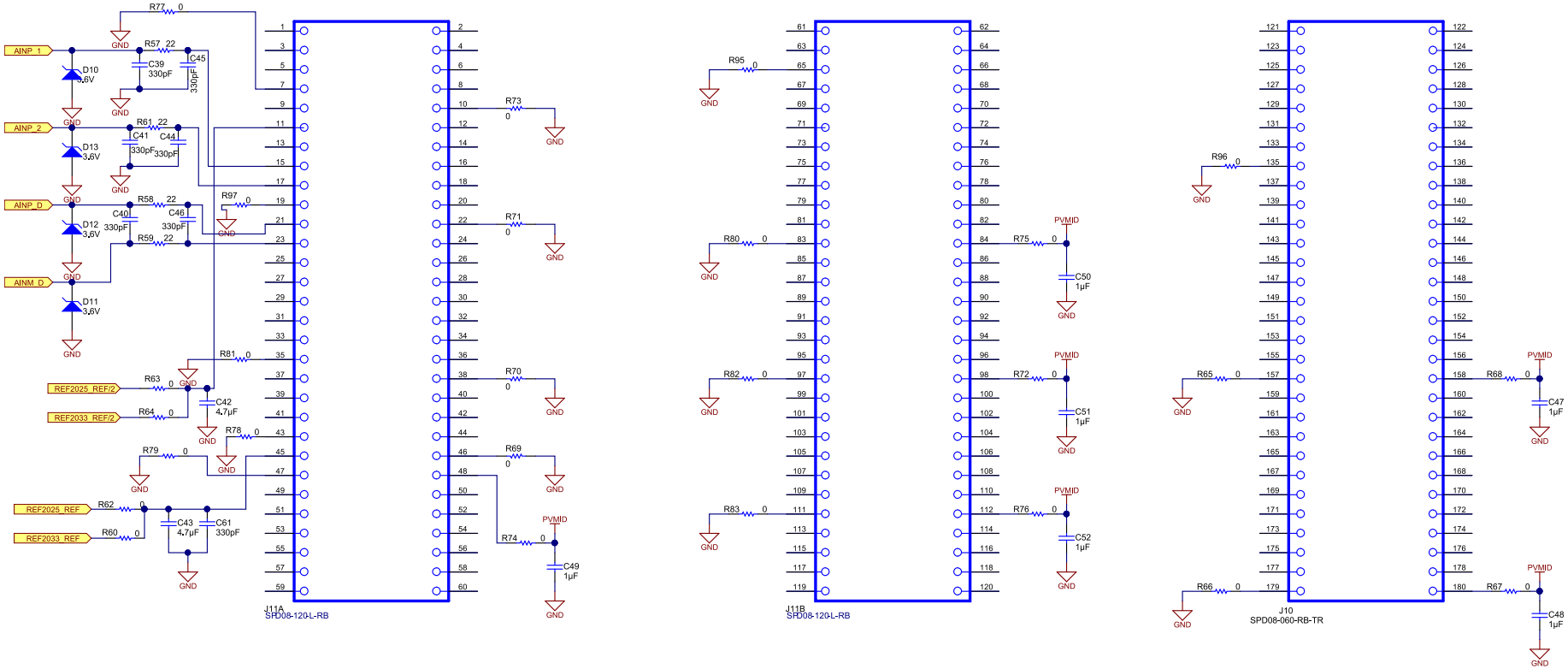


Figure 94. Delfino Controller Interface Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00316.

8.3 PCB Layout Recommendations

8.3.1 Layout of Unipolar Signal Chain

Figure 95 shows the layout of unipolar signal conditioning circuit (using OPA2322) on the TIDA-00316 board.

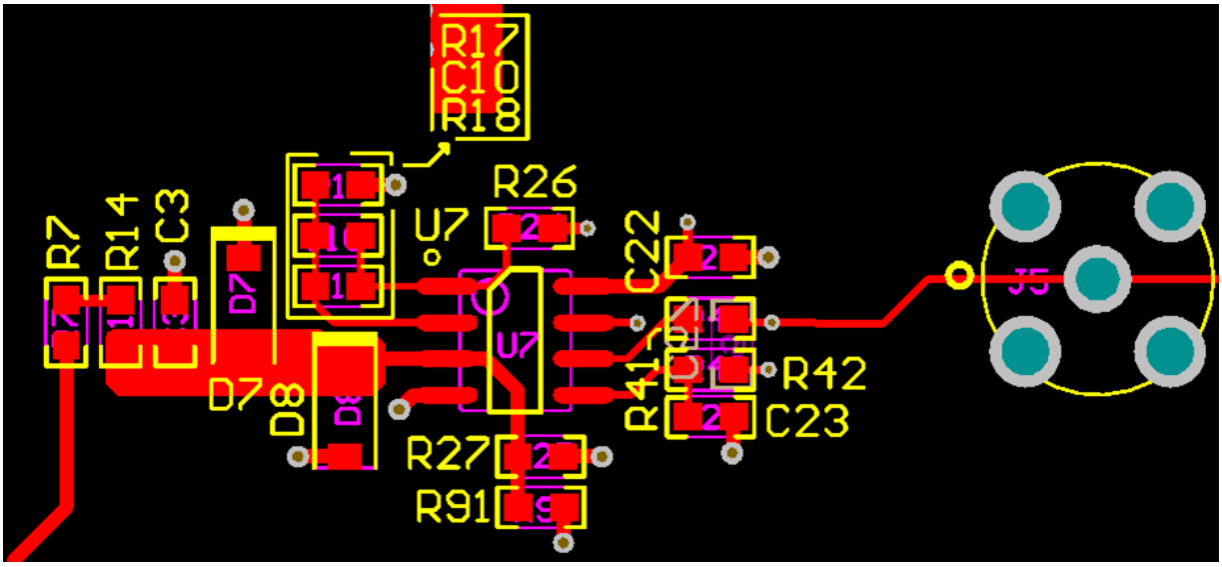


Figure 95. Layout of Unipolar Signal Conditioning Circuit

8.3.2 Layout of Bipolar Signal Chain

Figure 96 shows the layout of bipolar signal conditioning circuit (using OPA2192) on the TIDA-00316 board.

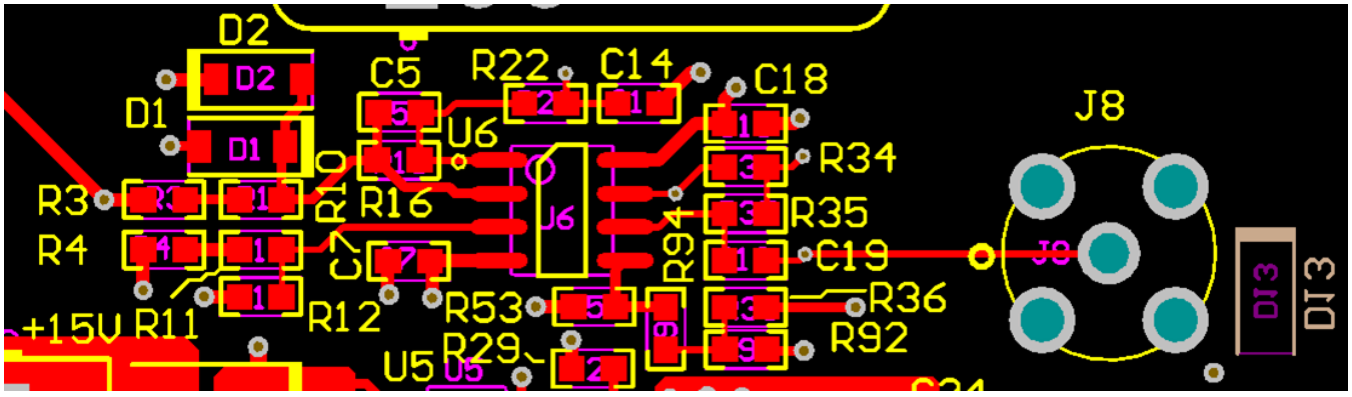


Figure 96. Layout of Bipolar Signal Conditioning Circuit

8.3.3 Layout of TPS7A4901 and TPS7A3001

The TPS7A4901 family of positive, high-voltage linear regulators achieves stability with a minimum input and output capacitance of 2.2 µF; however, TI highly recommends using a 10-µF capacitor to maximize AC performance. The input and output capacitors should be placed as close to the pin as possible, on the same side as the IC; do not use vias between the capacitor and the pin.

Do's and Don'ts:

- Place at least one, low-ESR, 2.2-µF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.
- Provide adequate thermal paths away from the device.
- Do not place the input or output capacitor more than 10 mm away from the regulator.
- Do not exceed the absolute maximum ratings.
- Do not float the Enable (EN) pin.
- Do not resistively or inductively load the NR/SS pin.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC. Every capacitor (CIN, COUT, CNR/SS, and CFF) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself. Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively and even cause instability. Figure 97 shows the layout of the TPS7A4901 and TPS7A3001 done on the TIDA-00316 board.

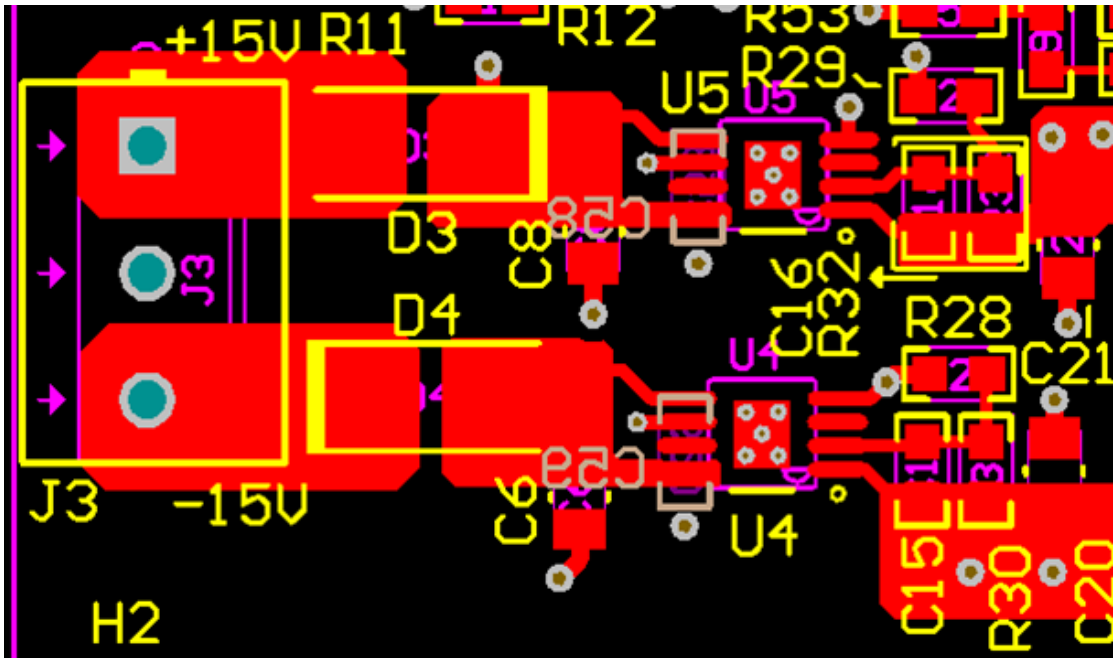


Figure 97. Layout of TPS7A4901 and TPS7A3001

8.3.4 Layout for TPS62150

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62150 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

Both AGND and PGND pins are directly connected to the exposed thermal pad. On the PCB, the direct common ground connection of AGND and PGND to the exposed thermal pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to VOUT at the output capacitor. Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops that conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated. Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As signals carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane. The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

Figure 98 shows the layout of the TPS62150 on the TIDA-00316 board.

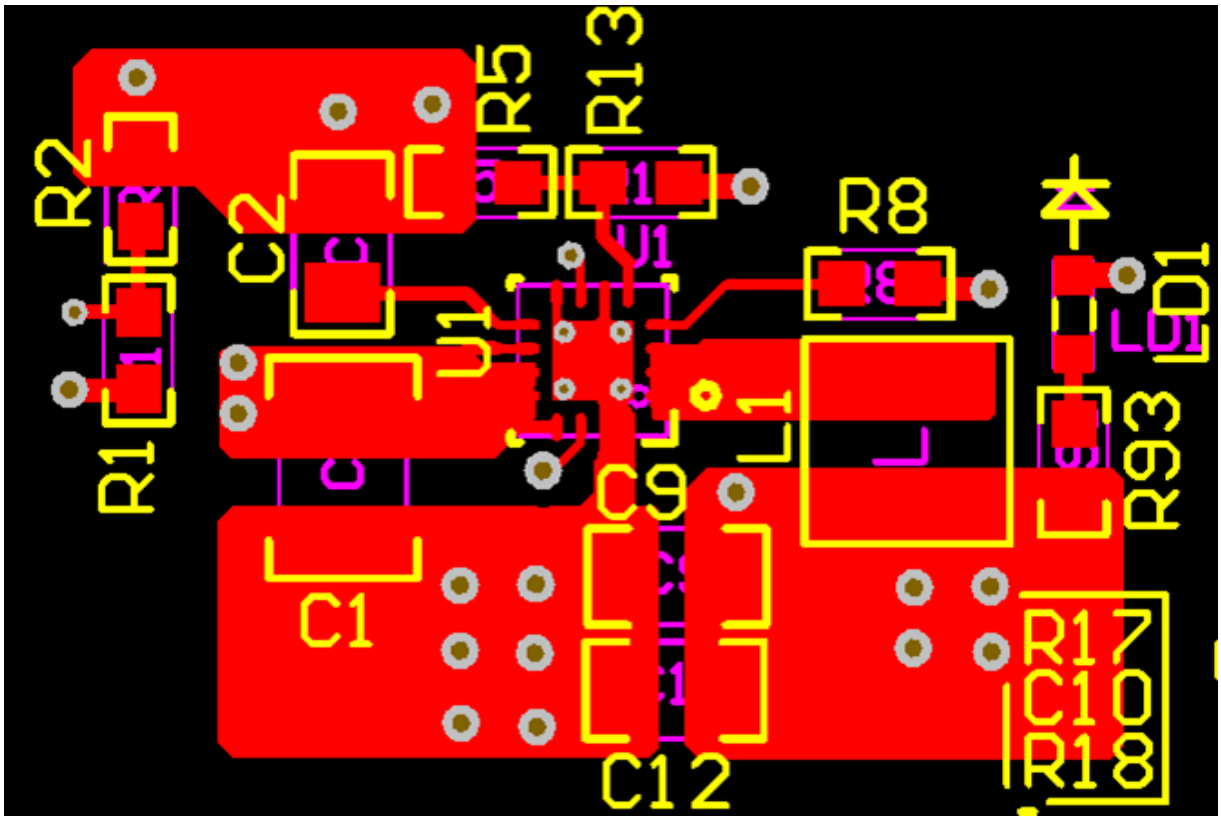


Figure 98. Layout of TPS62150

8.3.5 Layout of REF20xx

Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF}, and V_{BIAS} of the REF20xx.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Figure 99 shows the layout of the REF2025 and REF2033 on the TIDA-00316 board.

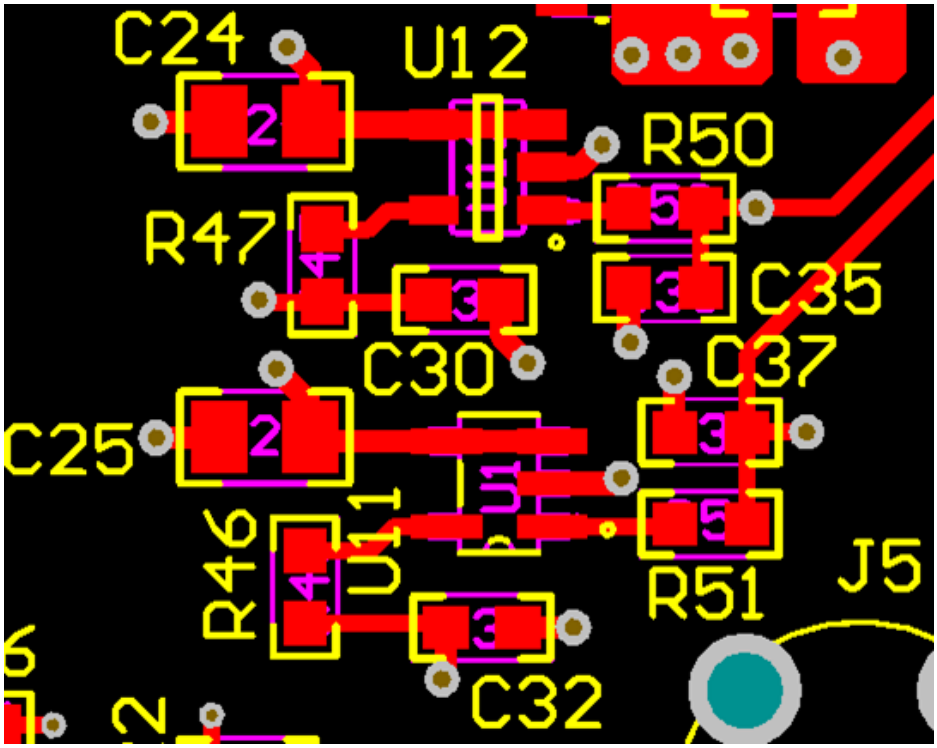


Figure 99. Layout of Voltage Reference Devices

8.3.6 Layout of Anti-Aliasing Filters for Control Card

The anti-aliasing filters for ADC inputs are not available on the Delfino Control Card. Therefore, they are provided on the TIDA-00316 PCB. Figure 100 shows these filters:

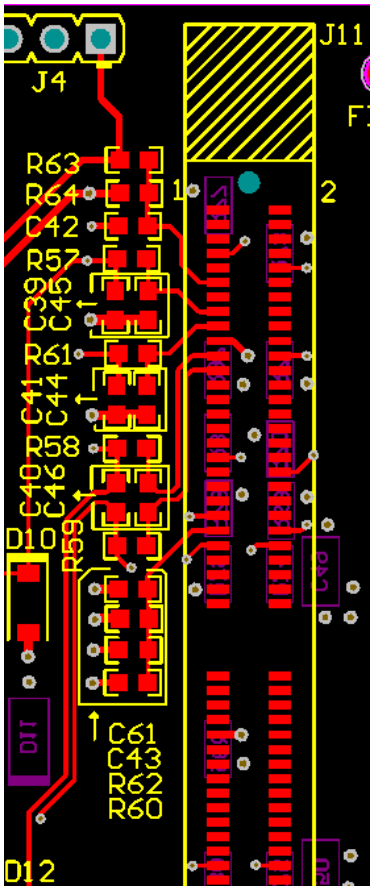


Figure 100. Layout Capture for ADC Input (and Filter Components) for Delfino Control Card

8.3.7 Layout of Sensor LAH 25-NP

The layout of LAH 25-NP is shown in Figure 101. Note the traces from which current would be passing are thick.

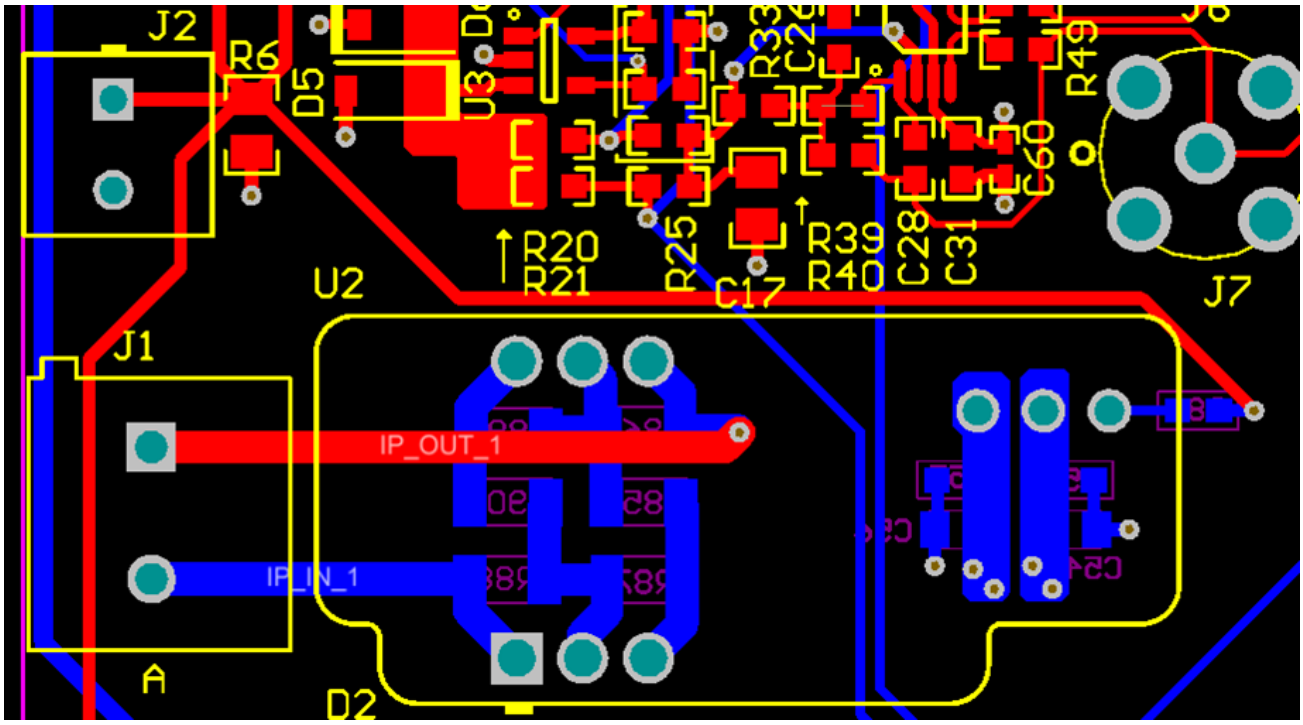


Figure 101. Sensor Circuit

The current, measured in the motor drive, can have higher voltages that need special isolation and spacing on the board. Figure 102 and Figure 103 show that there is no ground plane or power plane placed below the sensor as well as the input connector.

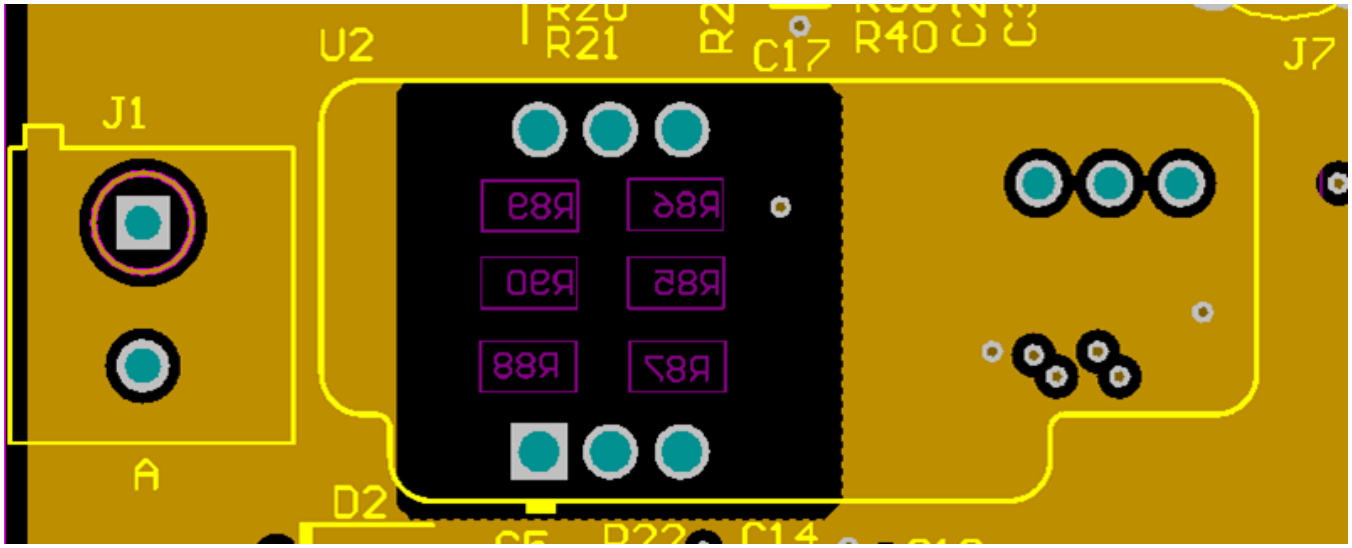


Figure 102. Cut in Ground Plane for Isolation to High-Voltage Sections

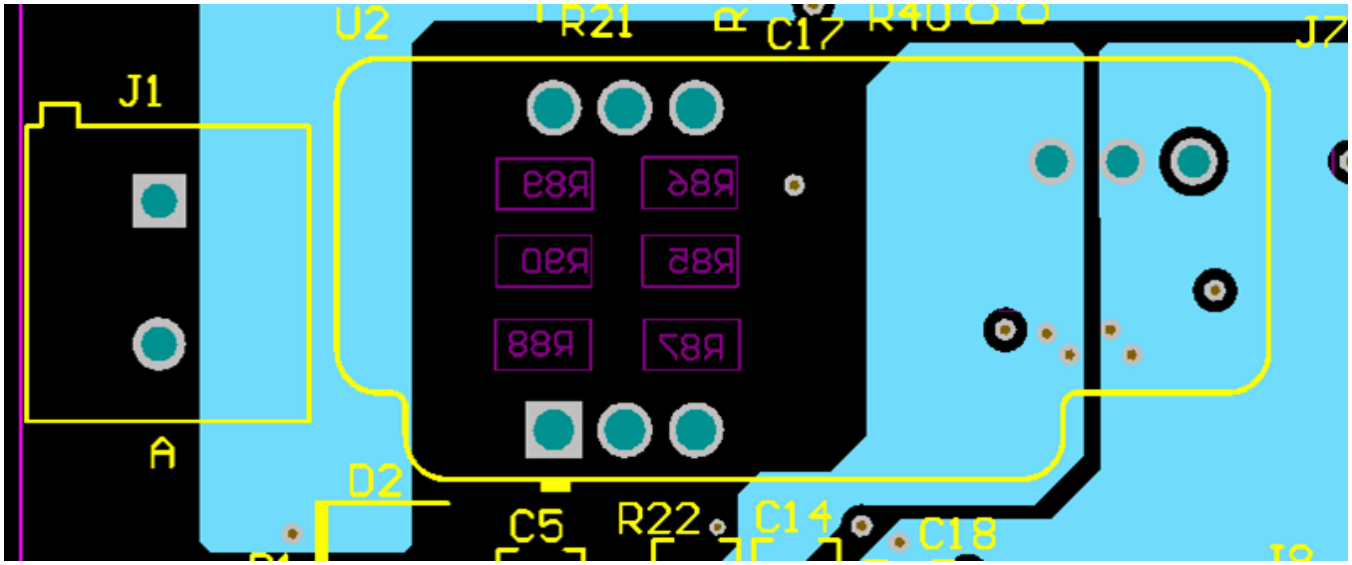


Figure 103. Cut in Power Plane for Isolation to High-Voltage Sections

8.3.8 Ground Plane and Power Planes

Figure 104 shows the power plane for the TIDA-00316 PCB.

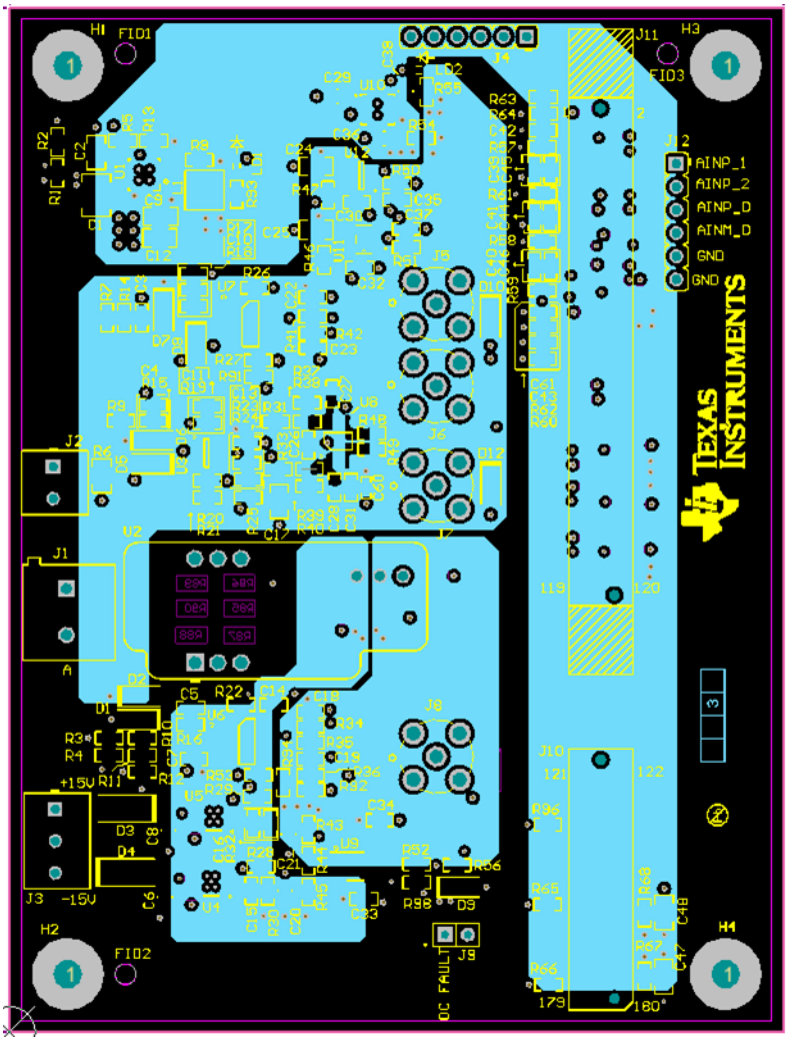


Figure 104. Power Planes

Figure 105 shows the ground plane for the TIDA-00316 PCB.

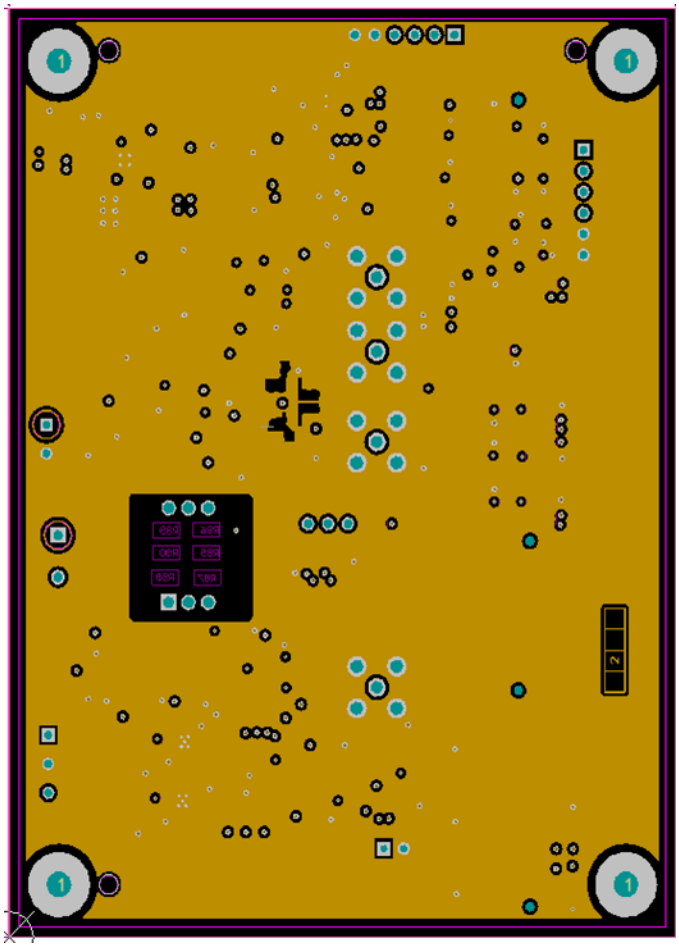


Figure 105. Ground Plane

8.3.9 Layer Plots

To download the layer plots, see the design files at TIDA-00316.

8.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00316.

8.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00316.

9 References

1. LEM Technologies (www.lem.com)
2. LEM Component publication: *Closed Loop Transducers with small footprint up to 100A nominal* (www.lem.com)
3. Smart Sensors for Industrial Applications (Editor: Krzysztof Iniewski)
4. FilterPro™ Software (http://www.ti.com/tool/filterpro)
5. Texas Instruments, *FilterPro™ User's Guide* (SBFA001)

10 Acknowledgment

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Revision History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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