*TI Designs*

# *AFE Using High-Speed ADC and Differential Amplifier for Digital Fault Recorder or TWFL Reference Design*

## Design Overview

A transient recorder can record and depict fast transients. The key principle for transient measurement is its high sampling rate. A DFR detects oscillatory transients, which tends to occur at frequencies of 1 MHz or less. Impulsive transients peak and decay in microseconds. To capture impulsive transients, the sampling rate must be 2 MHz (33,333 samples per cycle) or faster (166,000 samples per cycle or more).
This TI Design demonstrates capturing +ve or –ve transient waveforms ≤ 2.5-kV peak for DFR (up to 1 MHz) and transient recorder (up to 25 MHz) with a resolution of 12- to 14-bits and an accuracy < 10%. The AFE can be used to measure partial discharge measurement in medium-voltage (MV) power systems.

## Design Resources

| | |
|---|---|
| TIDA-00499 | Tool Folder Containing Design Files |
| ADC3421 | Product Folder |
| ADC3441 | Product Folder |
| ADS9120 | Product Folder |
| ADS8354 | Product Folder |
| ADS7854 | Product Folder |
| ADS7254 | Product Folder |
| THS4531 | Product Folder |
| THS4521 | Product Folder |
| THS4551 | Product Folder |
| LM4140 | Product Folder |
| REF5025 | Product Folder |
| TPS7A6550 | Product Folder |
| TPS62080 | Product Folder |
| AM3352 | Product Folder |
| OPA322 | Product Folder |

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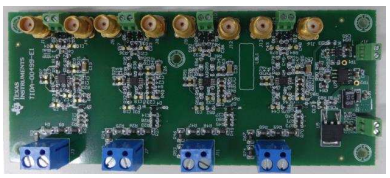
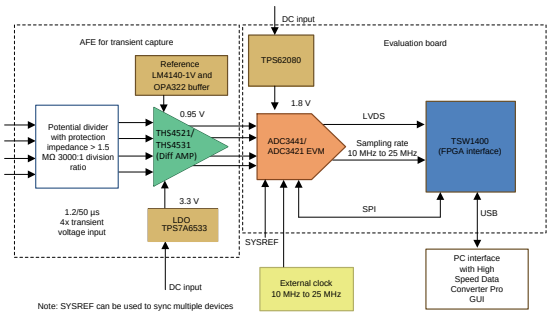


## Design Features

- Captures Transients up to Four Channels Simultaneously
- Captures 1.2/50-µs Transients at > 10 MHz and up to 25 MHz (166,000 Samples per Cycle or More) Using ADC3441 (14-bit) or ADC3421 (12-bit) ADC
- Transients Fault Recording of 17/20-µs up to 1 MHz Using ADS9110 (18-bit), ADS8354 or ADS9120 (16-bit), ADS7854 (14-bit), or ADS7254 (12-bit)
- Differential Amplifier Front-End (THS4531, THS4521, or THS4551) to Interface Transient Inputs to ADC With Onboard Reference of 0.995 V (1.024 V) or 2.5 V
- Differential Amplifier Interfaced to ADC3441/ADC3421 EVM and TSW1400EVM (High-Speed Data Capture Platform) for Transient Capture and ADS8354EVM-PDK or ADS9120EVM-PDK With AM3352 for DFR
- Capture Input Voltage Transient From 250 V to ≥ 2-kV Peak, 1.2/50 µs With ± 20-V Resolution From 10% to 100% of Input Voltage Range With Accuracy of < ±10% ±15 V From 10% to 100% of Input Voltage (at > 10 kHz) for Transient Capture
- Measurement Accuracy < 1% at 50 Hz for DFR
- Meets EMC Pre-Compliance Test as per IEC61000-4-5 up to 4 kV With 42-Ω Impedance

## Featured Applications

- Transient Recorder and Digital Fault Recorder
- Traveling Wave Fault Locator (TWFL)
- Sequence of Even Recorder (SOE)
- Sequence of Fault Recorder (SFR)



# 1 Design Theory—Transient and Digital Fault Recorders

The faults on overhead transmission lines can be divided into three categories:

- Permanent faults
- Intermittent or recurring faults
- Transient faults

Transient over-voltages (widely termed as surges) are short (micro- or millisecond) duration increases in voltage between two or more conductors. Direct lightning strikes to high- and low-voltage (HV/LV) power cables or telephone lines result in discharge flashovers to the earth or ground, causing line-to-line overvoltage transients and a flow of part of the lightning current along the line to electric equipment. Indirect strikes, coupled into electrical services, through resistive, inductive and capacitive effects can cause transients when discharge currents attempt to flow through conductors, circuits, and other electrical equipment.

Surge transients are caused by overvoltages from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults, such as short circuits and arching faults to the grounding system of the installation. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes.

The problems caused by transient overvoltages, whether induced by lightning or electrical switching, range in consequence level and can be broadly classified into disruptions, degradation, damage, and downtime.

- Disruptions result in no physical damage, but can be a nuisance to electronic systems often involving data loss, software corruption, system crashes or lockups, and spurious tripping.
- Degradation is the gradual deterioration of components due to long-term, lower-level transient overvoltages reducing the life of components and increasing susceptibility to premature failure.
- Damage manifests in burnt-out circuit boards through overheating and insulation failure and is exacerbated by the subsequent power follow-on. Damage can also occur because of mal-operation or short-circuits caused by the transient overvoltage.
- Downtime is the interruption to work or operations resulting in lost business and increased costs.

## *1.1 Power Disturbances*

Transient recorders and digital fault recorders (DFR) are able to record problems related to power quality, as discussed in the following subsections.

### 1.1.1 Momentary Phenomena—Transients

Transients can be classified into two categories:

- Impulsive transients: An impulsive transient is a sudden non-power frequency change in the steady-state condition of voltage or current that is unidirectional in polarity (either positive or negative).
- Oscillatory transients: An oscillatory transient is a sudden, non-power frequency change in the steady-state condition of voltage or current that includes both a positive and negative polarity value.

### 1.1.2 Long-Duration Voltage Variations

Long-duration voltage variations are defined as the root mean square (RMS) variations in the supply voltage at a fundamental frequency for periods exceeding one minute. These variations are classified into overvoltages, undervoltages, and sustained interruptions. An overvoltage (or undervoltage) is a 10% or more increase (or decrease) in RMS voltage for more than one minute.

Common voltage and power disturbances are:

- Overvoltage and undervoltage
- Swell, sag, and interruption
- Notch
- Transient
- Flicker
- Harmonic distortion
- Electrical noise

## *1.2 Transients*

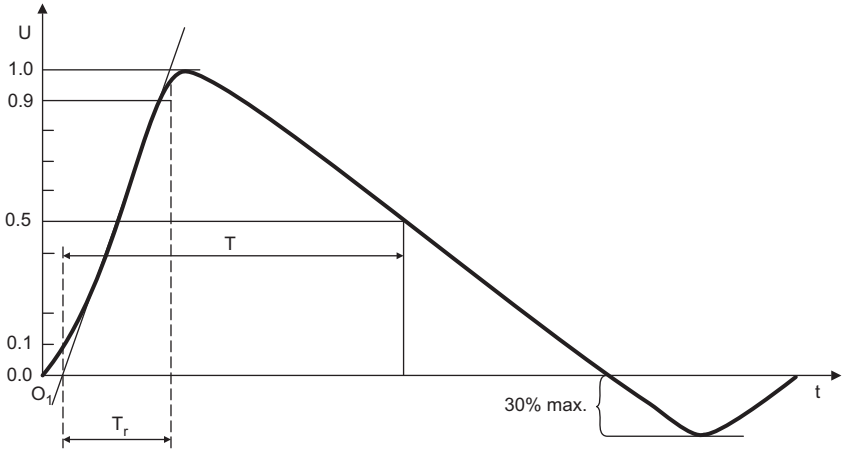
An impulsive transient is a sudden, non–power frequency change in the steady-state condition of voltage, current, or both that is unidirectional in polarity (primarily either positive or negative). IEC 61000-4-5 addresses the most severe transient conditions on power lines, which are transients caused by lightning strikes and switching. The IEC 61000-4-5 standard defines a transient entry point and a set of installation conditions. The transient is defined in terms of a generator producing a given waveform and having specified open-circuit voltage and source impedance.

Two surge waveforms are specified: the 1.2- x 50-µs open-circuit voltage waveform and the 8- x 20-µs short-circuit current waveform.

### 1.2.1 Transient Voltages Defined

What the industry calls transients are actually transient voltages. More familiar terms may be surges or spikes. Switching transients, or extremely brief periods of overvoltage, inflict damage in less than a millionth of a second, far less time than the sampling interval of traditional power management software. Damage may be incurred in both hardware and software, resulting in burned circuitry, component stress or failure, and memory and data losses.

The open-circuit voltage waveform of the 1.2/50-µs shape has a front time of 1.2 µs and a time-to-half value of 50 µs (see Figure 1).




Front time: $T_r$ = 1.2 µs ± 30%
Time to half-value: T = 50 µs ± 20%

**Figure 1. Waveform of Open-Circuit Voltage (1.2/50 µs)**

The short-circuit current waveform of the same generator has an 8-μs front time and a 20-μs time-to-half value (see Figure 2).

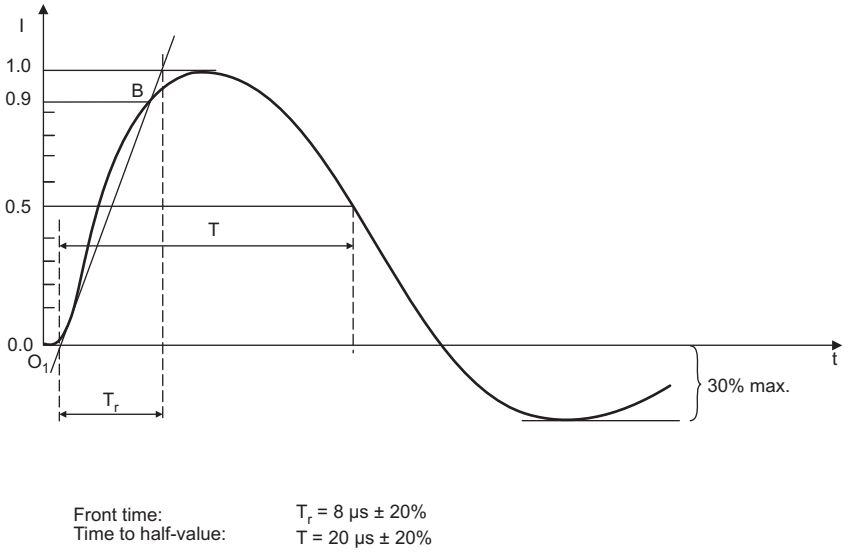



**Figure 2. Waveform of Short-Circuit Current (8/20 μs)**

### 1.2.2 Impulsive Transients

An impulsive transient is a sudden, non-power frequency change in the steady-state condition of a voltage waveform, current waveform, or both that is essentially in one direction, either positive or negative, with respect to those waveforms. The most common cause of this type of transient is lightning. The following Figure 3 shows a typical impulsive transient (at point X) occurring on a normal voltage waveform. The magnitude of such a transient can be many times larger than the peak value of the normal voltage waveform.

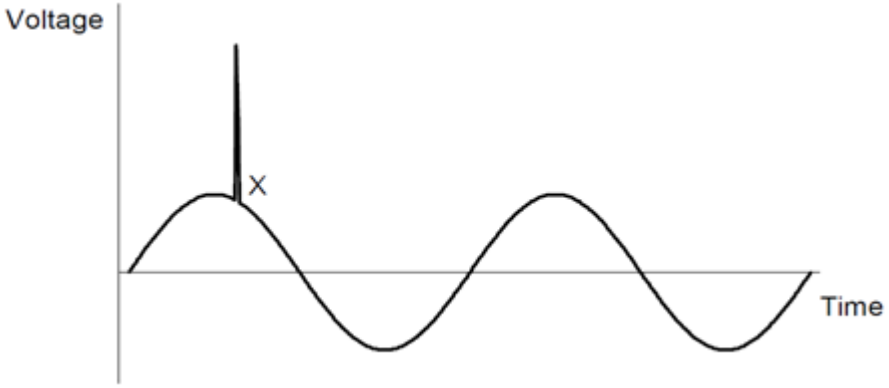



**Figure 3. Impulsive Transient Showing Point X**

## *1.3 Transient Recording*

Instead of sampling a few times a cycle, a transient recorder samples several times every millionth of a second on all voltage input channels and neutral-to-ground. Instead of reporting the simple trends of past events, a transient recorder can apply statistical measures to create actionable insights and plot power events against a “power profile”, which describes the comfort zone for a user’s critical equipment.

Rather than just logging the fact that a power disturbance took place, a transient recorder can accurately capture and display the waveform of the event, which enables a more sophisticated analysis and troubleshooting.

With the accuracy of high-rate sampling, coupled with analytic insights, a transient recorder represents an entirely different category in power monitoring. Transient recorders are installed at the substation along transmission and distribution systems, manufacturing centers, enterprise data centers, hospitals, and anywhere else where clean, continuous power is essential for high-value equipment and operations.

### 1.3.1 Subcycle—Very-Fast Transient Recorder (> 1 MHz)

Transients often cause intermittent, expensive periods of downtime. The subcycle transient recorder allows the user to:

- Record subcycle transients at a ≥ 10-MHz resolution
- Monitor switching noise from capacitors, static transfer switches, silicon control rectifiers (SCRs), and other devices that negatively impact power quality
- Perform essential tasks for critical applications such as hospitals, wafer fabrication plants, data centers, and other high-power, quality-sensitive applications

The following are features of a typical sub-nano second transient recorder:

- 10-MHz recorder (up to 166,000 samples per cycle)
- EN61000-4-30 Class A compliant power quality measurements (certified)
- Statistical reporting providing easy-to–understand, weekly reports on power quality
- Dual Ethernet ports with separate and secured IP addresses
- Fiber optic over Ethernet
- High-speed communication to deliver high-performance results

### 1.3.2 Fault Recorder—Subcycle Transient Recorder (< 1 MHz)

High-speed transient recorders are used to analyze switching transients and lightning strikes. This type of transient recorder simultaneously captures impulsive transients for four or more voltage channels for subcycle disturbance. High-speed transient recorders also detect and capture short transients as short as 20 μs at 50 Hz (17 μs at 60 Hz) to identify problems as result of short disturbances, for example, the switching of capacitors and so forth. Transients are measured relative to the ground and can be measured up to 2 kV. A fault locator calculates the distance to a fault based on the configurable line model.

## *1.4 Other Applications*

### 1.4.1 Waveform Capture

A protection relay or power quality analyzer (PQA) provides oscillograph-recording capabilities. These relays or PQAs record all measured signals along with the binary signals of pickup, trip, logic, and contact closures. The measured signals are captured at 256, 512, or 1024 samples per cycle. The waveform recorder captures a fixed number of records or pre-trip data for cases that use a protection relay or a fixed amount of records for cases that use a power quality analyzer. The user can retrieve the stored data in a COMTRADE compatible file format such as a *.csv*. When a trip or a fault occurs, data capture is halted and a date and time stamp is added.

### 1.4.2 Traveling Wave Fault Location (TWFL) in Power Transmission Lines (HV/MV)

Faults in power grid transmission lines often occur in remote locations and repairing them can be time consuming, especially if the location of the fault is unknown. Traveling wave fault location (TWFL) is a method of estimating the location of a fault based on measuring the difference in arrival times of fault artifacts at the two ends of a faulted line. Faults on overhead transmission lines cause transients that travel at the speed of light and propagate along the power line as traveling waves (TWs). TW methods use the naturally occurring surges and waves that are generated by the fault. The accuracy in fault location depends upon the sampling frequency. Because the speed at which the wave travels over transmission lines is slightly lower than light speed, to achieve higher accuracy, a very high sampling frequency must be used in TWFL methods.

## *1.5 TIDA-00499 System Description and Functionality*

### 1.5.1 System Description

The TIDA-00499 analog front-end (AFE) has been designed to be interfaced to the ADC34xx high-speed analog-to-digital (ADC) family for transient recording and the ADSxx54 successive approximation register (SAR) ADC family for digital fault recording. The references, power supply regulator, and potential divider values change for both applications. To make the system design simple, the two design files for both boards have been provided (see Section 8 *Design Files*). Customers can use the design information depending on the application.

This design demonstrates the analog input capturing functionalities that can be used in a transient recorder or digital fault recorder.

The TIDA-00499 TI Design demonstrates the following:

- Fast transient capture of 1.2/50 µs at a sampling rate of up to 20 MHz for transient response and transient capture of 17/20 µs at a sampling speed of up to 1 MHz for DFR
- Using the AFE to measure a transient input of 2 kV to 2.5 kV, which overrides on a 50/60-Hz AC input voltage of 110 V or 230 V
- Attenuation of transient inputs using a potential divider (multiple resistors)
- Converting the transient input to a differential output level that is compatible to the differential ADC inputs used for TR and DFR
- Interfacing to simultaneous sampling ADCs with different resolutions (12-bit to 16-bit)
- Interfacing the ADCs to a signal processing board to control the ADC sampling and read the converted sample for further processing
- Interfacing to a graphical user interface (GUI) to plot the ADC waveform and also display the measured sample values
- Capturing values from ADC samples to a *.csv* file
- References and power supply regulator for AFE functionality are provided onboard
- AFE along with evaluation module (EVM) and data capture board can perform the TR or DFR function

### 1.5.2 Subcycle Very Fast Transient Recorder From 10 MHz to 25 MHz

This (transient recorder) TI Design demonstrates the following:

- Using an ADC3441 quad-channel, 14-bit, 25-Msps ADC or ADC342x quad-channel, 12-bit, 25-Msps ADC for sampling transient inputs of 1.2/50 µs
- Using a THS4531, THS4521, or THS4551 differential amplifier to convert the transient voltage inputs to different outputs compatible with the ADC inputs
- Using a LM4140-1.024 precision micropower, reference to generate 0.95 V
- Using a TPS7A6533 300-mA, 40-V, LDO regulator with ultralow quiescent current to generate a power supply for the AFE
- Interfacing to ADC3441 or ADC3421 EVM and TSW1400 high-speed data capture and pattern generation platform for capturing the voltage inputs
- Using the High Speed Data Converter Pro software for capturing and analyzing the transient inputs

### 1.5.3 Fault Recorder—Subcycle Transient Recorder (< 1 MHz)

This (DFR) TI Design demonstrates the following:

- Using an ADS9120 or ADS8354 SAR ADC, dual, 700-Ksps, 16-bit, simultaneous sampling, ADS7854 SAR ADC, dual, 1-Msps, 14-bit, simultaneous sampling, or ADS7254 SAR ADC, dual, 1-Msps, 12-bit, simultaneous sampling for sampling transients that are > 17 µs
- Using a THS4531, THS4521, or THS4551 differential amplifier to convert the transient voltage inputs to different outputs compatible with the ADC inputs
- Using a LM4140-2.5 precision, micropower reference to generate 2.5 V
- Using a TPS7A6550 300-mA LDO regulator with ultralow quiescent current to generate the power supply for the AFE
- Interfacing to a ADS8354EVM-PDK, ADS9120EVM-PDK, or ADS7854EVM-PDK for capturing the voltage inputs
- Using the ADS8353 EVM GUI for capturing and analyzing the transient inputs

### 1.5.4 TIDA-00499 Advantages

This design demonstrates using different TI ADC families (high-speed and SAR ADC) for transient recording and digital fault recording. This TI Design also demonstrates the use of other differential amplifiers which have a high slew rate and bandwidth. The advantage of these ADC families is scalability in terms of performance and resolution with pin compatibility. These advantages offer options for customers to choose the required ADCs based on specific requirements for system performance. This type of compatibility also helps customers optimize the design for both performance and cost. Maintaining compatibility between systems reduces the design cycle time and testing cycle time and also reduces the requirement to maintain multiple versions of a design.

# 2 Key System Specifications

## 2.1 Transient Recorder (TR)

**Table 1. System Specifications for Transient Recorder**

| SERIAL NUMBER | PARAMETERS | SPECIFICATION |
|---|---|---|
| 1 | Transient input range | ≤ 2500-V peak |
| 2 | ADC sampling rate | 10 MHz to 25 MHz |
| 3 | ADC resolution and type | 12- to 14-bit, simultaneous sampling, and pipeline |
| 4 | ADC input type and range | Differential, 2 VPP |
| 5 | Differential amplifier | Bandwidth: 36 MHz<br>Slew rate: 200 V/µs, 0.95-V common-mode output |
| 6 | Transient input type and range | 1.2/50 µs , ≥ 2-kV peak |
| 7 | Power supply | 1.8 V, 3.3 V |
| 8 | ADC interface | TSW1400 board based on EP4SGX70 FPGA |

## 2.2 Digital Fault Recorder (DFR)

**Table 2. System Specifications for DFR**

| SERIAL NUMBER | PARAMETERS | SPECIFICATIONS |
|---|---|---|
| 1 | Transient input range | ≤ 2000-V peak |
| 2 | ADC sampling rate | ≤ 1 MHz |
| 3 | ADC resolution and type | 12- to 16-bit, simultaneous sampling, and SAR |
| 4 | ADC input type and range | Differential, 0 V to 5 V |
| 5 | Differential amplifier | Bandwidth: 36 MHz<br>Slew rate: 200 V/µs, 2.5-V common mode output |
| 6 | Transient input type and range | 17/20 µs, ≥ 2-kV peak |
| 7 | Power supply | 5 V, 3.3 V |
| 8 | Interface | Serial data capture card (SDCC) – AMC3352 based |

## 3 Block Diagram

The block diagram in Figure 4 shows the connection of the transient capture signal conditioning board to the ADC3441 EVM. The clock for the EVM is provided externally.

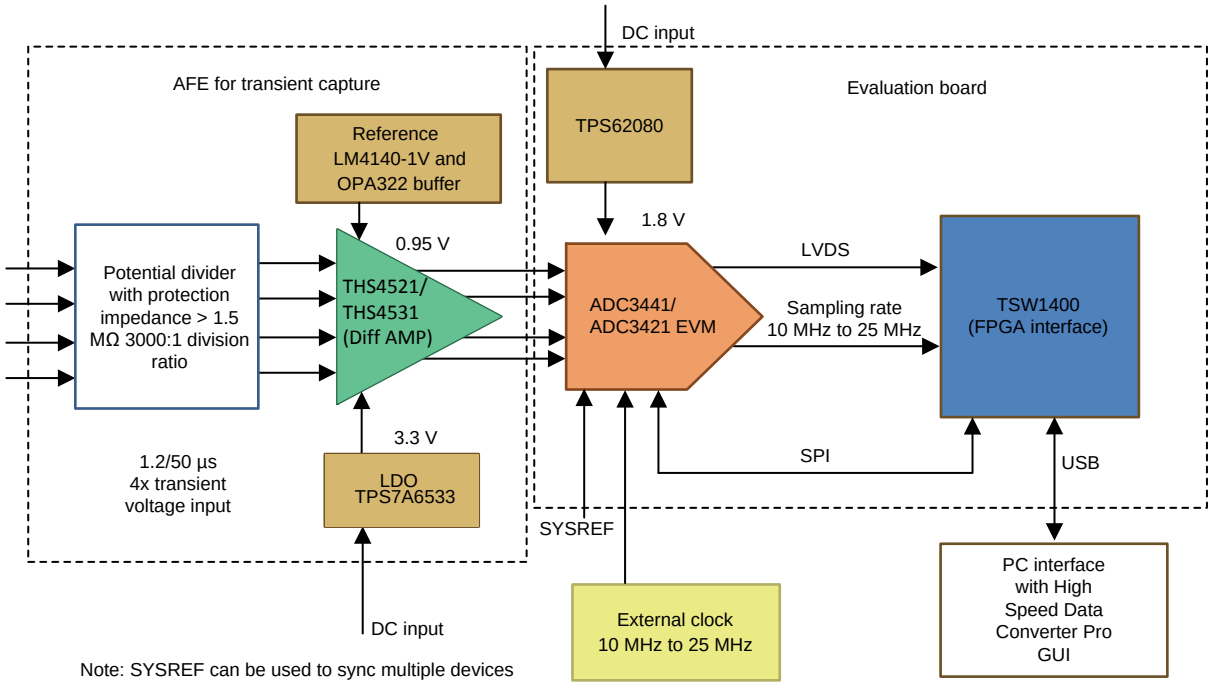



**Figure 4. Transient Recorder Block Diagram**

The block diagram in Figure 5 shows the connection of the digital fault recorder signal conditioning board to the ADSXX54 EVM.

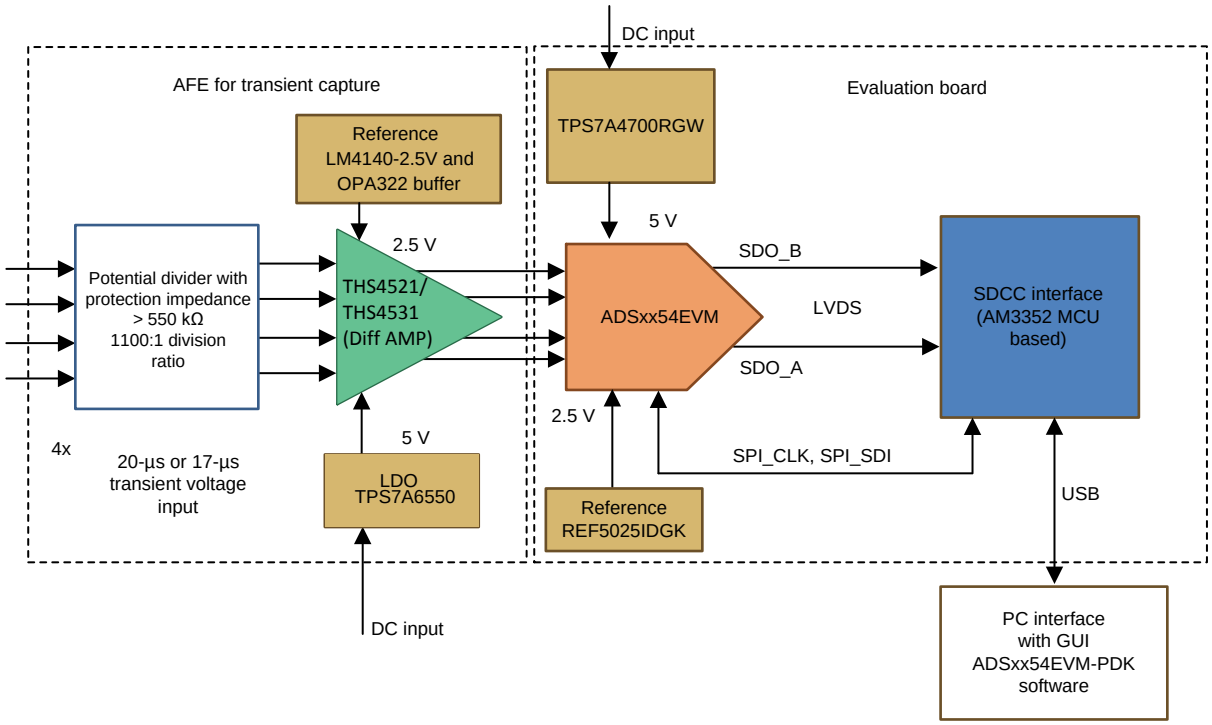



**Figure 5. Digital Fault Recorder Block Diagram**

## 3.1 Highlighted Devices

### 3.1.1 ADC for Transient Recorder and Digital Fault Recorder

#### 3.1.1.1 Transient Recorder

Transient recorders capture the AC input and transient input (50 Hz and 1.2/50 µs) at a high sampling rate. The sampling rate can be up to 20 MHz. Use either a 12- or 14-bit ADC resolution depending on the application. Choosing a 12-or 14-bit ADC resolution that is pin compatible reduces the design efforts and provides options for scalability. Some applications may require sampling the analog inputs at > 20 MHz with the sampling rate ranging up to 100 MHz. The number of channels measured by transient recorders varies from 4 to 16 with all channels synchronized. The ADC34xx family meets all the requirements to make it a good choice for transient recorder applications.

**ADC3421**

The ADC342x are a high-linearity, ultralow power, quad-channel, 12-bit, 25-Msps to 125-Msps, ADC family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC342x family supports serial low-voltage differential signaling (LVDS) to reduce the number of interface lines, which allows for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

**Features**

- Quad channel
- 12-bit resolution
- Single supply: 1.8 V
- Serial LVDS interface
- SNR = 70.2 dBFS, SFDR = 87 dBc at fIN = 70 MHz
- Ultralow power consumption:
  - 98 mW/ch at 125 Msps
- Channel isolation: 105 dB
- Internal dither and chopper
- Temperature range: –40°C to TMAX = 85°C
- Support for multi-chip synchronization
- Pin-to-pin compatible with 14-bit version

For more details on the ADC3421 device, refer to the product page: http://www.ti.com/product/adc3421.

**ADC3441**

The ADC344x are a high-linearity, ultralow power, quad-channel, 14-bit, 25-Msps to 125-Msps, ADC family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC344x family supports serial LVDS to reduce the number of interface lines, which allows for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

**Features**

- Quad channel
- 14-bit resolution
- Single supply: 1.8 V
- Serial LVDS interface
- SNR = 72.4 dBFS, SFDR = 87 dBc at fIN = 70 MHz
- Ultralow power consumption:
- 98 mW/ch at 125 Msps
- Channel isolation: 105 dB
- Internal dither and chopper
- Temperature range: –40°C to TMAX = 85°C
- Support for multi-chip synchronization
- Pin-to-pin compatible with 12-bit version

For more details on the ADC3441 device, refer to the product page: http://www.ti.com/product/adc3441.

#### *3.1.1.2 Digital Fault Recorder—ADS8354 (16 Bit), ADS7854 (14 Bit), or ADS7254 (12 Bit)*

Digital fault recorders capture the AC input and slow transient input (50 Hz and 17/20 µs) at a sampling rate up to 1 MHz. Depending on the application either 12-bit, 14-bit, or 16-bit ADC resolution is used. Choosing a 12-, 14-, or 16-bit ADC resolution that is pin compatible reduces the design efforts and provides options for scalability. The ADSxx54 family meets all the requirements that make it a good choice for digital fault recorder applications.

**ADSxx54 ADC family**

The ADS8354, ADS7854, and ADS7254 belong to a family of pin-compatible, dual, high-speed, simultaneous-sampling, ADCs that support fully-differential analog inputs. Each device includes two individually programmable reference sources that can be used for system-level gain calibration. Also, a flexible serial interface that can operate over a wide power-supply range enables easy communication with a large variety of host controllers. Power consumption for a given throughput can be optimized by using the two low-power modes supported by the device. All devices are fully specified over the extended industrial temperature range (–40°C to 125°C) and are available in pin-compatible, WQFN-16 (3-mm × 3-mm) and TSSOP-16 packages.

**Features**

- 16-, 14-, and 12-bit, pin-compatible family
- Simultaneous sampling of two channels
- Supports fully-differential inputs
- High speed:
  - ADS8354: 16 bits, 700 Ksps
  - ADS7854: 14 bits, 1 Msps
  - ADS7254: 12 bits, 1 Msps

- Excellent DC performance:
  - ADS8354:
    - 93-dB signal-to-noise ratio (SNR), –100-dB total harmonic distortion (THD)
  - ADS7854:
    - 14-bit NMC DNL, ±1.5-LSB max INL
  - ADS7254:
    - 12-bit NMC DNL, ±1-LSB max INL
- Excellent AC performance:
  - ADS8354:
    - 93-dB signal-to-noise ratio (SNR), –100-dB total harmonic distortion (THD)
  - ADS7854:
    - 88-dB SNR, –95-dB THD
  - ADS7254:
    - 72-dB SNR, –90-dB THD
- Dual, programmable, and buffered 2.5-V internal reference

For more details on the ADS8354 device, refer to the product page: http://www.ti.com/product/ads8354.

### 3.1.2 Differential Amplifier

The use of differential ADC inputs is preferential for TR and DFR applications. The transient voltage inputs are converted to differential inputs compatible with the ADC measurement range using the differential amplifiers. The voltage rise time requirement is specified up to 15 kV/µs. The bandwidth requirement for these amplifiers is 5 MHz or more. The THS4531 differential amplifier meets these requirements. The THS4521 has a higher slew rate and bandwidth than the THS4531 and can be used based on the system requirements.

**THS4531**

The THS4531 is a low-power, fully-differential op amp with an input common-mode range below the negative rail and rail-to-rail output. The device is designed for low-power data acquisition systems and high density applications where power consumption and dissipation is critical.

The device features accurate output common-mode control that allows for DC coupling when driving ADCs. This control, coupled with the input common-mode range below the negative rail and rail-to-rail output, allows for easy interface from single-ended ground-referenced signal sources to successive-approximation registers (SARs) and delta-sigma (ΔΣ) ADCs using only a single supply 2.5- to 5-V power supply. The THS4531 is also a valuable tool for general-purpose, low-power differential signal conditioning applications.

The THS4531 is characterized for operation over the extended industrial temperature range from –40°C to +125°C.

**Features**

- Ultralow power:
  - Voltage: 2.5 V to 5.5 V
  - Current: 250 µA
  - Power-down mode: 0.5 µA (typical)
- Fully-differential architecture
- Bandwidth: 36 MHz
- Slew rate: 200 V/µs
- THD: –120 dBc at 1 kHz (1 $V_{RMS}$, $R_L$= 2 kΩ)
- Input voltage noise: 10 nV/$\sqrt{Hz}$ (f = 1 kHz)

- High DC accuracy:
  - $V_{OS}$ drift: ±4 µV/°C (–40°C to +125°C)
  - $A_{OL}$: 114 dB
- Rail-to-rail output (RRO)
- Negative rail input (NRI)
- Output common-mode control

For more details on the THS4531 device, refer to the product page: http://www.ti.com/product/ths4531.

**THS4521**

The THS4521, THS4522, and THS4524 family of devices are very low-power, fully differential amplifiers with rail-to-rail output and an input common-mode range that includes the negative rail. These amplifiers are designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter. These amplifiers also provide exceptional performance in audio applications.

These fully differential amplifiers feature accurate output common-mode control that allows for DC-coupling when driving ADCs. This control, coupled with an input common-mode range below the negative rail as well as the rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, these devices are ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single 2.5- to 5-V and ground power supply.

The THS4521, THS4522, and THS4524 family of fully differential amplifiers is characterized for operation over the full industrial temperature range from –40°C to +85°C.

**Features**

- Fully differential architecture
- Bandwidth: 145 MHz ($A_V$ = 1 V/V)
- Slew rate: 490 V/µs
- HD2: –133 dBc at 10 kHz (1 $V_{RMS}$, $R_L$ = 1 kΩ)
- HD3: –141 dBc at 10 kHz (1 $V_{RMS}$, $R_L$ = 1 kΩ)
- Input voltage noise: 4.6 nV/$\sqrt{Hz}$ (f = 100 kHz)
- THD+N: –112dBc (0.00025%) at 1 kHz (22-kHz BW, G = 1, 5 VPP)
- Open-loop gain: 119 dB (DC)
- Negative rail input (NRI)
- Rail-to-rail output (RRO)
- Output common-mode control (with low offset)
- Power supply:
  - Voltage: 2.5 V (±1.25 V) to 5.5 V (±2.75 V)
  - Current: 1.14 mA/ch
- Power-down capability: 20 µA (typical)

For more details on the THS4521 device, refer to the product page: http://www.ti.com/product/ths4521.

### 3.1.3 Reference and Buffer

TR and DFR ADCs have different input ranges. The common mode output of the differential amplifier also must be adjusted based on the ADC range. The reference required is 0.95 V and 2.5 V. The LM4140 series of references provides the reference values nearest to the required values. These references have excellent initial accuracy and a low temperature coefficient.

**LM4140 series**

The LM4140 series of precision references are designed to combine high accuracy, low drift, and noise with low power dissipation in a small package. The LM4140 is the industry's first reference with output voltage options lower than the bandgap voltage. The key to the advance performance of the LM4140 is the use of EEPROM registers and CMOS digital-to-analog converters (DACs) for temperature coefficient curvature correction and trimming of the output voltage accuracy of the device during the final production testing. The major advantage of this method is the much higher resolution available with DACs than is economically available with most methods utilized by other bandgap references. The low input and dropout voltage, low supply current, and output drive capability of the LM4140 makes this product an ideal choice for battery powered and portable applications.

The LM4140 is available in three grades (A, B, and C) with 0.1% initial accuracy and 3-, 6-, and 10-ppm/°C temperature coefficients.

**Features**

- High initial accuracy: 0.1%
- Ultralow noise
- Low temperature coefficient: 3 ppm/°C (A grade)
- Low voltage operation: 1.8 V
- Low dropout voltage: 20 mV (typical) at 1 mA
- Supply current: 230 μA (typical), ≤ 1-μA disable mode
- Enable pin
- Output voltage options: 1.024 V, 1.250 V, 2.048 V, 2.500 V, and 4.096 V
- Custom voltages from 0.5 V to 4.5 V

For more details on the LM4140 device, refer to the product page: http://www.ti.com/product/lm4140.

**OPA322 op-amp buffer**

The OPA322 series consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs and outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, the low quiescent current of only 1.5 mA per channel makes these devices well-suited for power-sensitive applications.

The combination of very low noise (8.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz), high gain-bandwidth (20 MHz), and fast slew rate (10 V/μs) make the OPA322 family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPA322 series is also excellent for consumer audio applications, particularly for single-supply systems.

All versions are specified for operation from –40°C to +125°C.

**Features**

- Gain bandwidth: 20 MHz
- Low noise: 8.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz
- Slew rate: 10 V/μs
- Low THD+N: 0.0005%
- Rail-to-rail I/O
- Offset voltage: 2 mV (maximum)
- Supply voltage: 1.8 V to 5.5 V

- Supply current: 1.5 mA/ch
  - Shutdown: 0.1 µA/ch
- Unity-gain stable

For more details on the OPA322 device, refer to the product page: http://www.ti.com/product/opa322.

### 3.1.4 LDO

The TPS7A65xx-Q1 is a family of low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 µA in light-load applications. These devices feature integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the requirement of using a boost converter during cold crank conditions. Because of these features, these devices are well-suited in power supplies for various automotive applications.

**Features**

- Low dropout voltage
  - 300 mV at $I_{OUT}$ = 150 mA
- 4- to 40-V wide input voltage range With up to 45-V transients
- 300-mA maximum output current
- 25-µA (typical) ultralow quiescent current at light loads
- 3.3- and 5-V fixed output voltage with ±2% tolerance
- Low-ESR ceramic output stability capacitor
- Integrated fault protection
  - Short-circuit and overcurrent protection
  - Thermal shutdown
- Low input-voltage tracking

For more details on the LDO device, refer to the product page: http://www.ti.com/product/tps7a6533-q1.

# 4 Transient Recorder and Digital Fault Recorder AFE—Design Theory

## 4.1 High Speed ADC

### 4.1.1 Transient Recorder

The following Figure 6 shows the pin configuration for the ADC3441 ADC.

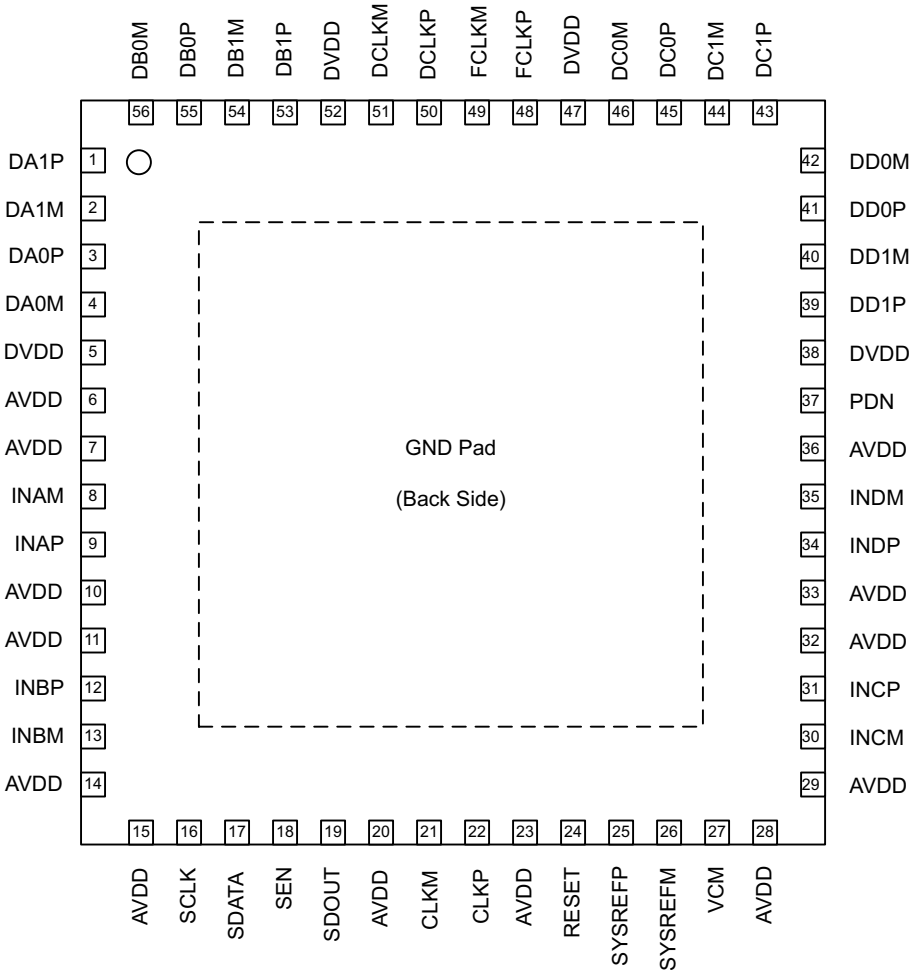



**Figure 6. ADC3441 Pin Configuration**

**Applicable key specifications**

AVDD analog supply voltage range: 1.7 V to 1.9 V

DVDD digital supply voltage range: 1.7 V to 1.9 V

Differential input voltage ($V^{ID}$): 2 VPP

VCM common-mode voltage output ($V_{OC\_VCM}$): 0.95 V

Input clock frequency and sampling clock frequency: 10 Msps to 25 Msps

This TI Design uses the ADC3441 EVM with the following listed changes to perform the input voltage measurement. The ADC3441 device is a four channel ADC with a 14-bit resolution. The output is connected to a processing unit such as a digital signal processor (DSP) or field-programmable gate array (FPGA) using a serial LVDS interface. This ADC can measure up to a 2-VPP differential input. The recommended reference is 0.95 V.

The following steps list the changes for properly interfacing the ADC3441EVM to the AFE for transient input measurement:

1. Ensure that the following connectors are mounted:
   J1, J2, J3, J4, J5, J6, J7, and J8
2. Remove the following resistors from the EVM board:
   R2, R13, R16, R27, R30, R41, R44, and R55
3. Connect the following for data input:
   J1 → R3
   J2 → R14
   J3 → R16
   J4 → R27
   J5 → R30
   J6 → R41
   J7 → R44
   J8 → R55

**NOTE:** The VCM common-mode voltage for analog inputs is available as an output of the ADC and can be used to provide the common-mode reference input to differential amplifiers.

Refer to the ADS3441EVM for details on connection, input range, and output interface:
http://www.ti.com/tool/adc3441evm

### 4.1.2 Digital Fault Recorder

The following Figure 7 shows the pin configuration for the ADS7853 ADC.

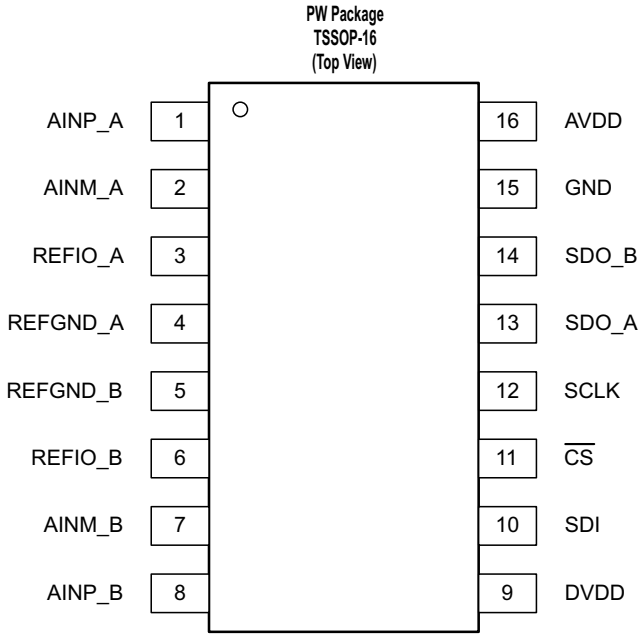



**Figure 7. ADS7853 Pin Configuration**

This TI Design uses the ADSxx54 family of EVMs with the following listed changes to perform the input voltage measurement. The ADS8353, ADS7853, and ADS7253 belong to a family of pin-compatible, dual, high-speed, simultaneous-sampling, ADCs that support single-ended and pseudo differential analog inputs. These devices are two-channel ADCs and two ADCs must be used when four channels are required for DFR applications.

The following steps list the changes for properly interfacing the EVM to the AFE:

1. Disconnect the R21 end that leads to R15 and connect this to the J2 input
2. Disconnect the R22 end that leads to R18 and connect this to the J1 input
3. Remove C22 (this value can be adjusted based on the application)

Refer to the EVM for details on connection, input range, and output interface: http://www.ti.com/tool/ads8354evm-pdk.

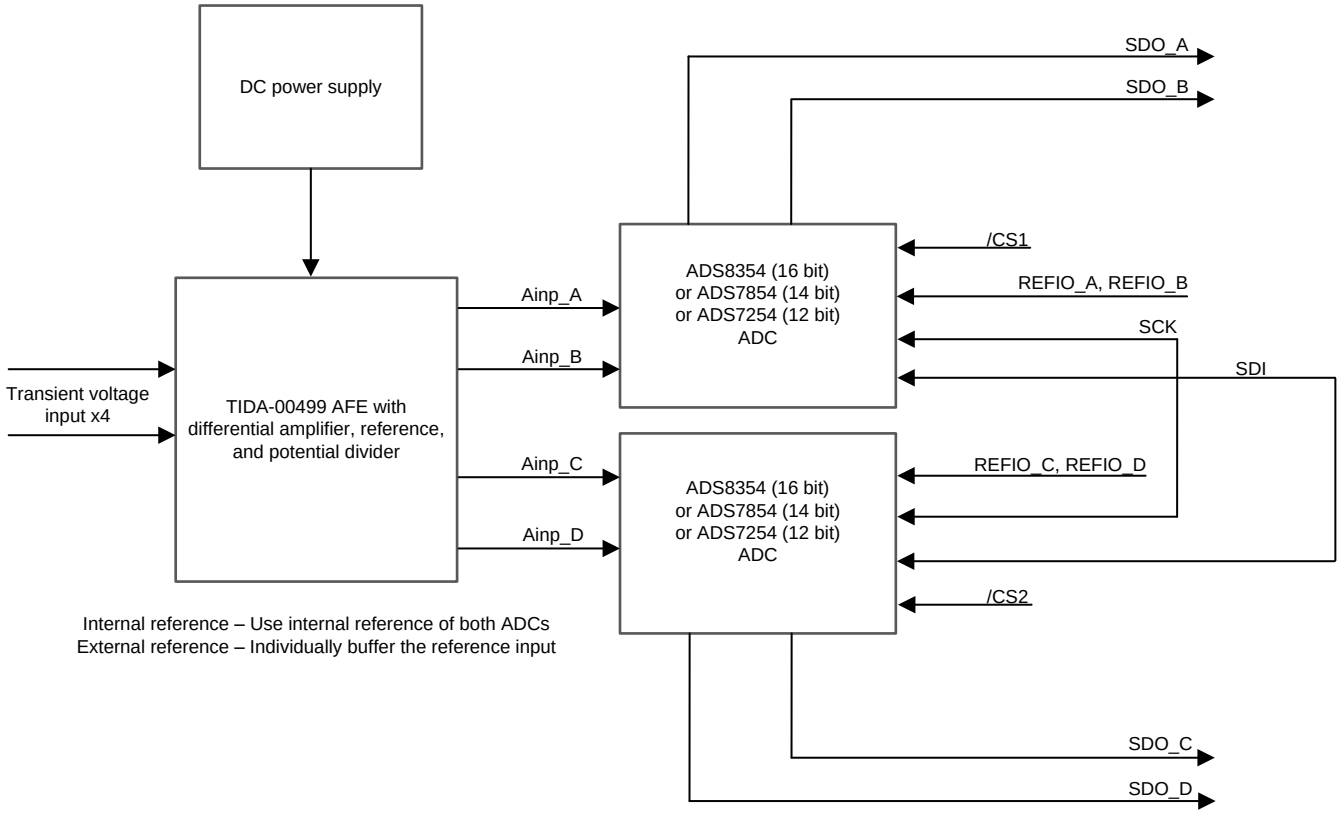



**Figure 8. Connecting Two ADCs to Configure Design for Four-Channel DFR**

**NOTE:** The reference output is available from the ADCs and can be used to provide the AC input level shift required at the differential amplifiers.

Refer to the respective datasheet of the ADSxx54 family of EVMs for details on the connection and interface.

## 4.2 Differential Amplifier

The AFE can be used with the THS4531, THS4521, or THS4551 differential amplifier depending on the application requirements and temperature range.

The output of the potential divider (resistive voltage divider) is applied as the input to the differential amplifier. The input is typically an AC input with a positive or negative transient, which overrides the AC waveform. The AC input must be level shifted by VDD / 2. The values are 2.5 V for the SAR ADC and 0.95 V for the ADC34xx family of ADCs.

The settings for the gain of the differential amplifier are as follows:

### Transient recorder

The potential divider resistance is 1650 kΩ and the differential amplifier feedback resistance is 499 Ω. The ADC input range is 1 V at the peak. The gain is approximately 3300, which enables measurement of a peak transient of approximately 2.5 kV.

### Digital fault recorder

The potential divider resistance is 550 kΩ and the differential amplifier feedback resistance is 499 Ω. The ADC input range is 2.5 V at the peak. The gain is approximately 1100, which enables measurement of a peak transient of approximately 2 kV.

The following Figure 9 shows a schematic of the differential amplifier for the digital fault recorder used in this TIDA-00499 design.

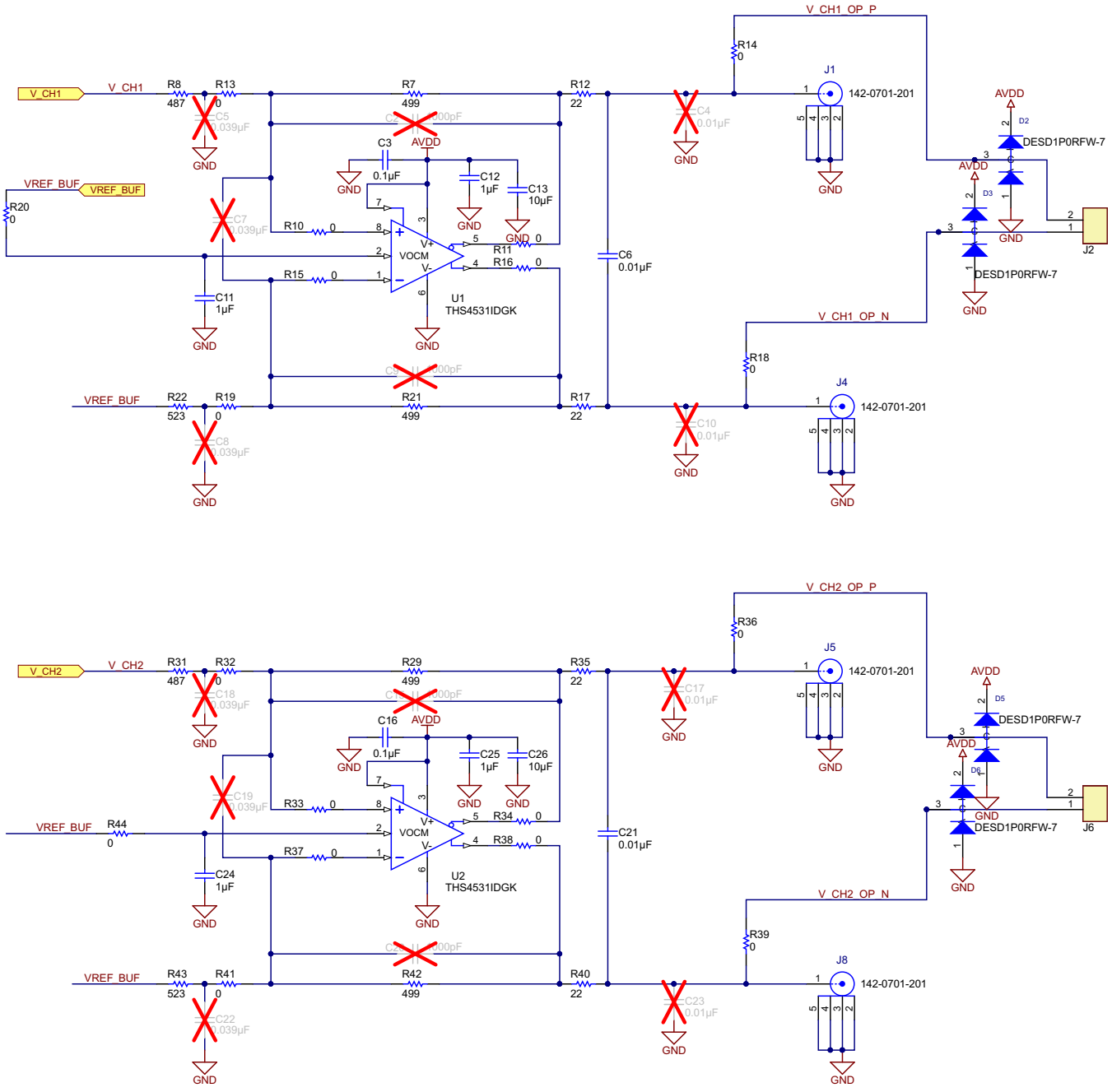



**Figure 9. TIDA-00499 DFR Schematic**

### Setting the output common-mode voltage

The output common-model voltage is set by the voltage at the $V_{OCM}$ pin and the internal circuit works to maintain the output common-mode voltage as close as possible to this voltage. If left unconnected, the output common-mode is set to mid-supply by internal circuitry, which may be overdriven from an external source. Figure 10 shows a representation of the $V_{OCM}$ input. The internal $V_{OCM}$ circuit has about 24 MHz of a –3-dB bandwidth, which is required for the best performance; however, for the purposes of this design, the $V_{OCM}$ circuit is intended to function as a DC bias input pin. TI recommends placing bypass capacitors on this pin to reduce the noise. The following formula in Equation 1 is used to calculate the external current required to overdrive the internal resistor divider:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{60\ k\Omega} \quad (1)$$

where

- $V_{OCM}$ is the voltage applied to the $V_{OCM}$ pin.

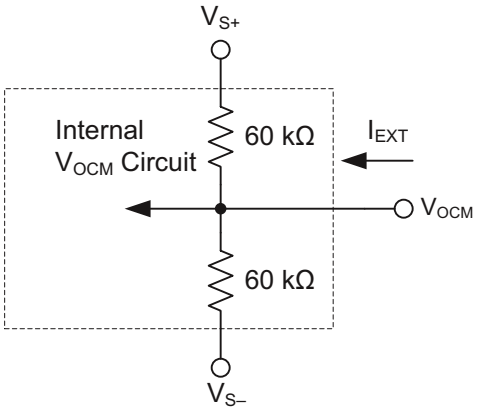



**Figure 10. Circuit for $V_{OCM}$ Configuration**

The resistor connected to the $V_{OCM}$ has the following specifications:

Transient recorder: 15 kΩ

Digital fault recorder: 0 Ω

## 4.3 Reference and Buffer

The TIDA-00499 design uses the following reference voltages:

Transient recorder: The reference for the TR is 1.024 V, which is divided to 0.95 V before buffering. The buffered 0.95 V is applied to the differential amplifiers, which are interfaced to the ADC3441 or ADC3421 ADC.

Digital fault recorder: The reference for the DFR is 2.5 V. The references are buffered before applying to the differential amplifier to provide the required switching current as applicable. The OPA322 op amp is configured as a buffer in this application.

**NOTE:** If the design uses an external reference for SAR ADCs, the reference inputs to all the ADCs must be individually buffered.

The following Figure 11 shows a schematic of the reference with a buffer.

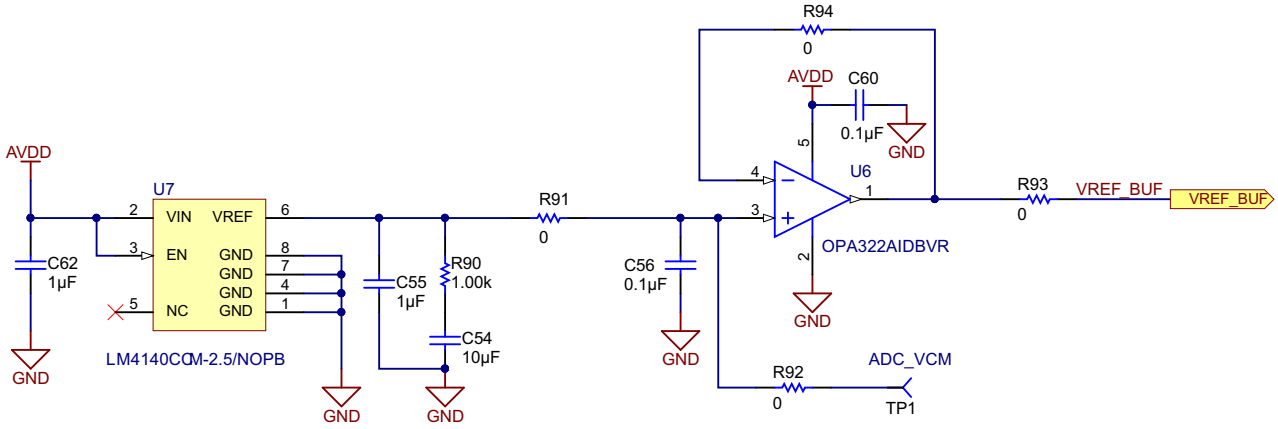



**Figure 11. Reference With Buffer**

## 4.4 Power Supply Regulator—LDO

The LDO provides the required power supply for the AFE operation.

Fixed output regulators are used to power the differential amplifiers, buffer, op amp, and reference. The regulator which has been selected has a higher current rating than required for the differential amplifiers. This selection has been made to provide an option to power the ADCs or any other peripherals required. If an external DC voltage is available, this regulator is optional. The regulator output is protected for overvoltage and electrostatic discharge (ESD) using a Zener diode. The Zener rating must be changed based on the output regulator used.

The following regulators have been used in the AFE design

Transient recorder: 3.3 V (TPS7A6533)

Digital fault recorder: 5 V (TPS7A6550)

The following Figure 12 shows a schematic of the LDO.

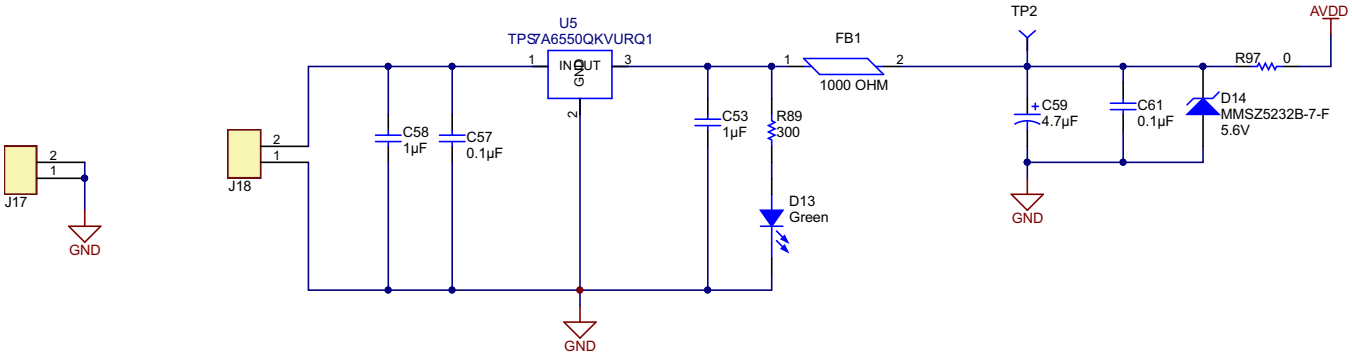



**Figure 12. LDO for Differential Amplifiers**

## 4.5 EVM and Digital Interface for Capturing Samples

### 4.5.1 Transient Recorder

The following Figure 13 shows the ADC3441 EVM.

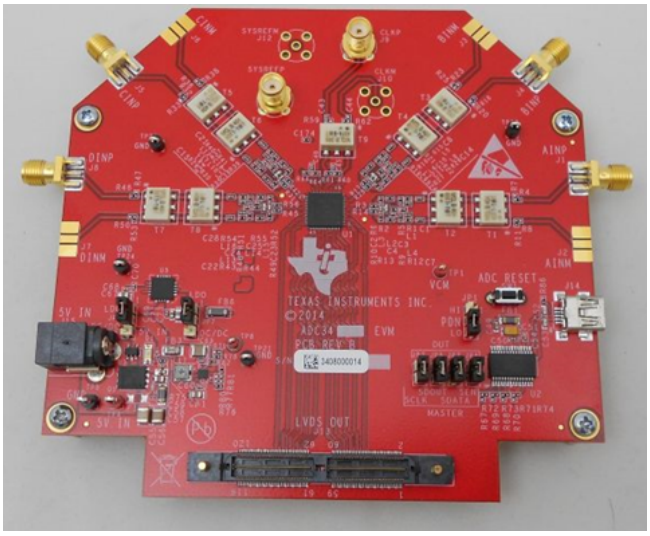


**Figure 13. ADC3441 EVM Board Image**

Clock Input: Apply an Input clock of > 10 MHz 1.8 VPP at J9 and J10.

**NOTE:** The SYSREF input enables complete system synchronization. The current TIDA-00499 design does not use the SYSREF input because this design only uses one ADC. However, some applications exist that require measuring more than four transient input channels. For such applications, the user can utilize multiple ADC34xx devices and synchronize them using the SYSREF input.

The following Table 3 details the EVM connections.

**Table 3. ADC3xxxx EVM Connectors**

| DEVICE | CONNECTOR | FUNCTION |
|---|---|---|
| ADC34xx | J1 | AINP – positive input for A, Ch1 single-ended input |
| | J2 | AINM – negative input for A, DNI |
| | J3 | BINM – negative input for B, DNI |
| | J4 | BINP – positive input for B, Ch2 single-ended input |
| | J5 | CINP – positive input for C, Ch3 single-ended input |
| | J6 | CINM – negative input for C, DNI |
| | J7 | DINM – negative input for D, DNI |
| | J8 | DINP – postive input for D, Ch4 single-ended input |
| | J9 | CLK_INP – postive CLK input, single-ended clock input |
| | J10 | CLK_INM – negative CLK input, DNI |
| | J11 | SYSREF_INP – positive input for SYSREF frame clock, single-ended input |
| | J12 | SYSREF_INM – negative SYSREF input, DNI |
| | J13A, J13B | HSMC data connector to TSW1400 evaluation platform |
| | J14 | Mini USB connector for SPI control |
| | J15 | Power connector for 5-V adapter |

**Interfacing to the TSW1400 EVM—high-speed data capture and pattern generation platform**

The TSW1400EVM is a complete pattern generator and data capture circuit board used to evaluate most of Texas Instruments' (TI) high-speed ADCs. When using this device with an ADC EVM, high-speed data (either CMOS, LVDS, or JESD204B serial) is captured and then stored into a memory bank or directly inside the FPGA, depending on which TSW14xxx platform is being used. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on a serial peripheral interface (SPI). An onboard high-speed USB-to-SPI converter bridges the FPGA SPI to the host PC and GUI.

The following Figure 14 shows a top view of the TSW1400EVM.

Points to note and address when using a TSW1400EVM:

- The user must install the High-Speed Data Converter Pro GUI (HSDC Pro GUI) software for interfacing with the ADC EVM.
- The TWS1400 board does not store the EVM data and reports an error if the ADC clock that has to be externally applied has not done so.
- Select the firmware to be loaded into the data capture board based on the ADC EVM board used (for example, the ADC3441 or ADC3421).

**Figure 14. Top View of TSW1400EVM Circuit Board**

### 4.5.2 Digital Fault Recorder

**ADC EVM**

The ADSxx54 is a dual-channel, simultaneous-sampling ADC that supports fully-differential analog inputs. Each channel of the ADSxx54 uses a THS4521 or THS4531 fully-differential amplifier to drive the differential inputs of the ADC. The ADSxx54EVM is designed for easy interfacing to multiple analog sources. SubMiniature version A (SMA) connectors allow the EVM to connect to input signals through coaxial cables. In addition, header connectors JP1 through JP4 provide a convenient way to connect input signals. All analog inputs are buffered by a high-speed, fully differential amplifier to properly drive the ADSxx54 ADC inputs.

Figure 15 shows a board image of the ADSxx54EVM.

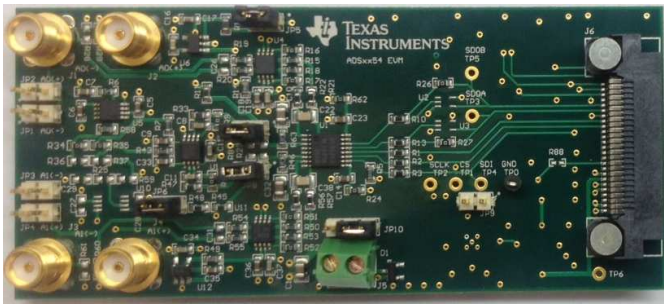


**Figure 15. ADSxx54EVM Board Image**

### Serial data capture card (SDCC) interface

The evaluation kit combines the ADSxx54EVM board with a serial data capture card (SDCC) controller board. The SDCC controller board consists of TI Sitara™ embedded microcontroller (AM3352) and an FPGA (see Figure 16). The SDCC controller board provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the SDCC controller board platform and the SDCC board provides the power and digital signals used to communicate with the ADSxx54EVM board.

**Figure 16. SDCC Card of ADSxx54 Board**

### SDCC with USB cable interfaced to EVM

Figure 17 shows how the ADSxx54EVM is interfaced to the SDCC card.

**Figure 17. ADSxx54-EVM-PDK**

## 4.6 Graphical User Interface (GUI)

### 4.6.1 Transient Recorder

The following GUIs in Figure 18 and Figure 19 must be installed for use with the transient recorder in TIDA-00499.

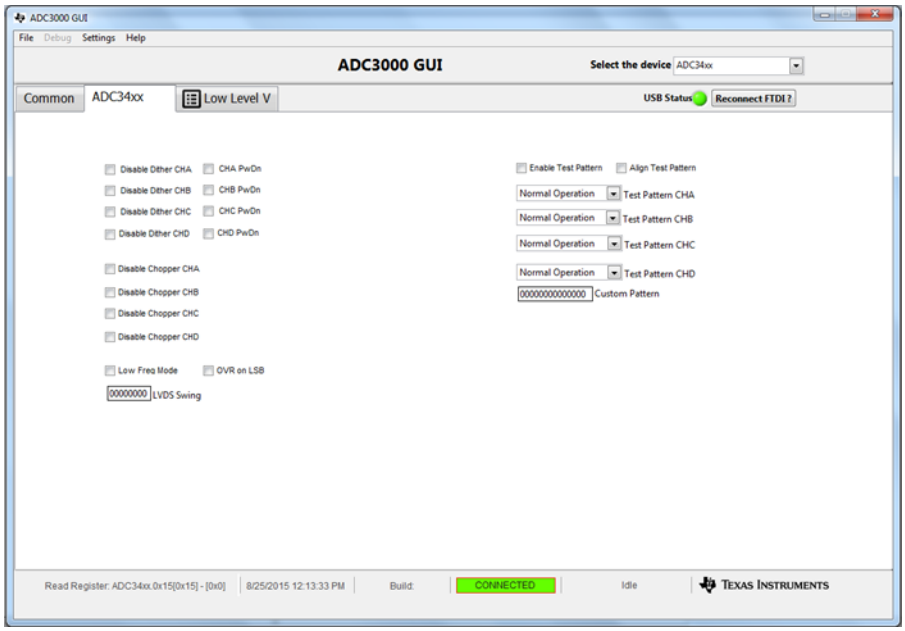



**Figure 18. ADC3441 GUI**

**NOTE:** Perform a reset using this GUI before testing. The channel for analysis is set using this GUI.

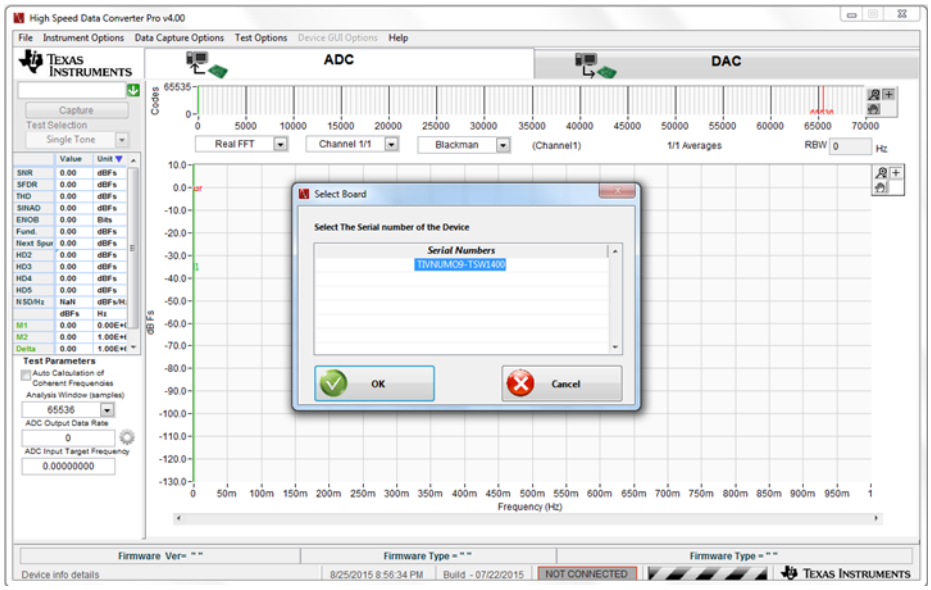



**Figure 19. ADC3441 High-Speed Data Converter Pro GUI**

**NOTE:** Both of the preceding GUIs must be running while testing the ADC performance.

### 4.6.2 Digital Fault Recorder

The following GUI in Figure 20 must be installed for use with the digital fault recorder in TIDA-00499.

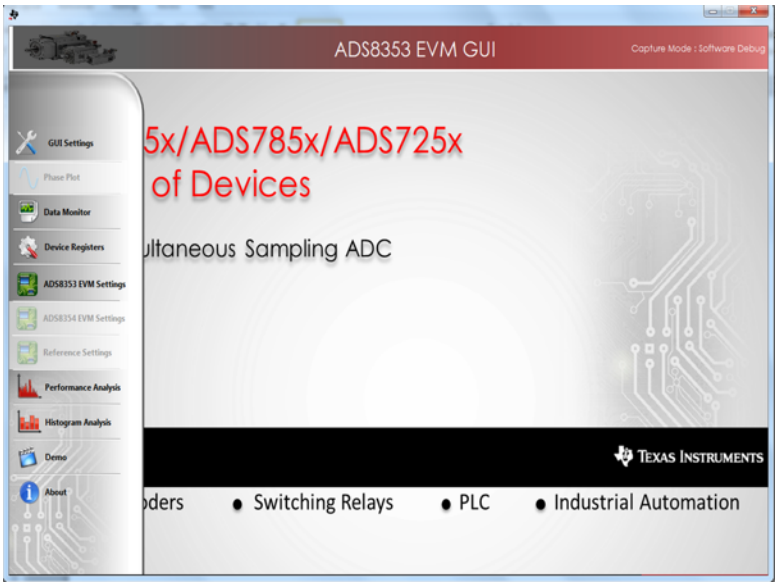



**Figure 20. ADS8353EVM GUI**

**NOTE:** The specific ADC (12-, 14-, or 16-bit) has been selected for measurement.

## 4.7 Potential Divider (Resistive Voltage Divider) for AC Input and Impulsive Input

### 4.7.1 Transient Recorder

The input voltage range for the ADC used in the TIDA-00499 transient recorder application is 2 VPP. The chosen divider ratio used must be selected to ensure a measurement range of 2 kVPP for the transient input. The divider consists of five 330-kΩ resistors in series totaling 1650 kΩ. The feedback resistor is 499 Ω. The attenuation is 1650 kΩ / 499 = ≈3300. The input of the ADC is protected for overvoltage. The following Figure 21 shows the potential divider PESD3V3L1BA for the transient recorder used in TIDA-00499. Select the protection device based on the application.

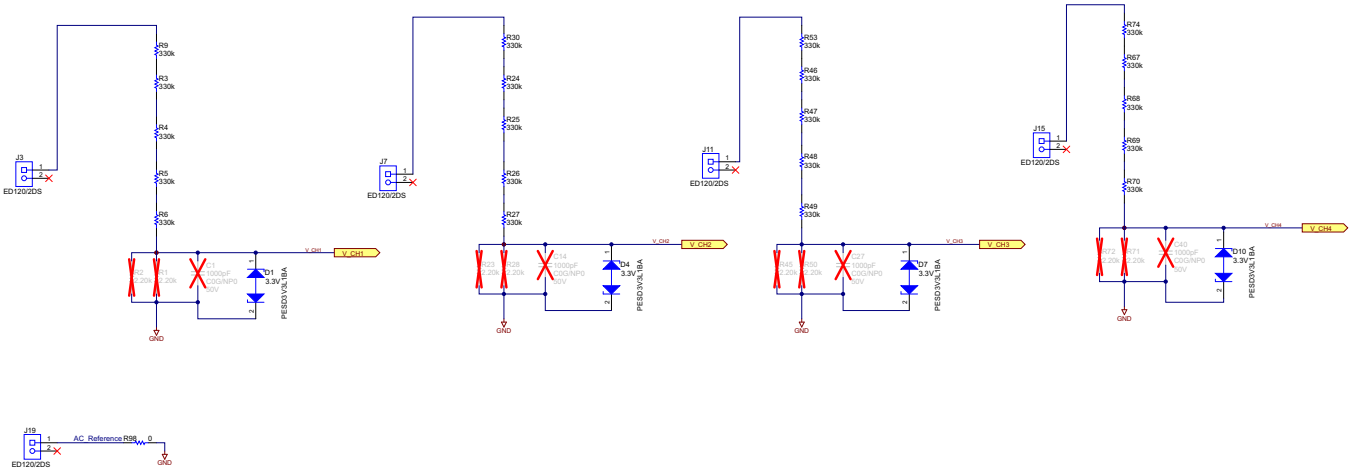


**Figure 21. Potential Divider and PESD3V3L1BA for Transient Recorder**

### 4.7.2 Digital Fault Recorder

The input voltage range for the ADC used in a digital fault recorder application is 5 VPP. The divider ration used must be selected to ensure a measurement range of 2.5 kVPP for the transient input. The divider consists of five 110-kΩ resistors in series totaling 550 kΩ. The feedback resistor is 499 Ω. The attenuation is 550 kΩ / 499 = ≈1100. The input of the ADC is protected for overvoltage. The following Figure 22 shows the potential divider PESD3V3L1BA for the digital fault recorder used in TIDA-00499. Select the protection device and the voltages based on the application requirement.

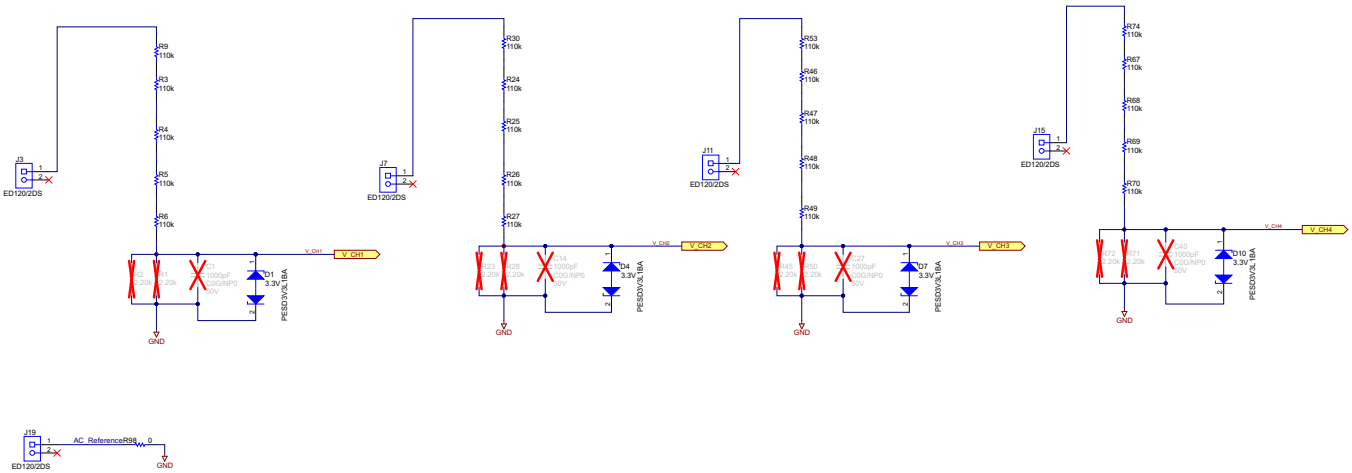



**Figure 22. Potential Divider and PESD3V3L1BA for Digital Fault Recorder**

### 4.7.3 Selection of Potential Dividers

The potential divider (resistor voltage divider) is used to divide the transient input (greater than a 2000-V peak) to levels that the ADC can measure accurately without saturation. The input to the ADC is protected for overvoltage that may be experienced during transient input. This design uses multiple resistors to withstand the transient voltage. The user can optimize the number of resistors used depending on the application and based on the tests performed.

**CAUTION**

**When using high-voltage AC inputs and transient inputs:** Typically the AC rated voltage (230- or 110-V AC) is applied to the input terminal and a transient of 1.2/50 µs and 2-kV peak is applied over the AC input. Do not touch the terminals on which the AC input or transient input has been applied. Touching the inputs with voltage applied may cause shock. The terminals have been configured to avoid the shorting of phase and neutral inputs. Separate terminals are available for four voltage inputs and references (neutral or ground), with one of the pins for all the terminals designated as no connect (NC).

## 4.8 Self-Test for ADC3441

The user can run diagnostics on the ADCs during power up or frequently based on the application. The ADC3441 device provides an option for testing the ADCs internally.

The user can generate an internal test pattern to test all the ADC channels. Refer to the ADC3441 datasheet for more details on test pattern generation and testing. Using the ADC3000 GUI, the user can generate a test pattern and the pattern is displayed in the HSDC Pro GUI software (see Figure 23).

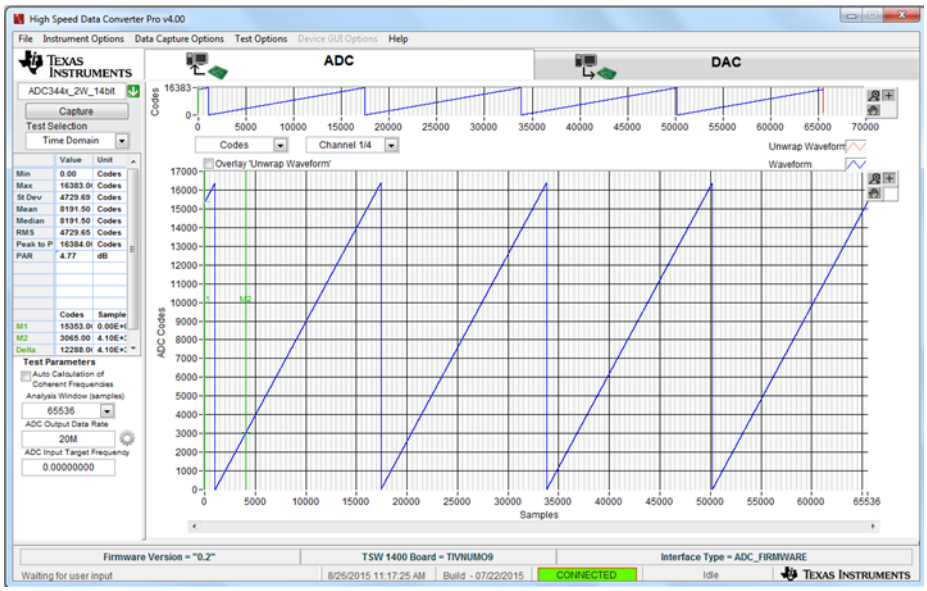



**Figure 23. Self-Test for ADC3441**

## 4.9 Design Guidelines

### 4.9.1 Layout Guidelines for SAR ADC ADSXX53 family

Figure 24 shows a board layout example for the ADS8353, ADS7853, and ADS7253 family of ADCs with the WQFN package. Use a ground plane underneath the device and partition the printed circuit board (PCB) into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As Figure 24 shows, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10-µF, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFIO-A and REFIO-B reference inputs and outputs are bypassed with 10-µF, X7R-grade, 0805-size, 16-V rated ceramic capacitors ($C_{REF-x}$). Place the reference bypass capacitors as close as possible to the reference REFIO-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO-x pins and the bypass capacitors. Small 0.1- to 0.2-Ω resistors ($R_{REF-x}$) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 24 shows $C_{IN-A}$ and $C_{IN-B}$ filter capacitors placed across the analog input pins of the device.

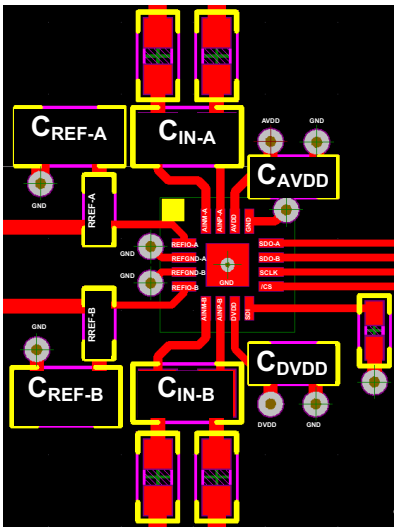



**Figure 24. Recommended Layout for SAR ADC ADSXX53 Family**

### 4.9.2 Layout Guidelines for ADC34XX High-Speed ADC Family

The ADC344x EVM layout can be used as a reference layout to obtain the best performance. Figure 25 shows a layout diagram of the EVM top layer. Some important points to remember when laying out the board are:

1. Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize the onboard crosstalk, the analog inputs must exit the pinout in opposite directions as much as possible, as the reference layout in Figure 25 shows.
2. In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs to minimize coupling between them. This configuration is also maintained as much as possible on the reference layout of Figure 25.
3. Keep the digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver (such as an FPGA or an application-specific integrated circuit (ASIC)) must be matched in length to avoid skew among outputs.
4. At each power supply pin (AVDD and DVDD), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-, 1-, and 0.1-µF capacitors can be kept close to the supply source.

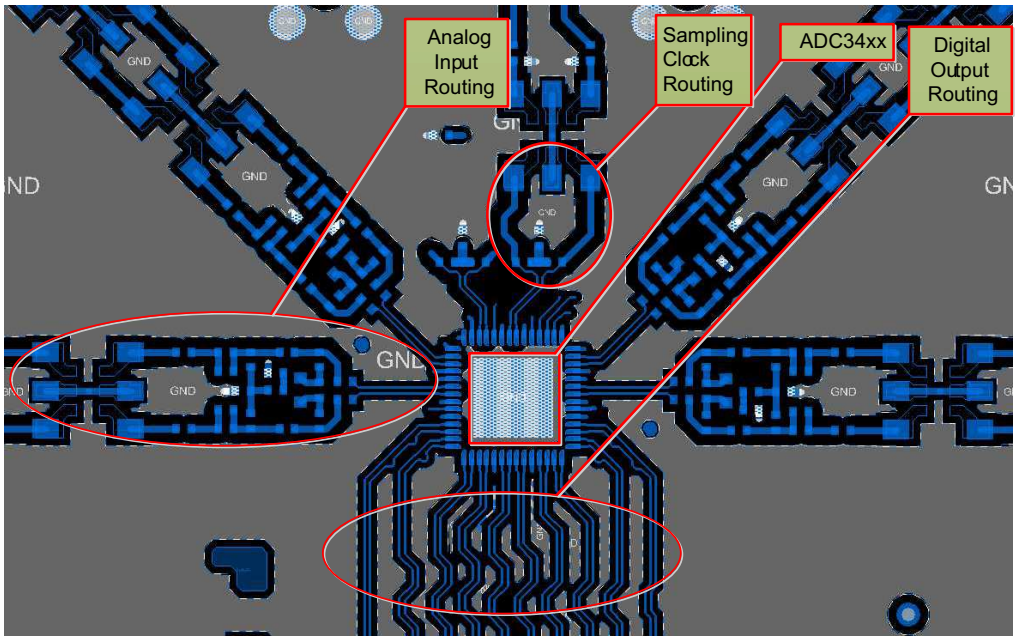



**Figure 25. Typical Layout of ADC344x Board**

### 4.9.3 Layout Recommendations for Differential Amplifier

Use the THS4531EVM as a reference when designing the circuit board (SLOU334). TI recommends to follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. The general guidelines are:

1. The signal routing must be direct and as short as possible into and out of the op amp.
2. The feedback path must be short and direct, avoiding vias if possible.
3. The ground or power planes must be removed from directly under the input and output pins of the amplifier.
4. TI recommends placing a series output resistor as close to the output pin as possible.
5. A 2.2-µF power supply decoupling capacitor must be placed within 2 in of the device and can be shared with other op amps. For a split supply configuration, a capacitor is required for both supplies.
6. A 0.1-µF power supply decoupling capacitor must be placed as close to the power supply pins as possible, preferably within 0.1 in. For a split supply setup, a capacitor is required for both supplies.
7. The PD pin uses transistor-transistor logic (TTL) levels referenced to the negative supply voltage (VS–). When not in use, the TTL must be tied to the positive supply to enable the amplifier. When using the TTL, it must be actively driven high or low and must not be left in an indeterminate logic state. A bypass capacitor is not required, but can be used for robustness in noisy environments.

## 4.10 Enhancements—Partial Discharge Measurement

The AFE previously described can also be used to measure partial discharges (PDs). PDs are small electrical sparks that occur within the insulation or on the surface of the insulation of medium- and high-voltage electrical equipment including power transformers or switchgear. A PD is the result of an electrical breakdown of a small portion of the insulation surface or an air pocket within the insulation. If allowed to continue, PDs will erode the insulation, resulting in tracking or a tree-shaped pattern of deterioration (electrical tree) and eventually result in complete breakdown and failure of the switchgear. Such failures cause unplanned power outages, loss of plant production, equipment damage, or personnel injury. Data obtained through PD testing and monitoring can provide critical information regarding the quality of insulation and its impact on system health. By detecting and trending partial discharge, it is possible to observe its development over time in order to assist asset managers with strategic decisions regarding the repair or replacement of the asset before an unexpected outage occurs.

To detect PD pulses using electromagnetic methods, two techniques are mainly distinguished: those that apply the conventional method based in the standard IEC 60270, in which PD pulses are measured in a frequency range below 1 MHz, and those that implement non-conventional methods based on the use of sensors measuring in the HF (1 to 80 MHz).

The following sensors are used to detect the partial discharge activity:

- Transient Earth Voltage (TEV) sensors (bandwidth = 1 to 50 MHz)
- High-frequency current transformer (HFCT) sensors (bandwidth = 100 kHz to 15 MHz)
- Radio frequency current transducer (RFCT)
- Capacitive coupler
- Acoustic emission (AE) sensor

To measure a PD in the frequency range of 1 to 80 MHz, ADCs with a sampling rate up to 125 MHz are best suited. The following high-speed ADCs highlighted in Table 4 can be used for measurement of partial discharge:

**Table 4. TI Pipeline ADCs for Partial Discharge Measurement**

| PARAMETER | ADC3424 | ADC3444 |
|---|---|---|
| Resolution (Bits) | 12 | 14 |
| Sample rate (Max) (MSPS) | 125 | 125 |
| Number of input channels | 4 | 4 |
| Power consumption (Typ) (mW) | 391 | 391 |
| Architecture | Pipeline | Pipeline |
| Interface | Serial LVDS | Serial LVDS |

In some of the approaches to measure partial discharge, < 50-MSPS sampling is adequate. ADCs ADC3442 or ADC3422 can be considered for these applications.

# 5 Getting Started Hardware

The connector interface is identical for both the transient recorder and digital fault recorder. Table 5 shows the connectors for these AFE boards.

**Table 5. Connector for AFE Board—TR and DFR**

| VOLTAGE INPUTS | CONNECTOR TYPES | LOCATIONS |
|---|---|---|
| Voltage input 1 | Input | J3 |
| | Output | J1, J4, or J2 |
| Voltage input 2 | Input | J7 |
| | Output | J5, J8, or J6 |
| Voltage input 3 | Input | J11 |
| | Output | J9, J12, or J10 |
| Voltage input 4 | Input | J15 |
| | Output | J13, J16, or J14 |
| DC power | Input power supply | J18 |
| Reference for AC voltage input (neutral) | Input | J19 |

# 6 Test Setup

## 6.1 Test Setup for Transient Recorder AFE Performance Testing

Figure 26 shows a block diagram of the setup for testing the transient recorder AFE performance.

The power supply to the EVM and the TSW1400 data capture board is provided by a 5-V brick. The TSW1400 board captures the ADC samples and sends the sample to the HSDC Pro GUI to plot the waveform. Use the function generator to simulate the 1.2/50-µs waveform input. The AC voltage source is used to provide the 50/60-Hz input. An external clock of 20 MHz has been applied to the ADC. A single-ended clock can be applied from an external function generator, which the ADC EVM converts into the differential.

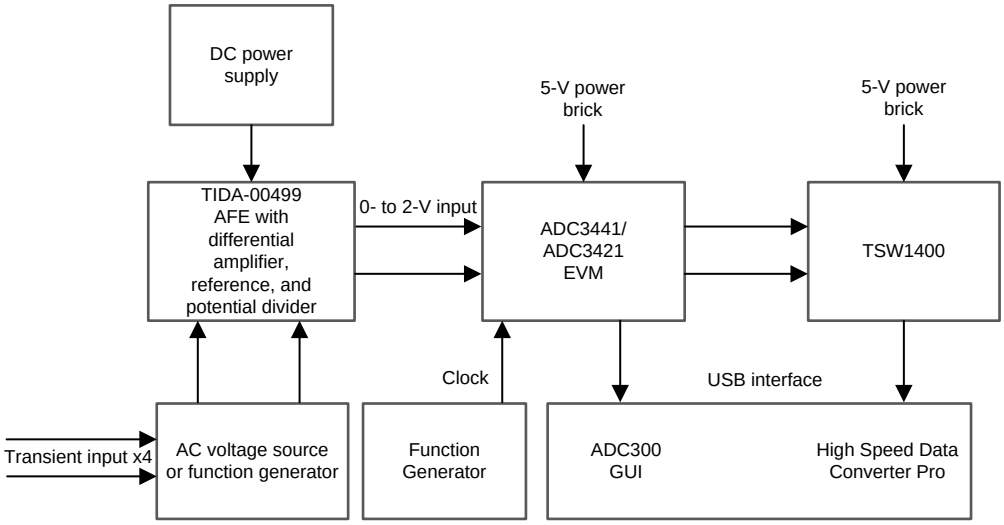



**Figure 26. Test Setup Block Diagram for Transient Recorder AFE Performance**

Figure 27 shows a picture of the physical setup for testing the transient recorder AFE performance.

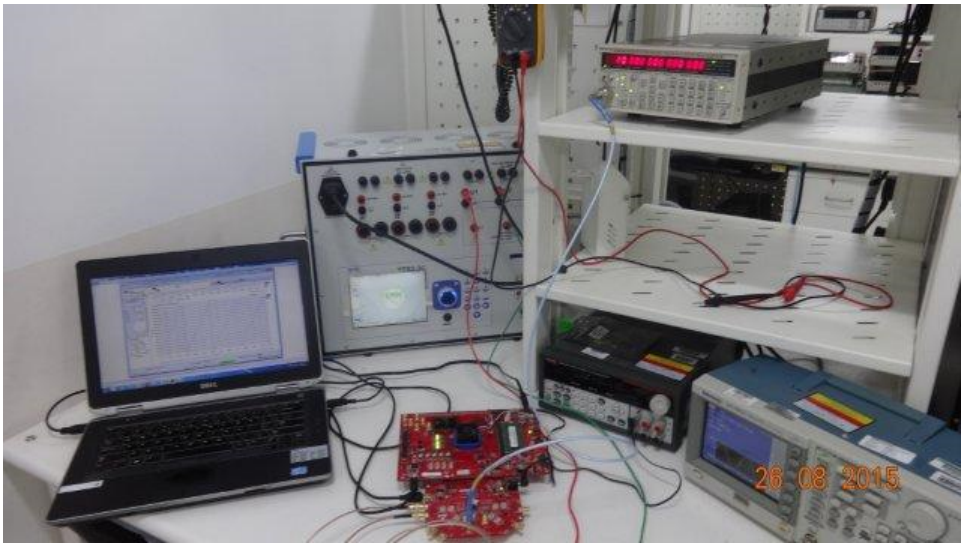



**Figure 27. Test Setup for Transient Recorder AFE Performance**

### 6.1.1 Graphical User Interface

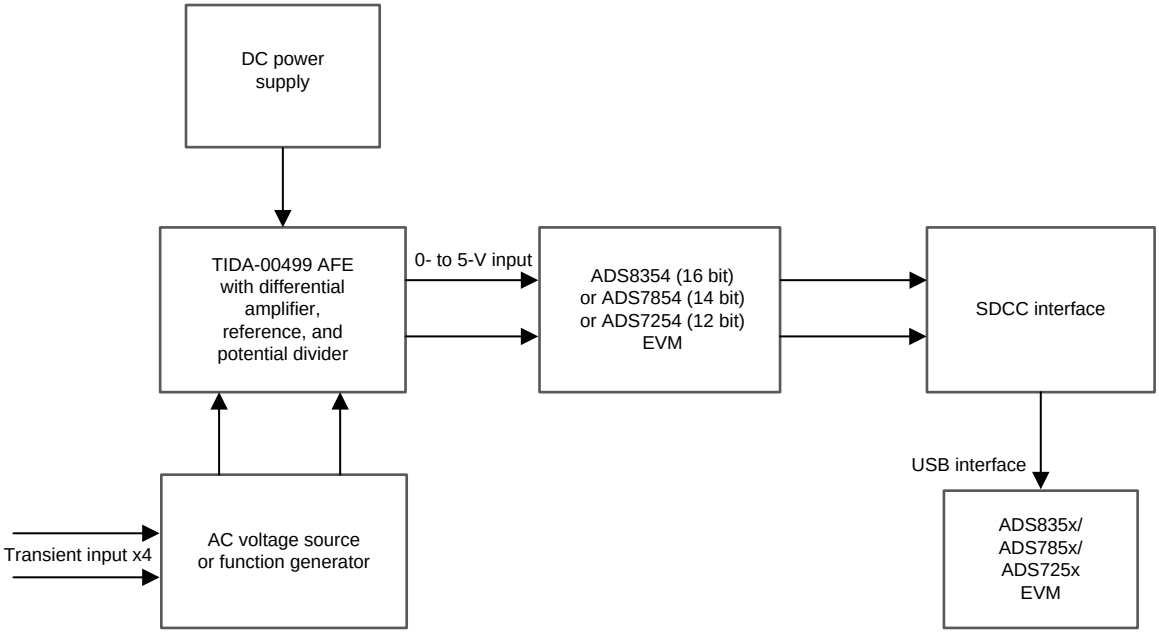
Testing the transient recorder requires installing the following GUIs: ADC3xxx GUI Installer Revision C (http://www.ti.com/tool/adc3441evm) and High-Speed Data Converter Pro software (http://www.ti.com/tool/tsw1400evm).

## 6.2 Test Setup for Digital Fault Recorder AFE Performance Testing

Figure 28 shows a block diagram of the setup for testing the digital fault recorder AFE performance.

An external power supply is used to power the DFR AFE. The SDCC interface provides the power for the ADC EVM. The SDCC board captures the ADC samples and sends the sample to the GUI to plot the waveform. Use the function generator to simulate the 17/20-µs waveform input.

The same board can be used to capture voltage fast transients (spikes) at a 5-µs resolution and 200-kHz sampling rate. An AC voltage source is used to provide the 50/60-Hz input.




Note: EVM with 12-bit, 14-bit, or 16-bit ADC must be ordered for testing

**Figure 28. Test Setup Block Diagram for Digital Fault Recorder AFE Performance**

Figure 29 shows a picture of the physical setup for testing the digital fault recorder AFE performance.

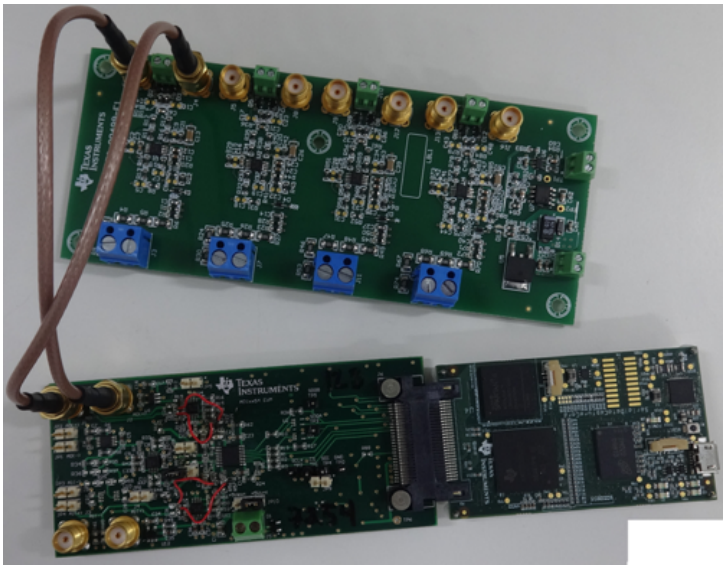


**Figure 29. Test Setup for Digital Fault Recorder AFE Performance**

### 6.2.1 Graphical User Interface

Testing the digital fault recorder requires installing the ADSxx53EVM-PDK and ADSxx54EVM-PDK software Revision A (http://www.ti.com/tool/ads8354evm-pdk).

# 7 Test Data

## 7.1 Functional Testing

This subsection details some of the basic tests for measuring the power supply, reference voltage output, and differential voltage output. The user must perform these tests before engaging the performance tests.

### 7.1.1 Transient Recorder

**Table 6. Power Supply Measurements for AFE configured for TR**

| PARAMETERS | ACTUAL | MEASURED |
|---|---|---|
| ADC supply voltage | 1.8 V | 1.835 |
| ADC clock (10 to 25 MHz) | 20 MHz, 1.8 VPP | 20 MHz, 1.8 VPP |
| ADC power consumption | 180 mW | 200 mW |
| Diff amplifier supply | 3.3 V | 3.336 V |
| Reference output after buffer | 0.95-V DC | 0.951-V DC |
| Diff amp common-mode output | 0.95 V | 0.95 V and 0.97 V |

### 7.1.2 Digital Fault Recorder

**Table 7. Power Supply Measurements for AFE Configured for DFR**

| PARAMETERS | ACTUAL | MEASURED |
|---|---|---|
| ADC analog supply voltage AVDD | 5 V | 5.01 V |
| ADC digital supply voltage AVDD | 3.3 V | 3.3 V |
| Diff amplifier supply | 5-V DC | 5.013-V DC |
| Reference output after buffer | 2.5-V DC | 2.5-V DC |
| Diff amp common-mode output | 2.5 V | 2.5 V and 2.5 V |

## 7.2 Differential Amplifier Output

This section shows the results of the differential amplifier performance tests. The differential measurement contributes for the overall system performance accuracy. The accuracy test has been performed using a multimeter. The input to the differential amplifier and the output of the differential amplifier has been measured and the following graphs show the results. Additionally, the bandwidth performance of the differential amplifier for the frequency input of interest has been performed.

### 7.2.1 Differential Amplifier Output Linearity Testing

**Table 8. Input (mV) versus Diff Amp output—Error at 50 Hz**

| THS4531 INPUT (mV) | THS4531 OUTPUT (mV) | 50-Hz % ERROR |
|---|---|---|
| 93.120 | 93.148 | 0.030 |
| 350.100 | 350.087 | –0.004 |
| 700.200 | 700.273 | 0.010 |
| 1400.000 | 1400.546 | 0.039 |
| 1733.000 | 1733.536 | 0.031 |

The gain is 0.995.

**Table 9. Input (mV) versus Diff Amp Output—Error at 10 kHz**

| THS4531 INPUT (mV) | THS4531 OUTPUT (mV) | 10-kHz % ERROR |
|---|---|---|
| 93.100 | 93.088 | –0.013 |
| 349.900 | 349.888 | –0.003 |
| 699.800 | 699.677 | –0.018 |
| 1399.700 | 1399.552 | –0.011 |
| 1701.000 | 1700.734 | –0.016 |

The gain is 0.999.

**Table 10. Input (mV) versus Diff Amp Output—Error at 60 kHz**

| THS4531 INPUT (mV) | THS4531 OUTPUT (mV) | 60-kHz % ERROR |
|---|---|---|
| 92.990 | 92.937 | –0.057 |
| 350.100 | 349.900 | –0.057 |
| 700.400 | 700.099 | –0.043 |
| 1400.000 | 1399.299 | –0.050 |
| 1702.000 | 1701.297 | –0.041 |

The gain is 0.999.

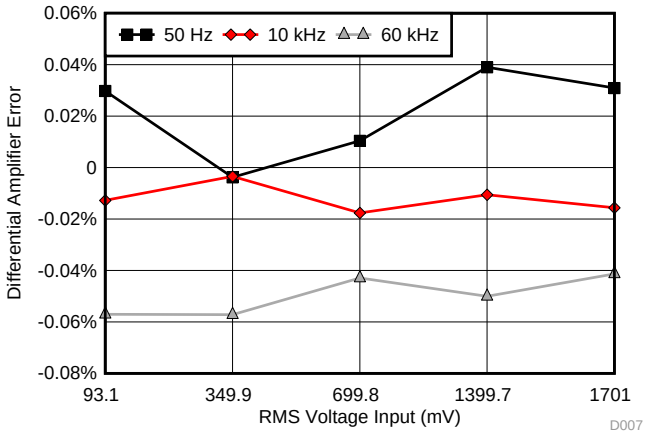



**Figure 30. Input (mV) vs Differential Amp Output Error**

### 7.2.2 Differential Amplifier Bandwidth

**Table 11. Differential Amplifier Output versus Frequency**

| FREQ (Hz) | INPUT (V) | THS4521 OUTPUT (V) | THS4531 OUTPUT |
|---|---|---|---|
| 50 | 1.247 | 1.248 | 1.248 |
| 60 | 1.247 | 1.248 | 1.248 |
| 400 | 1.246 | 1.246 | 1.247 |
| 50000 | 1.246 | 1.247 | 1.247 |
| 100000 | 1.245 | 1.244 | 1.244 |
| 1000000 | 1.252 | 1.252 | 1.252 |

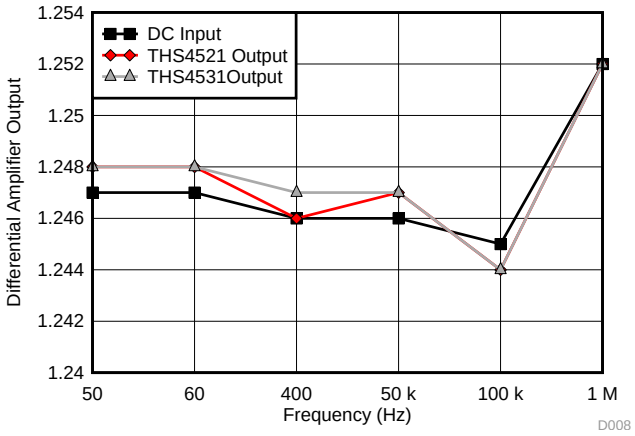



**Figure 31. Frequency vs Differential Amp Output**

## 7.3 Performance Testing—Transient Recorder

The ADC performance test has been performed with a 14-bit ADS3441 EVM. The waveforms have been plotted on a GUI. The input has been sampled at a 20-Msps sampling rate. To simulate an input up to 2 MHz, a function generator has been used. The 50-Hz inputs have been provided using a programmable voltage source. The samples have been captured by the FPGA card and plotted using the GUI. The following subsections provide the waveform plot and the accuracy measurement results under different conditions. The samples captured in the following tests are RMS samples.

### 7.3.1 Waveform Plots of ADC Samples

The following figures show the waveforms of various ADC samples with the AC input applied using a programmable voltage source.

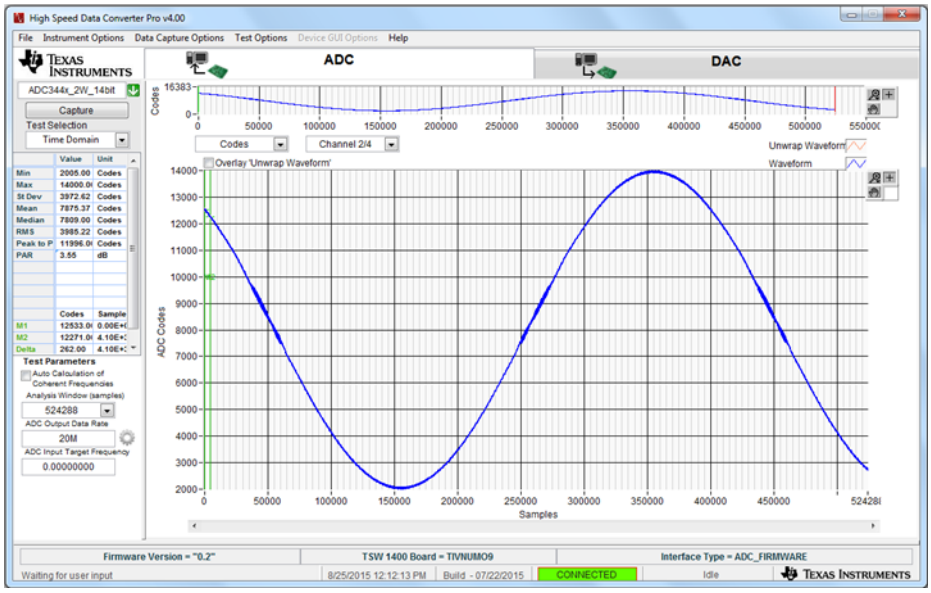



**Figure 32. ADC3441—AC Input With Resistor Divider at 50 Hz**

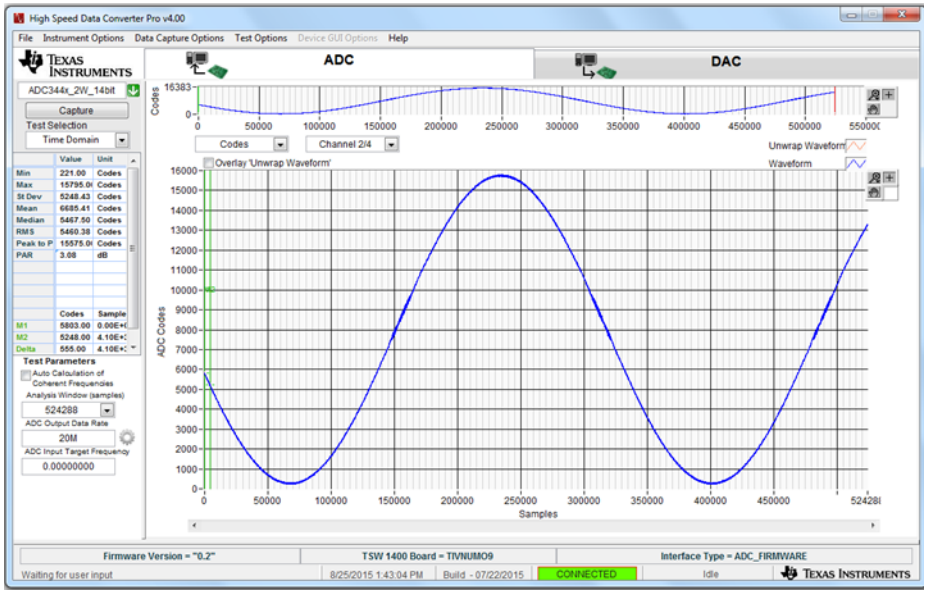



**Figure 33. ADC3441—AC Input With Resistor Divider at 60 Hz**

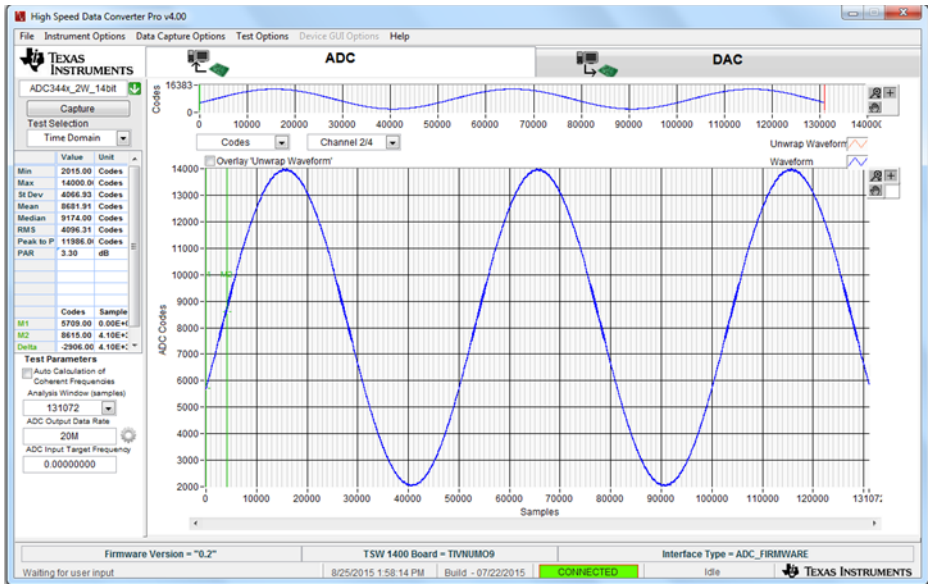



**Figure 34. ADC3441—AC Input With Resistor Divider at 400 Hz**

The following figures show the waveforms of various ADC samples with the input applied using a function generator.

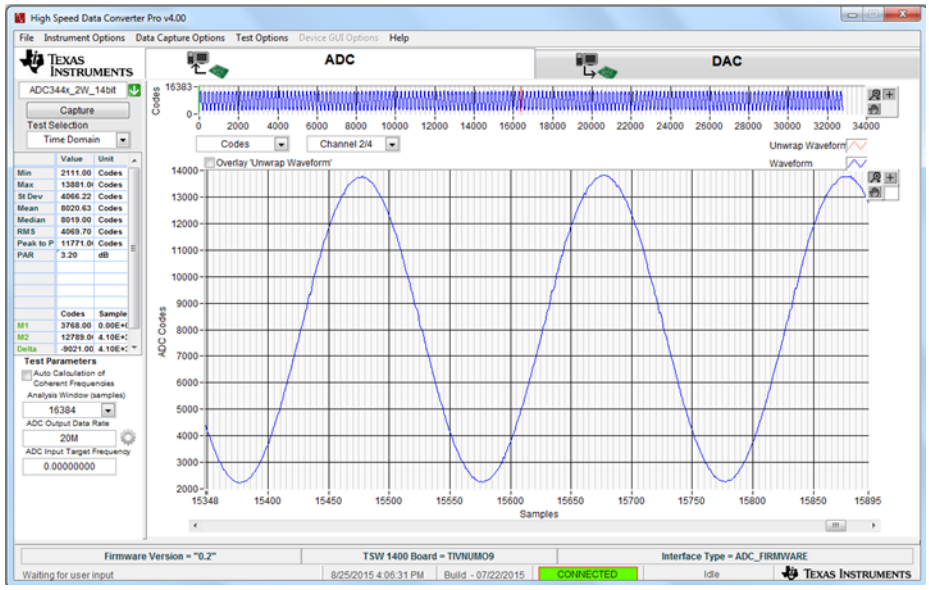



**Figure 35. ADC3441—Function Generator Input at 100 kHz**

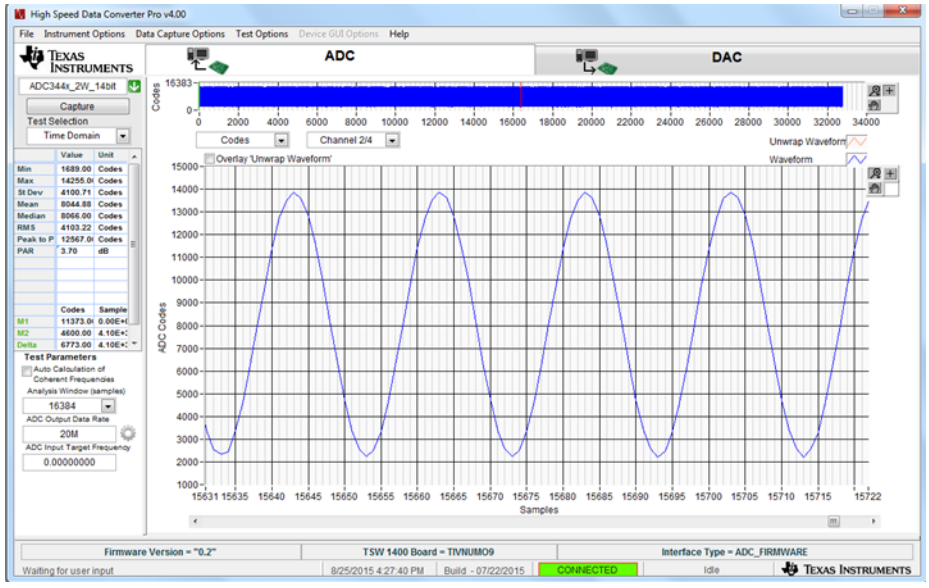



**Figure 36. ADC3441—Function Generator Input at 1 MHz**

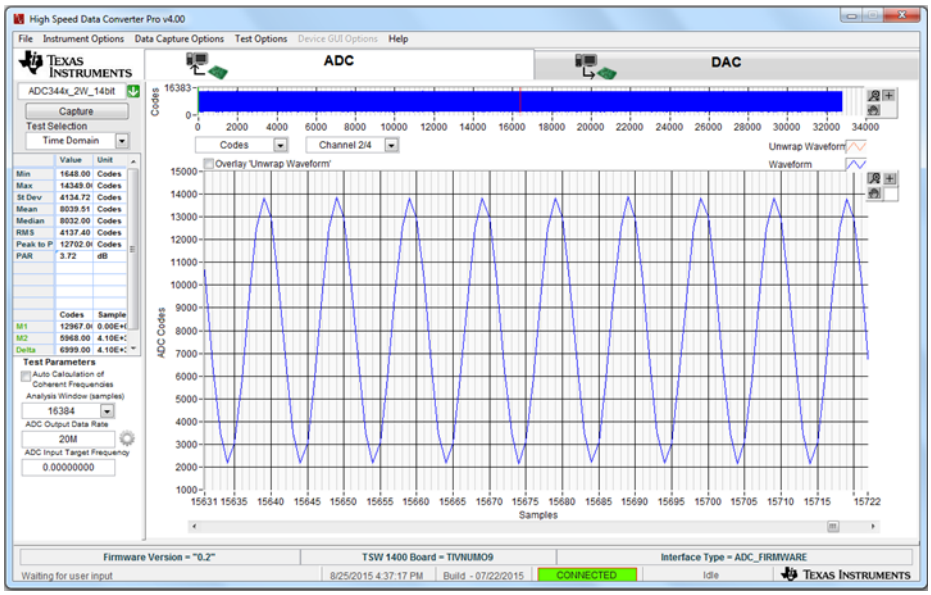



**Figure 37. ADC3441—Function Generator Input at 2 MHz**

### 7.3.2 High-Frequency Input Signal Capture

The input has been applied using a function generator. A function generator has been used to simulate the complete range of ADC input (equivalent to maximum transient).

**Table 12. ADC3 Input—Measurement With THS4521 Differential Amplifier**

| FREQ (MHz) | RMS (mV) | EXPECTED SAMPLES | MEASURED SAMPLES | 100-kHz % ERROR |
|---|---|---|---|---|
| 0.1 | 707.21 | 5793.493635 | 5801.055 | 0.130515 |
| 0.1 | 530.41 | 4345.128554 | 4351.59 | 0.148706 |
| 0.1 | 353.61 | 2896.75237 | 2903.19 | 0.222236 |
| 0.1 | 176.80 | 1448.376185 | 1440.945 | –0.51307 |
| 0.1 | 106.08 | 869.0257109 | 864.8035 | –0.48586 |
| 0.1 | 88.40 | 724.1880924 | 722.07 | –0.29248 |
| **FREQ (MHz)** | **RMS (mV)** | **EXPECTED SAMPLES** | **MEASURED SAMPLES** | **1-MHz % ERROR** |
| 1 | 707.21 | 5793.493635 | 5795.02 | 0.026346 |
| 1 | 530.41 | 4345.128554 | 4348.12 | 0.068846 |
| 1 | 353.61 | 2896.75237 | 2900.16 | 0.117636 |
| 1 | 176.80 | 1448.376185 | 1445.84 | –0.17511 |
| 1 | 106.08 | 869.0257109 | 867.08 | –0.2239 |
| 1 | 88.40 | 724.1880924 | 722.92 | –0.17511 |
| **FREQ (MHz)** | **RMS (mV)** | **EXPECTED SAMPLES** | **MEASURED SAMPLES** | **2-MHz % ERROR** |
| 2 | 707.21 | 5793.493635 | 5796 | 0.043262 |
| 2 | 530.41 | 4345.128554 | 4343.85 | –0.02943 |
| 2 | 353.61 | 2896.75237 | 2894.85 | –0.06567 |
| 2 | 176.80 | 1448.376185 | 1452.15 | 0.260555 |
| 2 | 106.08 | 869.0257109 | 869.4 | 0.04307 |
| 2 | 88.40 | 724.1880924 | 724.5 | 0.04307 |

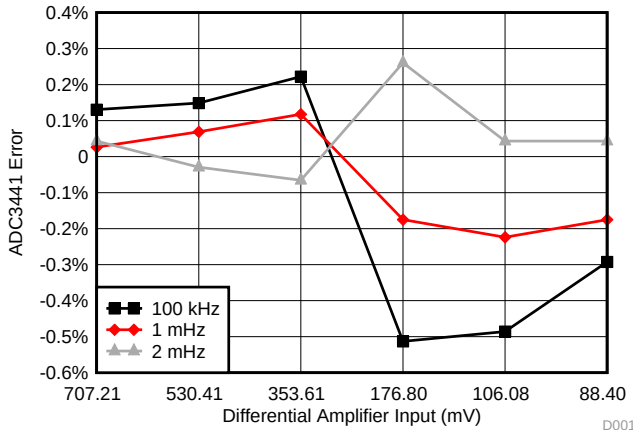



**Figure 38. HF Input (mV) vs ADC Error**

### 7.3.3 Test With AC Input (50 Hz to 400 Hz)

The following Table 13 shows the measurement with a 150-kΩ input impedance. A 150-kΩ impedance has been used to simulate a transient input of 2.5 kV to test the ADC range, which is for testing only.

**Table 13. ADC1 Input Measurement With ≈ 150 kΩ—THS4531**

| AC VOLTAGE (V) | FREQ (Hz) | EXPECTED SAMPLES | RMS INPUT (V) | MEASURED SAMPLES | 50-Hz % ERROR |
|---|---|---|---|---|---|
| 195 | 50 | 5498.02 | 0.67 | 5529.50 | 0.57 |
| 175 | | 4965.43 | 0.61 | 4982.50 | 0.34 |
| 150 | | 4285.35 | 0.52 | 4319.00 | 0.79 |
| 100 | | 2859.63 | 0.35 | 2875.00 | 0.54 |
| 50 | | 1433.91 | 0.18 | 1423.00 | –0.76 |
| 20 | | 567.01 | 0.07 | 562.50 | –0.80 |
| **AC VOLTAGE (V)** | **FREQ (Hz)** | **EXPECTED SAMPLES** | **RMS INPUT (V)** | **MEASURED SAMPLES** | **60-Hz % ERROR** |
| 195 | 60 | 5498.024 | 0.671 | 5486.5 | –0.2096 |
| 175 | | 4965.43 | 0.61 | 4944.50 | –0.42 |
| 150 | | 4285.35 | 0.52 | 4278.00 | –0.17 |
| 100 | | 2859.63 | 0.35 | 2842.50 | –0.60 |
| 50 | | 1433.91 | 0.18 | 1434.00 | 0.01 |
| 20 | | 567.01 | 0.07 | 572.00 | 0.88 |
| **AC VOLTAGE (V)** | **FREQ (Hz)** | **EXPECTED SAMPLES** | **RMS INPUT (V)** | **MEASURED SAMPLES** | **400-Hz % ERROR** |
| 195 | 400 | 5498.02 | 0.67 | 5524.50 | 0.48 |
| 175 | | 4965.43 | 0.61 | 4940.00 | –0.51 |
| 150 | | 4285.35 | 0.52 | 4274.50 | –0.25 |
| 100 | | 2859.63 | 0.35 | 2857.50 | –0.07 |
| 50 | | 1433.91 | 0.18 | 1424.50 | –0.66 |
| 20 | | 567.01 | 0.07 | 564.50 | –0.44 |

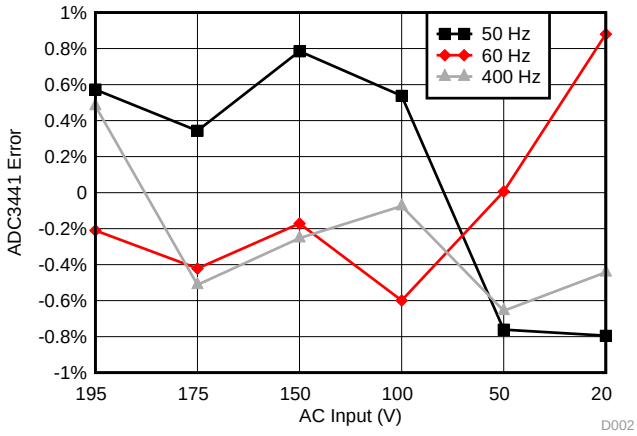



**Figure 39. THS4531—AC Input vs ADC Error**

The following Table 14 shows the measurement with a 150-kΩ input impedance.

**Table 14. ADC2 Input Measurement With 150 kΩ—THS4521**

| AC VOLTAGE (V) | FREQ (Hz) | EXPECTED SAMPLES | RMS INPUT (V) | MEASURED SAMPLES | 50-Hz % ERROR |
|---|---|---|---|---|---|
| 195 | 50 | 5498.02 | 0.67 | 5452.00 | –0.84 |
| 190 | | 5407.89 | 0.66 | 5371.00 | –0.68 |
| 175 | | 4965.43 | 0.61 | 5005.50 | 0.81 |
| 150 | | 4285.35 | 0.52 | 4237.50 | –1.12 |
| 125 | | 3572.49 | 0.44 | 3533.00 | –1.11 |
| 100 | | 2859.63 | 0.35 | 2829.00 | –1.07 |
| 75 | | 2146.77 | 0.26 | 2135.50 | –0.52 |
| 50 | | 1433.91 | 0.18 | 1442.00 | 0.56 |
| 25 | | 716.96 | 0.09 | 713.00 | –0.55 |
| 20 | | 567.01 | 0.07 | 570.00 | 0.53 |
| **AC VOLTAGE (V)** | **FREQ (Hz)** | **EXPECTED SAMPLES** | **RMS INPUT (V)** | **MEASURED SAMPLES** | **60-Hz % ERROR** |
| 195 | 60 | 5498.02 | 0.67 | 5517.00 | 0.35 |
| 190 | | 5407.89 | 0.66 | 5443.50 | 0.66 |
| 175 | | 4965.43 | 0.61 | 5012.50 | 0.95 |
| 150 | | 4285.35 | 0.52 | 4257.00 | –0.66 |
| 125 | | 3572.49 | 0.44 | 3571.50 | –0.03 |
| 100 | | 2859.63 | 0.35 | 2866.50 | 0.24 |
| 75 | | 2146.77 | 0.26 | 2130.00 | –0.78 |
| 50 | | 1433.91 | 0.18 | 1445.00 | 0.77 |
| 25 | | 716.96 | 0.09 | 712.50 | –0.62 |
| 20 | | 567.01 | 0.07 | 572.50 | 0.97 |
| **AC VOLTAGE (V)** | **FREQ (Hz)** | **EXPECTED SAMPLES** | **RMS INPUT (V)** | **MEASURED SAMPLES** | **400-Hz % ERROR** |
| 195 | 400 | 5498.02 | 0.67 | 5512.50 | 0.26 |
| 190 | | 5407.89 | 0.66 | 5428.50 | 0.38 |
| 175 | | 4965.43 | 0.61 | 4939.50 | –0.52 |
| 150 | | 4285.35 | 0.52 | 4280.00 | –0.12 |
| 125 | | 3572.49 | 0.44 | 3579.00 | 0.18 |
| 100 | | 2859.63 | 0.35 | 2833.50 | –0.91 |
| 75 | | 2146.77 | 0.26 | 2150.00 | 0.15 |
| 50 | | 1433.91 | 0.18 | 1422.50 | –0.80 |
| 25 | | 716.96 | 0.09 | 719.00 | 0.29 |
| 20 | | 567.01 | 0.07 | 570.00 | 0.53 |

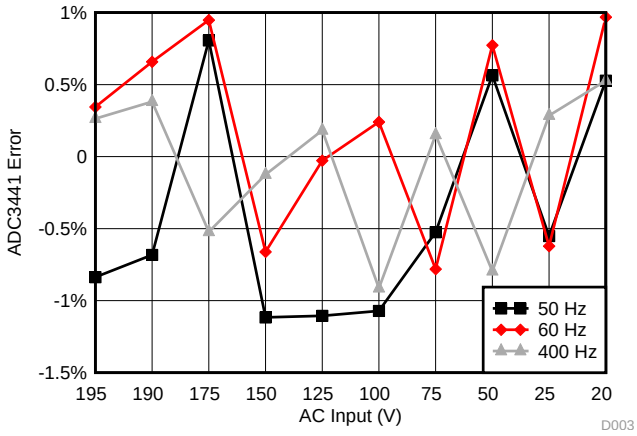



**Figure 40. THS4521—AC Input vs ADC Error**

The following Table 15 and Table 16 show the measurements with a 3.15-MΩ input impedance. The resistors have been chosen for the potential divider to have a total input of 3.15 MΩ

**Table 15. ADC1 Input Measurement With THS4531**

| AC INPUT (V) | FREQ (Hz) | EXPECTED SAMPLES | RMS INPUT (V) | MEASURED SAMPLES | % ERROR |
|---|---|---|---|---|---|
| 433 | 50 | 1433.911 | 0.175 | 1445.5 | 0.808217 |
| 346.4 | | 1155.322 | 0.141 | 1159.5 | 0.361588 |
| 173.2 | | 581.7581 | 0.071 | 569 | –2.19303 |
| 138.56 | | 458.8515 | 0.056 | 457.5 | –0.29454 |
| 433 | 60 | 1433.911 | 0.175 | 1431 | –0.203 |
| 346.4 | | 1155.322 | 0.141 | 1167 | 1.010758 |
| 173.2 | | 581.7581 | 0.071 | 582.5 | 0.127522 |
| 138.56 | | 458.8515 | 0.056 | 453 | –1.27525 |

**Table 16. ADC2 Input Measurement With THS4521**

| AC INPUT (V) | FREQ (Hz) | EXPECTED SAMPLES | RMS INPUT (V) | MEASURED SAMPLES | % ERROR |
|---|---|---|---|---|---|
| 433 | 50 | 1433.911 | 0.175 | 1423 | –0.76092 |
| 346.4 | | 1155.322 | 0.141 | 1152 | –0.28758 |
| 173.2 | | 581.7581 | 0.071 | 588 | 1.072932 |
| 138.56 | | 458.8515 | 0.056 | 453 | –1.27525 |
| 433 | 60 | 1433.911 | 0.175 | 1433 | –0.06352 |
| 346.4 | | 1155.322 | 0.141 | 1142 | –1.15314 |
| 173.2 | | 581.7581 | 0.071 | 577.5 | –0.73194 |
| 138.56 | | 458.8515 | 0.056 | 453 | –1.27525 |

## 7.4 ADC Performance Testing—DFR

The ADC performance test for the digital fault recorder has been performed with a 12-, 14-, and 16-bit ADSxx54 EVM. The waveforms have been plotted on a GUI. The input has been sampled at a sampling rate of up to 1 MHz. To simulate an input up to 60 kHz, a function generator has been used. The 50-Hz inputs are provided using a programmable voltage source. The samples are captured by the SDCC card and plotted using the GUI. The following subsections provide the waveform plot and the accuracy measurement results under different conditions.

### 7.4.1 ADC Samples Waveform Plot

#### 12-bit ADS7254

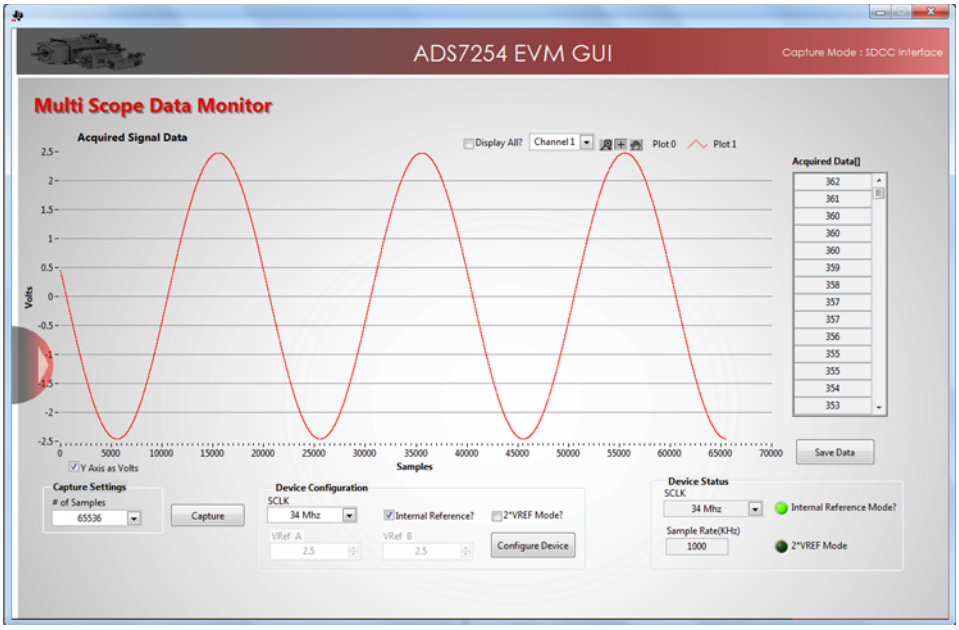



**Figure 41. 12-Bit ADS7254 at 50 Hz**

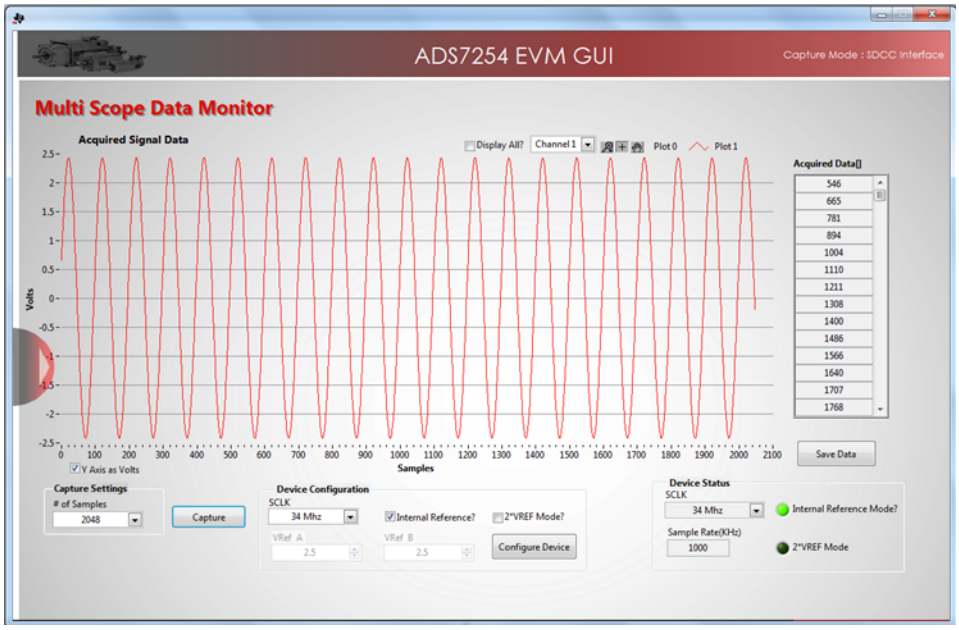



**Figure 42. 12-Bit ADS7254 at 10 kHz**

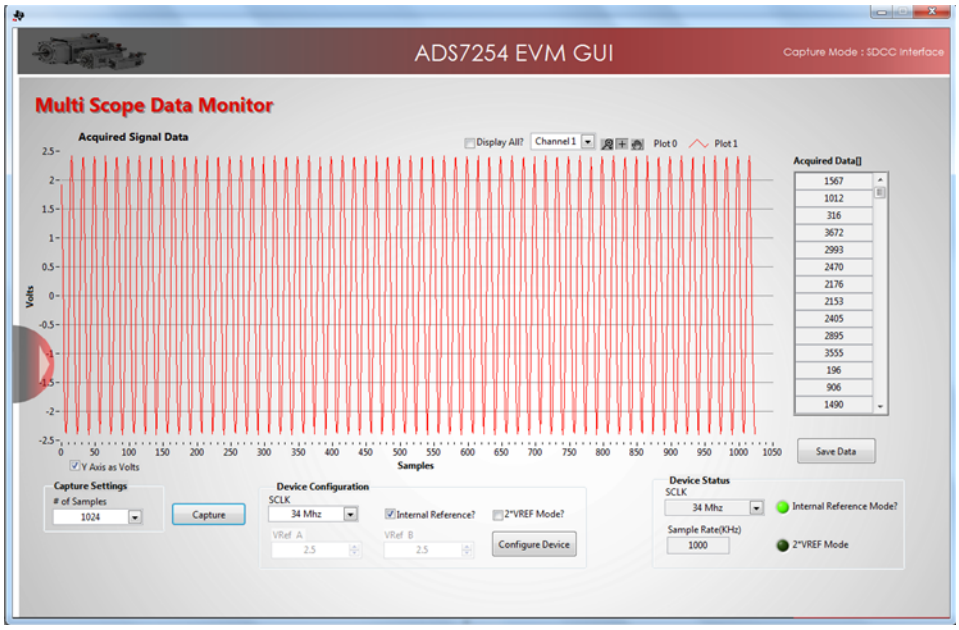



**Figure 43. 12-Bit ADS7254 at 60 kHz**

### 14-bit ADS7854

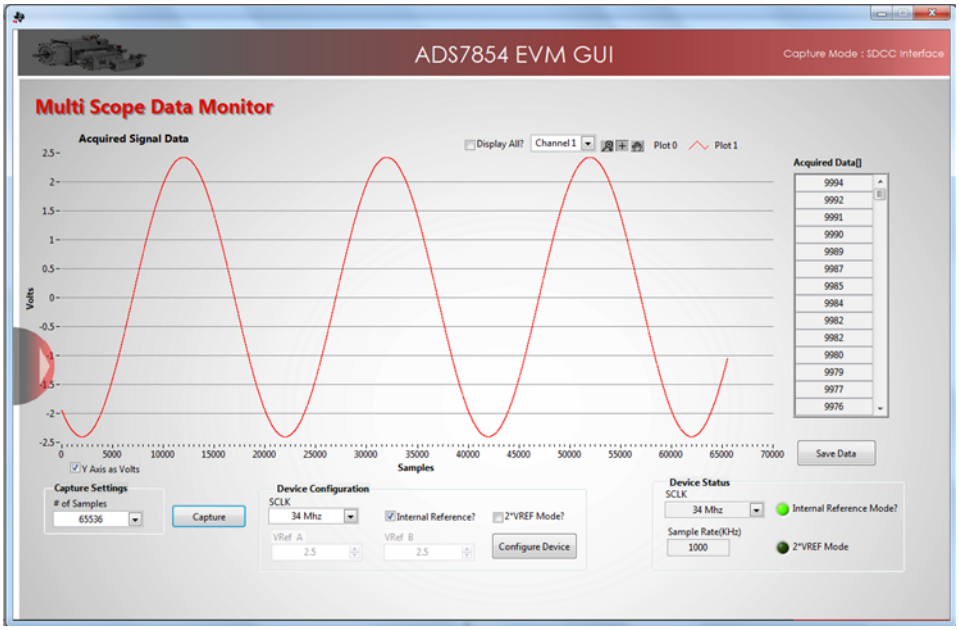



**Figure 44. 14-Bit ADS7854 at 50 Hz**

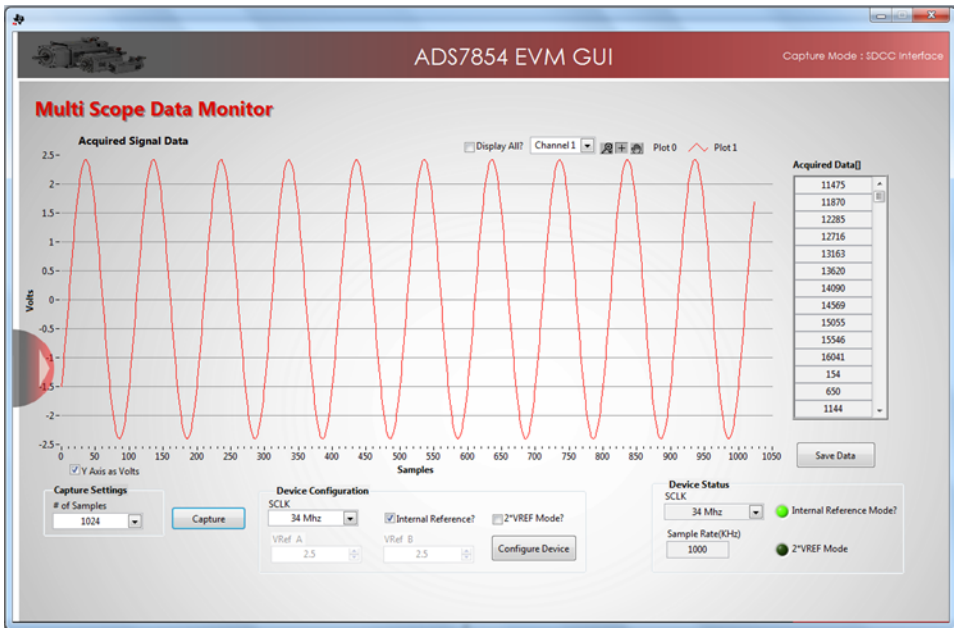



**Figure 45. 14-Bit ADS7854 at 10 kHz**

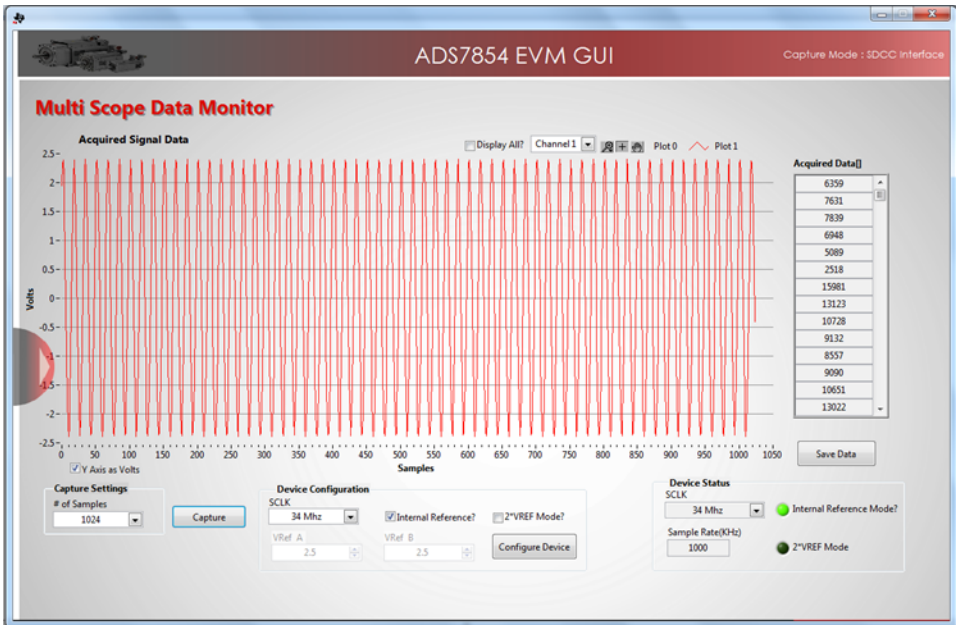



**Figure 46. 14-Bit ADS7854 at 60 kHz**

### 16-bit ADS8354

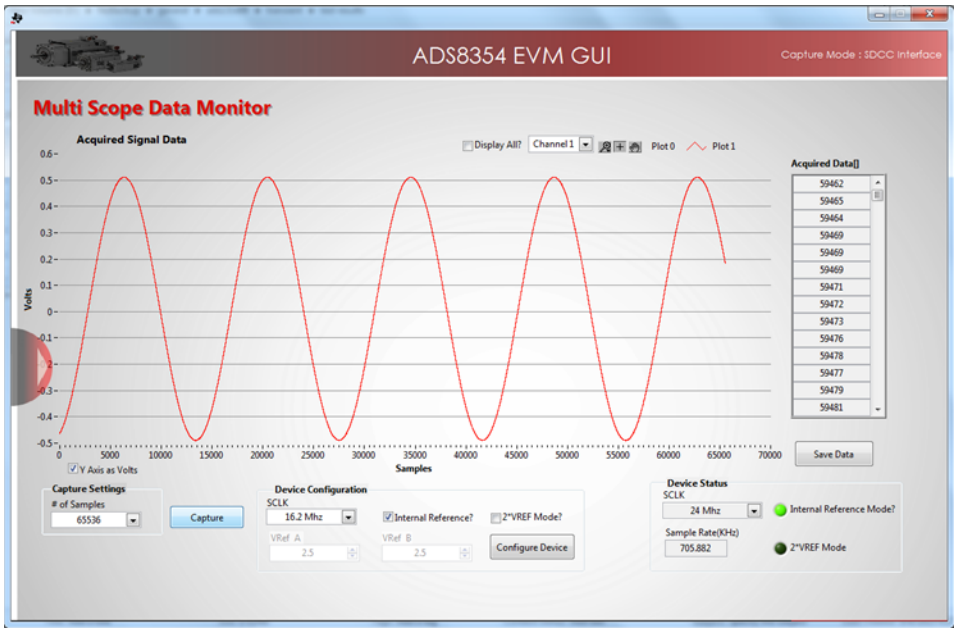



**Figure 47. 16-Bit ADS8354 at 50 Hz**

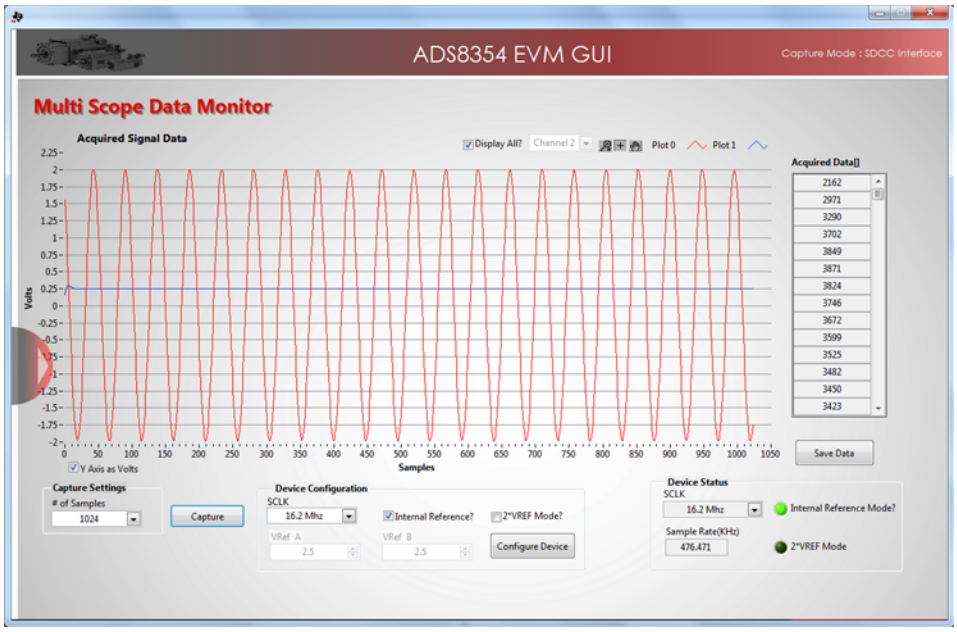



**Figure 48. 16-Bit ADS8354 at 10 kHz**

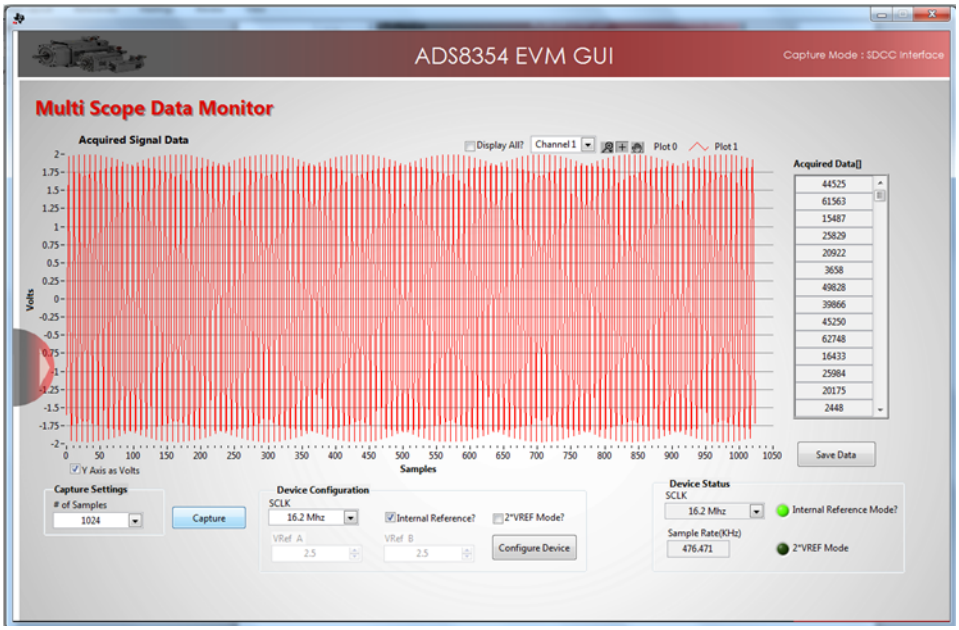



**Figure 49. 16-Bit ADS8354 at 60 kHz**

### 7.4.2 ADS7254 12-Bit Performance Testing

**Test with high-frequency signal input using function generator**

**Table 17. ADC1 Measurement With 50-Hz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 50-Hz % ERROR |
|---|---|---|
| 93.710 | 93.352 | –0.382 |
| 352.200 | 352.192 | –0.002 |
| 704.500 | 701.556 | –0.418 |
| 1409.000 | 1409.477 | 0.034 |
| 1744.000 | 1739.745 | –0.244 |

**Table 18. ADC1 Measurement With 10-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 10-kHz % ERROR |
|---|---|---|
| 93.650 | 93.352 | –0.318 |
| 352.000 | 350.071 | –0.548 |
| 703.900 | 700.707 | –0.454 |
| 1408.000 | 1407.355 | –0.046 |
| 1711.000 | 1704.385 | –0.387 |

**Table 19. ADC1 Measurement With 60-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 60-kHz % ERROR |
|---|---|---|
| 93.030 | 92.645 | –0.414 |
| 350.250 | 348.515 | –0.495 |
| 700.800 | 696.605 | –0.599 |
| 1400.700 | 1393.211 | –0.535 |
| 1703.000 | 1692.362 | –0.625 |

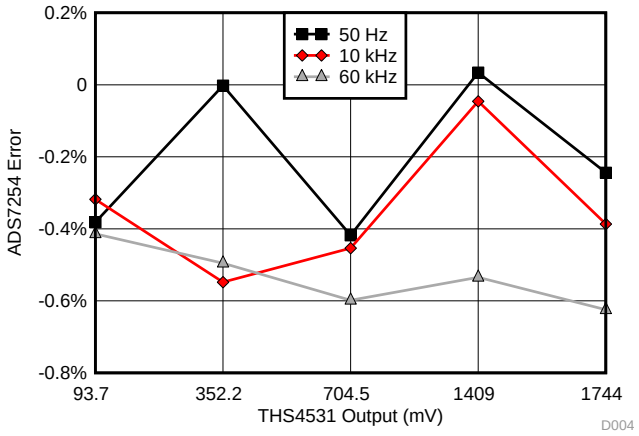



**Figure 50. Differential Amp Output versus 12-Bit ADC Error**

**Test with 50-Hz AC input**

**Table 20. ADC1 Measurement With 12-Bit, THS4521, and PD (Impedance ≈ 150 kΩ)**

| AC VOLTAGE (V) | THS4521 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 25.000 | 86.150 | 85.573 | –0.670 |
| 50.000 | 172.200 | 171.146 | –0.612 |
| 86.660 | 298.500 | 297.030 | –0.493 |
| 173.200 | 596.800 | 594.059 | –0.459 |
| 259.800 | 895.500 | 891.089 | –0.493 |

**Table 21. ADC1 Measurement With 12-Bit, THS4531, and PD (Impedance ≈ 550 kΩ)**

| AC VOLTAGE (V) | THS4521 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 43.300 | 48.880 | 48.798 | –0.168 |
| 86.600 | 97.820 | 97.595 | –0.230 |
| 173.000 | 195.600 | 194.484 | –0.571 |
| 346.000 | 391.400 | 388.967 | –0.621 |

### 7.4.3 ADS7854 14-Bit Performance Testing

**Test with high-frequency signal input using function generator**

**Table 22. ADC1 Measurement With 50-Hz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 50-Hz % ERROR |
|---|---|---|
| 90.480 | 90.523 | 0.048 |
| 336.500 | 335.926 | –0.170 |
| 702.000 | 700.141 | –0.265 |
| 1405.000 | 1401.697 | –0.235 |
| 1704.000 | 1704.385 | 0.023 |

**Table 23. ADC1 Measurement With 10-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 10-kHz % ERROR |
|---|---|---|
| 90.440 | 90.523 | 0.092 |
| 336.300 | 338.048 | 0.520 |
| 701.900 | 700.141 | –0.251 |
| 1404.000 | 1396.747 | –0.517 |
| 1703.000 | 1697.313 | –0.334 |

**Table 24. ADC1 Measurement With 60-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | 60-kHz % ERROR |
|---|---|---|
| 89.850 | 89.816 | –0.038 |
| 334.700 | 336.634 | 0.578 |
| 698.800 | 700.141 | 0.192 |
| 1396.000 | 1396.747 | 0.053 |
| 1692.000 | 1697.313 | 0.314 |

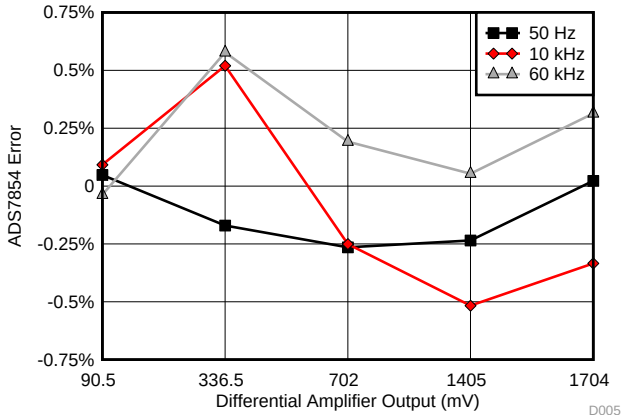



**Figure 51. Differential Amp Output versus 14-Bit ADC Error**

### Test with 50-Hz AC input

**Table 25. ADC1 Measurement With 14-Bit, THS4521, and PD (Impedance ≈ 150 kΩ)**

| AC VOLTAGE (V) | THS4521 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 25.000 | 86.150 | 85.573 | –0.670 |
| 50.000 | 172.200 | 171.853 | –0.202 |
| 86.660 | 298.500 | 297.030 | –0.493 |
| 173.200 | 596.800 | 595.474 | –0.222 |
| 259.800 | 895.500 | 892.504 | –0.335 |

**Table 26. ADC1 Measurement With 14-Bit, THS4531, and PD (Impedance ≈ 550 kΩ)**

| AC VOLTAGE (V) | THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 43.300 | 48.880 | 48.798 | –0.168 |
| 86.600 | 97.820 | 97.595 | –0.230 |
| 173.000 | 195.600 | 195.191 | –0.209 |
| 346.000 | 391.400 | 390.382 | –0.260 |

## 7.4.4 ADS8354 16-Bit Performance Testing

### Test with high-frequency signal input using function generator

**Table 27. ADC1 Measurement With 50-Hz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—PEAK (mV) | ADC OUTPUT—RMS (mV) | 50-Hz % ERROR |
|---|---|---|---|
| 93.770 | 132.000 | 93.352 | –0.446 |
| 353.200 | 498.000 | 352.192 | –0.285 |
| 705.200 | 994.000 | 702.970 | –0.316 |
| 1410.000 | 1986.000 | 1404.526 | –0.388 |

**Table 28. ADC1 Measurement With 10-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—PEAK (mV) | ADC OUTPUT—RMS (mV) | 10-kHz % ERROR |
|---|---|---|---|
| 93.750 | 132.000 | 93.352 | –0.424 |
| 352.300 | 495.000 | 350.071 | –0.633 |
| 704.000 | 990.000 | 700.141 | –0.548 |
| 1409.000 | 1980.000 | 1400.283 | –0.619 |

**Table 29. ADC1 Measurement With 60-kHz Input**

| THS4531 OUTPUT (mV) | ADC OUTPUT—PEAK (mV) | ADC OUTPUT—RMS (mV) | 60-kHz % ERROR |
|---|---|---|---|
| 93.160 | 131.000 | 92.645 | –0.553 |
| 350.700 | 494.000 | 349.364 | –0.381 |
| 701.600 | 985.000 | 696.605 | –0.712 |
| 1402.000 | 1970.000 | 1393.211 | –0.627 |

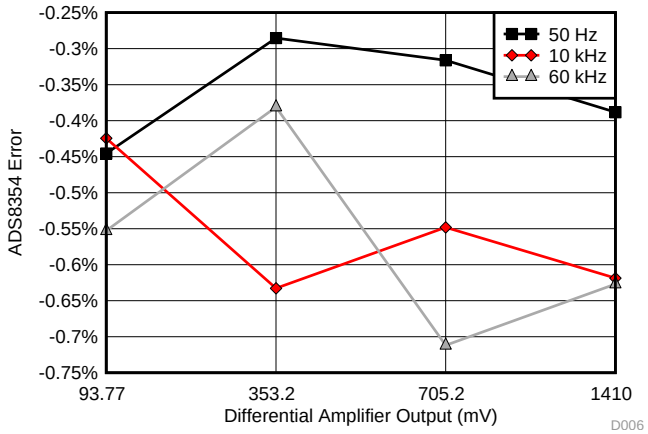



**Figure 52. Differential Amp Output versus 16-Bit ADC Error**

### Test with 50-Hz AC input

**Table 30. ADC1 Measurement With 16-Bit, THS4521, and PD (Impedance ≈ 150 kΩ)**

| AC VOLTAGE (V) | THS4521 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 25.000 | 86.150 | 85.926 | –0.259 |
| 50.000 | 172.200 | 171.853 | –0.202 |
| 86.660 | 298.500 | 297.595 | –0.303 |
| 173.200 | 597.100 | 595.474 | –0.272 |
| 259.800 | 895.760 | 894.625 | –0.127 |

**Table 31. ADC1 Measurement With 16-Bit, THS4531, and PD (Impedance ≈ 550 kΩ)**

| AC VOLTAGE (V) | THS4531 OUTPUT (mV) | ADC OUTPUT—RMS (mV) | % ERROR |
|---|---|---|---|
| 43.300 | 48.880 | 48.798 | –0.168 |
| 86.600 | 97.820 | 97.595 | –0.230 |
| 173.000 | 195.600 | 195.191 | –0.209 |
| 346.000 | 391.400 | 390.382 | –0.260 |

**NOTE:** Samples have been captured over a random power cycle (not zero cross to zero cross).

## 7.5 IEC Precompliance Testing

The TIDA-00499 design has been tested for the IEC61000-4-5 standard for surge. Table 32 shows the performance criteria for this test.

**Table 32. Performance Criteria**

| CRITERIA | PERFORMANCE (PASS) CRITERIA |
|---|---|
| A | The analog output module continues to operate as intended. No loss of function or performance, even during the test. |
| B | Temporary degradation of performance is acceptable. After the test, the analog output module continues to operate as intended without manual intervention. |
| C | Loss of functions is acceptable during the test, but destruction of hardware or software is not. After the test, the analog output module continues to operate automatically as intended after a manual restart, power off, or power on. |

### 7.5.1 IEC61000-4-5 Surge Immunity Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of one minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification has been used for this test. The test generator was configured for 1.2/50 μs and 42-Ω surges. A series of five negative and positive pulses, with ten seconds spacing between each pulse, have been applied during the test. The TIDA-00499 board has been tested for performance before and after the test. The equipment under test (EUT) performed normally after each test.

**Table 33. Surge Test Observations**

| IMMUNITY TEST | STANDARD | PORT | TARGET VOLTAGE | RESULT |
|---|---|---|---|---|
| Surge and diff mode | IEC 61000-4-5: (1.2 / 50 μs to 8 / 20 μs), 42 Ω–0.5 μF | Across the potential divider | ± 4 kV | Pass, criteria B (After the test the module continued to operate as intended) |

**Table 34. Surge Test Steps**

| TEST NO. | TEST MODE | OBSERVATION |
|---|---|---|
| 1 | 1 kV | Pass |
| 2 | –1 kV | Pass |
| 3 | 2 kV | Pass |
| 4 | –2 kV | Pass |
| 5 | 4 kV | Pass |
| 6 | –4 kV | Pass |

The following Figure 53 shows the surge setup for the AFE used in the transient recorder and digital fault recorder.

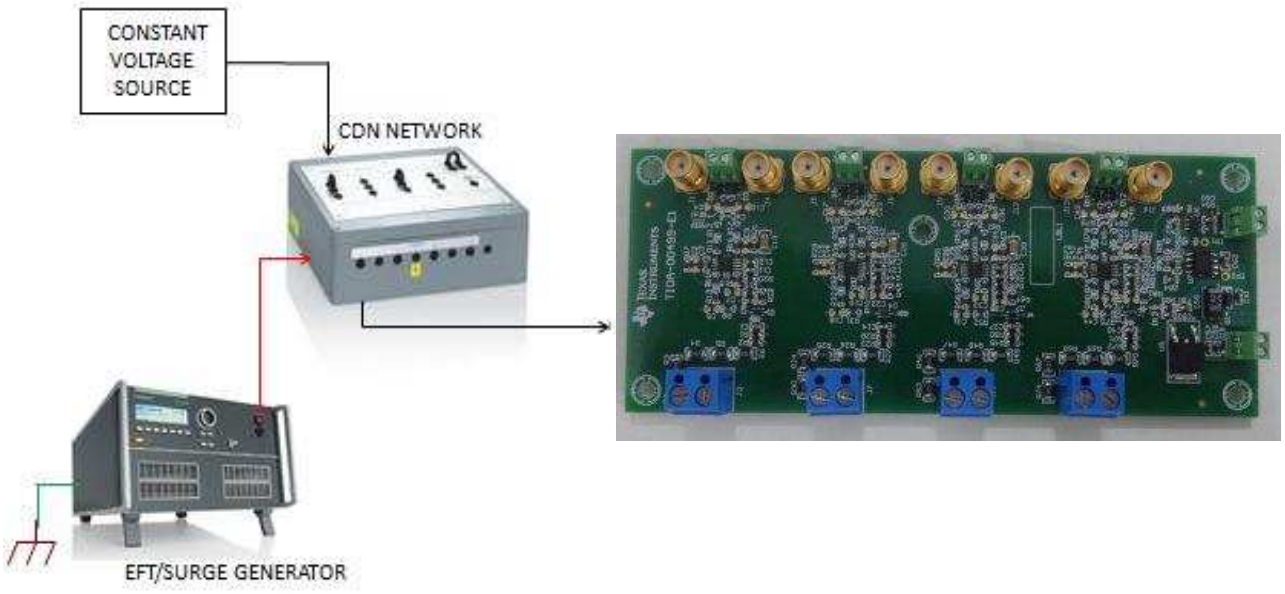



**Figure 53. Surge Setup for AFE Used in TR and DFR**

## 7.6 Summary of Test Results

**Table 35. Test Results**

| SERIAL NUMBER | PARAMETERS | RESULT |
|---|---|---|
| 1 | Power supply and reference for AFE | Ok |
| 2 | Potential divider and differential amplifier performance | Ok |
| 3 | 14-bit ADC3441 performance – pipeline | Ok |
| 4 | 12-bit - ADS7254 performance - SAR | Ok |
| 5 | 14-bit - ADS7854 performance - SAR | Ok |
| 6 | 16-bit - ADS8354 performance - SAR | Ok |
| 8 | Surge testing with 42-Ω impedance | Ok |

# 8 Design Files

## 8.1 Schematics

To download the schematics for each board, see the design files at TIDA-00499.

## 8.2 Bill of Materials

To download the Bill of Materials (BOM) for each board, see the design files at TIDA-00499.

## 8.3 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00499.

## 8.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00499.

## 8.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00499.

## 8.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00499.

# 9 References


1. Texas Instruments, *ADS8354EVM-PDK and ADS7854EVM-PDK*, User's Guide (SBAU209)
2. Texas Instruments, *ADC3xxx, ADC3xJxx EVM User's Guide*, User's Guide (SLAU579)
3. Texas Instruments, TIPD211 Product Page (http://www.ti.com/tool/tipd211)
4. Texas Instruments, TIDA-00772 Product Page (http://www.ti.com/tool/tida-00772)
5. Texas Instruments, TIDA-01036 Product Page (http://www.ti.com/tool/TIDA-01036)
6. Texas Instruments, ADS9120EVM-PDK Product Page (http://www.ti.com/tool/ads9120evm-pdk)
7. Texas Instruments, TIDA-00799 Product Page (http://www.ti.com/tool/TIDA-00799)


# 10 Terminology

**DFR—** Digital fault recorder

**TR—** Transient recorder

**TWFL—** Traveling wave fault locator

**SDCC—** Serial data control card

**LVDS—** Low-voltage differential signaling

**HV—** High voltage

**MV—** Medium voltage

**PD—** Potential divider

# 11 About the Author

**KALLIKUPPA MUNIYAPPA SREENIVASA** is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his Bachelor of Electronics (BE) in electronics and communication engineering (BE-E&C) from VTU, Mysore, India.

## Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (December 2015) to A Revision | Page |
|---|---|
| • Changed title from *AFE for Transient Recorder and Digital Fault Recorder Using High-Speed ADCs and Differential Amplifiers* | 1 |
| • Added last paragraph in Design Overview | 1 |
| • Added ADS9120 to Design Resources | 1 |
| • Added THS4551 to Design Resources | 1 |
| • Deleted TPS7A6533 from Design Resources | 1 |
| • Added REF5025 to Design Resources | 1 |
| • Added OPA322 to Design Resources | 1 |
| • Deleted "Differential Amplifier Front-End (THS4531, THS4521, or THS4551) to Interface AC Transient Inputs to Differential Input ADC" from Design Features | 1 |
| • Deleted "Onboard 0.995-V (1.024-V) Reference for Transient Capture and 2.5 V for DFR" from Design Features | 1 |
| • Added "Differential Amplifier Front-End (THS4531, THS4521, or THS4551) to Interface Transient Inputs to ADC With Onboard Reference of 0.995 V (1.024 V) or 2.5 V" to Design Features | 1 |
| • Deleted "Measurement Range: Capture Input Voltage Transient from 250 V to ≥ 2-kV Peak, 1.2/50 µs" from Design Features | 1 |
| • Deleted "Measurement Sensitivity: ± 20-V (Resolution) from 10% to 100% of Input Voltage Range (2-kV Peak)" from Design Features | 1 |
| • Deleted "Measurement Accuracy: < ±10% ±15 V from 10% to 100% of Input Voltage (at > 10 kHz) for Transient Capture" from Design Features | 1 |
| • Added "Capture Input Voltage Transient From 250 V to ≥ 2-kV Peak, 1.2/50 µs With ± 20-V Resolution From 10% to 100% of Input Voltage Range With Accuracy of < ±10% ±15 V From 10% to 100% of Input Voltage (at > 10 kHz) for Transient Capture" to Design Features | 1 |
| • Deleted "Power Quality Analyzers" from Featured Applications | 1 |
| • Added "Sequence of Even Recorder (SOE)" and "Sequence of Fault Recorder (SFR)" to Featured Applications | 1 |
| • Added the THS4551 differential amplifier to Section 1.5.2 | 6 |
| • Added ADS9120 to Section 1.5.3 | 7 |
| • Added ADS9120EVM-PDK to Section 1.5.3 | 7 |
| • Added Section 4.10 | 31 |

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